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The Test Guide For CMOS-On-SIMOX Test Chips NIST3 and NIST4

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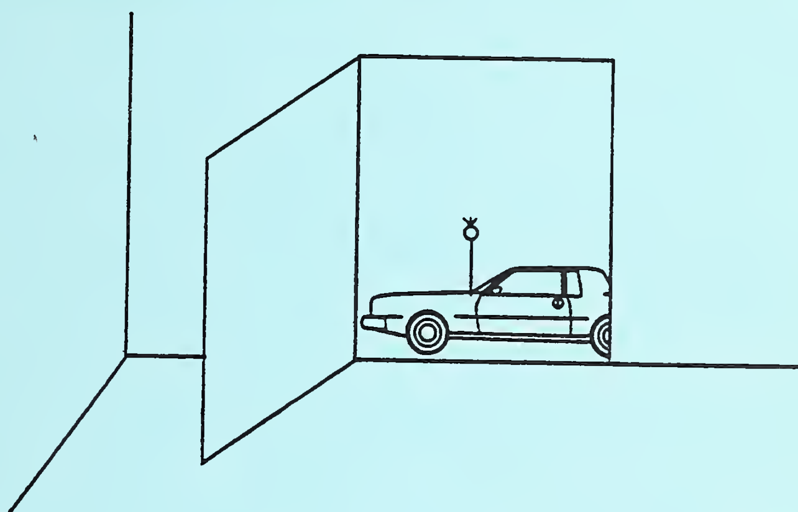

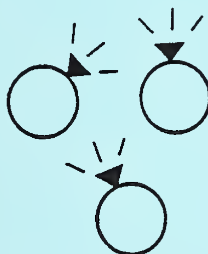

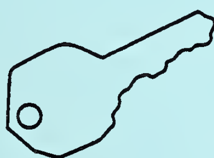

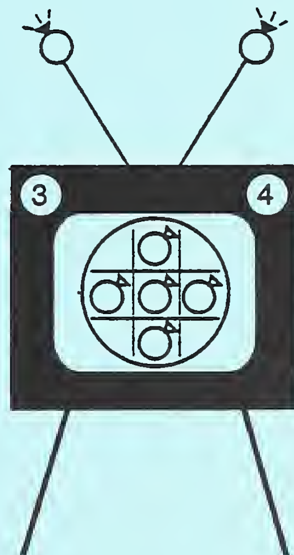

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THE TEST GUIDE FOR CMOS-ON-SIMOX TEST CHIPS NIST3 AND NIST4

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ABSTRACT

A test chip set has been designed for process monitoring and device parameter extraction for a CMOS (Complementary Metal-Oxide-Semiconductor)-on-SOI (Silicon-On-Insulator) process. The chips contain structures which are common to a standard CMOS process as well as structures specifically designed for a SIMOX (Separation by the IMplantation of OXygen) process.

NIST3 is 6380 μm $\times$ 4780 μm and contains several large-geometry MOSFETs, resistors, and capacitors. NIST4 is 1 cm $\times$ 1 cm and contains approximately 300 small-geometry test structures. The SIMOX specific structures found on these chips include MOSFETs, capacitors, interconnects, and pads. This report presents the information necessary to test NIST3 and NIST4.

Design guidelines, technology file modifications, and data output specifications for NIST3 and NIST4 are discussed in a separate manual [1].

Key words: Magic; MOSFET; NIST3; NIST4; SIMOX; SOI; test chip; test structure

1. INTRODUCTION

Two test chips, NIST3 and NIST4, have been designed for a SIMOX process. This design can be used to monitor or evaluate different SIMOX processes. This report presents the information necessary to test these chips. Since SIMOX is a relatively new technology, new or modified test structures are needed to obtain the process and device parameters. NIST3 contains several large-geometry MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), resistors, and capacitors, and NIST4 contains approximately 300 small-geometry test structures. These chips include structures for process monitoring and device parameter extraction. The SIMOX specific structures found on these chips include MOSFETs, capacitors, interconnects, and pads. Many structures common to a CMOS process are also included.

The design guide for these chips [1] describes the details of how the SIMOX structures were designed. This report is a quick reference guide for testing NIST3 and NIST4. It is assumed that the reader is already familiar with test structures, their testing, and the fundamentals of SIMOX processing.

In this report, brief overviews of the SIMOX process and the design rules are given in sections 2 and 3, respectively. Section 4 describes the general architecture of NIST4, which is divided into parts, and describes the structures within these parts. Section 5 describes the test chip NIST3. For completeness some of the sections found in the design guide are included in this testing manual.

The organization of the tables and figures in this report will aid the user by providing a quick reference for testing the devices. The tables and figures associated with NIST4 are given first, followed by the tables and figures for NIST3. NIST4 is shown in figure 1, followed by the key to the shading in figure 2. Table 1 lists the structures found according to their general vicinity in the four parts comprising NIST4. Figures 3, 4, 5, and 6 illustrate Parts I, II, III, and IV, respectively. Table 2 lists the basic structures found on NIST4 and the parameters measured.

Tables 3 through 11 list the designed cell name, critical dimensions, and electrical pad connections for the Part-I structures for each of the columns. This information is helpful when testing the structures. Figures 7 through 20 illustrate sample structures found in these columns. Tables 12 and 13, tables 14 through 16, and table 17 list this information for the Part-II, -III, and -IV structures, respectively. The sample structures for these parts can be found in figures 21 through 24, figures 25 through 27, and figures 28 and 29, respectively. Additional test structure information is given in table 18 and the structures are shown in figures 30 through 34.

NIST3 is shown in figure 35 followed by its cell structure in figure 36. The NIST3 test structure list is given in table 19 followed by an illustration of each of these structures in figures 37 through 58.

For completeness, some of the sections found in the design guide [1] are included in this testing manual.

2. THE SIMOX PROCESS

The mask set is designed for positive photoresist and subtractive etching. Positive photoresist is initially crosslinked, and exposure to UV light to areas selected by the masks breaks this crosslinking, enabling the exposed photoresist to be removed by an alkaline-aqueous developer. Since only positive photoresist is used, some masks are clear field while others are dark field. The dark areas on the mask do not allow UV light to penetrate. In general, for any features with layer height (i.e., island, polysilicon, and metal), everything but the feature needs to be etched; therefore, a clear field mask is needed. For the other features, where the photoresist and/or SiO_2, glass, or passivation needs to be etched away, thus

creating a "hole" for a contact or an area in which to implant a dopant, a dark field mask is needed.

The masks were made by the mask vendor from a tape of the digitized features. The masks must be specified to the mask vendor as clear field or dark field. Dark field masks imply the features defined in the CAD graphic layout editor, Magic,* are clear with an opaque background. Conversely, clear field masks imply the features defined in Magic are opaque with a clear background. Below are the processing masks (in the order in which they are used) with the appropriate clear or dark fields (not to be confused with clear or dark features which is the reverse):

1. ISLAND (clear field mask)
2. NWELL (dark field mask)
3. PWELL (dark field mask)
4. POLYSILICON (clear field mask)
5. NDIFFUSION (dark field mask)
6. SUBSTRATE CONTACT (dark field mask)
7. PDIFFUSION (dark field mask)
8. SUBSTRATE CONTACT (dark field mask)
   OTHER CONTACTS (dark field mask)
9. METAL (clear field mask)
10. GLASS (dark field mask)

The contact mask in Step 8 does not include the substrate contact cuts; therefore, the substrate contact mask must be reused to expose these regions.

The distinction between locos and mesa isolation is mainly determined by the process sequence, not by the mask polarity. The island mask for a mesa process is similar, yet not equivalent, to the active area mask in a locos process.

In SIMOX processing, the implanted, annealed film does not retain the initial substrate doping level after the high-temperature anneal. The substrate should be lightly doped (in this case, the substrate is *p*-type) to minimize capacitive coupling, while the scaling rules for submicrometer MOSFETs dictate relatively high-channel doping. Therefore, the mask set is designed to use four implants: nwell, pwell, ndiffusion, and pdiffusion. The polysilicon gates and interconnects are doped n^{++} by $POCl_3$ (phosphorus oxychloride) annealing. *N*-channel MOSFETs have a p^- implant in the channel area (which Magic calls pwell) with an n^+ source/drain implant (which Magic calls ndiffusion), while the *p*-channel MOSFETs have an n^- implant in the channel area (nwell) with a p^+ source/drain implant (pdiffusion).

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* In this paper commercial equipment, instruments, and computer programs are identified to specify adequately the procedure. This does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment or program is the best available for the purpose.

3. THE DESIGN RULES

Conservative design rules were used for designing NIST3 and NIST4 [1]. The design rules that were followed are given in Appendix B. These rules include a polysilicon width of 6 μm. This allowed for considerable overetch and still to have working parts. Also the ndiffusion contact (called ndc in the technology file) to *n*-channel MOSFET gate (nfet) and pdiffusion contact (pdc) to *p*-channel MOSFET gate (pfet) spacing rules were 2 μm apart.

After the design rules were chosen, the technology file was modified to reflect them. Therefore, any violations will be flagged interactively.

4. TEST CHIP NIST4

4.1 The General Architecture

The general architecture of NIST4 consists of four parts. The first part is the left side of the central area as shown in figure 3. It has twelve columns (2 pads wide) of four placements of 2 by 10 pads on 160-μm centers. These provide access to elemental active devices, inverters, and dc parametric test structures. An extra row of substrate contact test structures is included in the columns to assure contact to the substrate for each probe card placement. The right side of the central area has three columns of four 2 by 10 pad placements for circuits and their elemental parts. These Part-II structures are shown in figure 4. Again, an extra row of substrate contact test structures is included in the columns.

On the chip, the first and second parts of the design are surrounded by the third and fourth parts. Both occupy a flange about 1.6 mm wide which makes the composite layout consistent with a total step-and-repeat distance of 1 cm (not including the separation between chips). The size of the test chips was actually determined by the number, size, and spacing of the bondable pads required for each chip as well as the number of test chips possible per wafer given their size. The Part-III structures (shown in fig. 5) include the transistors connected to bondable pads for radiation studies. The Part-IV structures (shown in fig. 6) comprise the area between the bonded transistors and the core area. This area is used for systematic variations of new test structures. On NIST4, this area includes transistors padded out to be compatible with rf-probe cards for on-wafer rf testing.

The structures found on NIST4 are listed in table 2.

4.2 The Bond Pads and Contact Pads

The bond pads and contact pads for both test chips were designed as a composite structure of glass, metal, polysilicon contact, polysilicon, and island. The polysilicon level was included to add extra strength to the pads for multiple probing purposes. The polysilicon contact enables the designer to interface the test structures with the pad in polysilicon as well as metal without using an extra contact. The island level was included to minimize

capacitive coupling to the substrate.

The bond pads are located around the periphery of both chips, and the contact pads are in the center of NIST4 organized such that a 2 by 10 probe card can be used. The center of the contact pads are 160 μm apart. The dimensions for these pads (after CIF, Caltech Intermediate Form) are:

(a) Island (120×120 μm)
(b) Polysilicon (100×100 μm)
(c) Polysilicon contact (76×76 μm)
(d) Metal1 (80×80 μm)
(e) Via (72×72 μm)
(f) Metal2 (76×76 μm)
(g) Glass (70×70 μm)

The bonding pads are considerably larger to allow room for bonding. Their dimensions (after CIF) are:

(a) Island (180×180 μm)
(b) Polysilicon (160×160 μm)
(c) Polysilicon contact (136×136 μm)
(d) Metal1 (140×140 μm)
(e) Via (102×102 μm)
(f) Metal2 (106×106 μm)
(g) Glass (100×100 μm)

The island level in the bonding pads is 200 μm away from the edge of the chip, which is lenient for bonding purposes (which requires at least 100 μm).

Given a plot of the test chip, it is easy to figure out the scale of the plot with the above dimensions.

4.3 The Part-I Structures

The test structures in Part I were designed to be probed with 2 by 10 probes using 80-μm probe pads on 160-μm centers. The test structures were organized on a column-by-column basis as follows:

Column	
Column 1	18 n-channel MOSFETs with different channel lengths/widths and with the channel contact beside the drain
2	18 p-channel MOSFETs with different channel lengths/widths and with the channel contact beside the drain
3	9 cross-bridge resistors
4	10 inverters with different channel lengths
5	16 contact resistors
6	12 contact resistors

7	10 island-edge and other meanders
8	20 capacitors
9	20 capacitors
10	18 specially-sized (fat-FET, big square, etc.) MOSFETs
11	Repeat Column 1 (with channel contact near the channel)
12	Repeat Column 2 (with channel contact near the channel)

The rationale behind Columns 11 and 12 was to enable active transistor parameter extraction mapping when used in conjunction with Columns 1 and 2 and to explore a design variation regarding channel (well) contact placement.

The general order, from top to bottom, of test structures that merely change the material used is similar to the construction from top to bottom of a dissected structure, namely:

(a) Metal2 (optional)
(b) Metal1
(c) Polysilicon
(d) Ndiffusion (n^+ source/drain) - always before pdiffusion
(e) Pdiffusion (p^+ source/drain)
(f) Nwell (channel implant for *p*-channel MOSFETs) - always before pwell
(g) Pwell (channel implant for *n*-channel MOSFETs)
(h) Island

If contacts are considered, the order would be:

(a) Metal2-to-metal1 contact (optional)
(b) Polysilicon contact
(c) Ndiffusion contact
(d) Pdiffusion contact
(e) Nwell contact
(f) Pwell contact
(g) Island contact
(h) Substrate contact

When observing a test structure through a microscope, it is difficult to identify the critical dimensions. By labeling the test structures in metal with the critical dimension, these dimensions can then be read through a microscope.

The design considerations for the MOSFETs (in Columns 1,2 10-12) are given in the design guide [1]. A brief overview of some other basic parametric structures included in Part I (namely, cross-bridge resistors, inverters, contact resistors, island-edge and other meanders, and capacitors) follows:

1. Cross-bridge resistors (Column 3)

An example of a cross-bridge resistor [2] in polysilicon is given in figure 9. The possible

materials that can be used for this structure are metal2, metal1, polysilicon, nfet, pfet, ndiffusion, pdiffusion, nwell, pwell, and island. To make these other varieties, the polysilicon would be replaced with the appropriate material, and this material would be connected to the pads with metal1 using the appropriate contact (if needed). The diffusions and wells require the presence of the island layer in which to implant the dopants. The cross-bridge resistors were constructed with the same layers as would appear in an integrated circuit. For example, the opposite well with the diffusion cross-bridge resistors was included to simulate realistic device properties.

From the Van der Pauw [2] cross in the cross-bridge resistor, one determines the sheet resistance of the material using the formula:

$$R_s(\Omega/\square) = \frac{\pi \times f \times V}{I \times ln2}, \tag{1}$$

where I is the current forced, V is the voltage difference, and f is a correction factor (approximately one) that is related to the geometrical asymmetry of the structure. By repeating the measurements, reversing the current direction, and rotating the contacts by 90 deg, one can determine the effects of geometrical asymmetry, measurement voltage offsets, and Joule heating on the measurement.

From the bridge, the effective electrical linewidth (W_e) is calculated from the measurements and the sheet resistance using the formula:

$$W_e(\mu m) = \frac{R_s \times L_m \times I}{V}, \tag{2}$$

where R_s is the sheet resistance from (1), L_m is the design length between the bridge voltage taps (this dimension can be designed between 80 and 200 μm with negligible effect on the results), I is the current forced, and V is the voltage difference.

Effective linewidth, W_e, can also be expressed as:

$$W_e = W_m + ax_j \pm W_o, \tag{3}$$

where W_m is the designed photomask dimension, ax_j is the increase in width due to lateral diffusion for the implanted cross-bridges (note: $ax_j = 0$ for all other bridges), and W_o is the width offset due to the over or under etching in the photolithographic process.

All bridges on NIST4 are designed with $W_m = 10$ μm and $L_m = 130$ μm. When the bridge is rotated 90 deg, another linewidth measurement is possible from this orientation. The e-beam machine used to print the masks divides the masks into sections and works on a section at a time. When working on a section, the e-beam travels in the x-direction after

fine increments are made in the y-direction. Therefore, the linewidths on the masks may be different in the x- and y-directions, causing different linewidth results depending on the orientation.

2. Inverters (Column 4)

Inverters [3] with different channel lengths are included in this column. An example of one with channel lengths of 4 μm is given in figure 10. These inverters consist of an n-channel MOSFET and a p-channel MOSFET with twice the channel width of the n-channel MOSFET but with the same length. The design for these MOSFETs is similar to the ones in Columns 1 and 2.

These MOSFETs are on separate islands. The gates of the two MOSFETs are connected in polysilicon to form the input node, the drains are connected together to form the output node, the source of the n-channel MOSFET is connected to V_{SS}, and the source of the p-channel MOSFET is connected to V_{CC}. There is a substrate contact in the vicinity.

The only dimension that is changed in this structure throughout the column is the channel length.

3. Contact resistors (Columns 5 and 6)

Three types of contact resistors are included on NIST4. The first is the standard four-pad contact resistance structure (fig. 12) [4], the second is the Kelvin chain (fig. 13), and the third is a six-pad contact resistance structure (fig. 11).

For the four-pad contact resistance structure, the measured interfacial contact resistance is:

$$R_i = \frac{V_2 - V_1}{I}, \tag{4}$$

where the voltage taps are perpendicular to the direction of the current flow from one material, through the contact, to the next material. Interfacial contact resistance is an important parameter used in determining the performance of the fabrication process. The interfacial contact resistance is inversely proportional to the contact window area if the interfacial layer is uniform. Therefore, from plots of R_i versus contact area, one can ascertain approximate interfacial contact resistance values for all contact window sizes. These plots can be made from the measurements taken from strategically sized test structures in these columns.

For the Kelvin chain, the minimum design rules were used. From this chain, a measurement of the front contact resistance (not to be confused with the interfacial contact resistance) is possible using:

$$R_f = \frac{V_1 - V_2}{nI}, \tag{5}$$

where n = the number of contacts. Here, the voltage taps are at 90 deg to the direction of the current flow. This parameter is important for simulating circuit performance.

The six-pad contact resistance structure is similar to the four-pad contact resistance structure but is more versatile. In addition to measuring the interfacial contact resistance, the "end" contact resistance is obtained from which the "front" contact resistance is calculated. This structure and its measurement method were designed to minimize the effect of parasitic resistances and contact misalignments on the result.

4. Island-edge and other meanders (Column 7)

Polysilicon and metal are used as interconnects; therefore, they cross the island lip. As a result, the polysilicon or metal may break at these locations. Several test structures were included to test the integrity of the polysilicon (fig. 14) and metal as they meander over island edges [5]. These are small test structures. Metal atop polysilicon which meanders across the island edge are structures that are also included on NIST4 (fig. 15).

5. Capacitors (Columns 8 and 9)

The dimensions of the SIMOX structure preclude normal gate oxide capacitance measurements. The capacitance of the full gate-oxide-silicon-oxide-silicon structure has been simulated [6] under the assumption that the silicon film is completely isolated. Capacitors which meet these boundary conditions were included.

Figures 16, 17, and 18 are three capacitors which were designed for NIST4. Columns 8 and 9 include other capacitors [3], as well, from which to measure the capacitance between the various layers.

The capacitance is calculated using the formula:

$$C = \frac{\epsilon \times A}{d}, \tag{6}$$

where ϵ is the dielectric constant of the insulator, A is the area of the capacitor (i.e., the area of the smallest electrode), and d is the distance between the electrodes. The capacitors on NIST4 were designed to utilize as much area as possible inside a set of four probe pads.

4.4 The Part-II Structures

The following dynamic test structures are included in Part II:

(a) A 23-stage ring oscillator with NAND gate start-up circuitry

(b) A 4-stage output amplifier
(c) A NAND gate
(d) A 23-stage ring oscillator with output amplifier and NAND gate start-up circuitry
(e) A ring oscillator with a fanout of 2 and an output amplifier
(f) A 20-stage shift register
(g) A static RAM cell with the associated input and output circuitry
(h) Pieces of the larger dynamic structures (included in Column 13)
    (1) Inverters with the same dimensions as in the ring oscillators
    (2) *N*-channel MOSFETs of the same dimensions as in the dynamic integrated circuits
    (3) *P*-channel MOSFETs of the same dimensions as in the dynamic integrated circuits

These structures were designed in parts and then combined. For example, an inverter (with the minimum dimensions and using $W_p = 2 \times W_n$) was built, and this stage was copied repeatedly until the desired odd number of stages was obtained. This became the original ring oscillator. The components comprising the ring oscillator are pinned out separately in Column 13. These include the *n*-channel MOSFET, *p*-channel MOSFET, and inverter.

For the ring oscillators which included an output amplifier, the minimum dimensions were used in the first stage of the output buffer. Therefore, the inverter dimensions in the actual ring oscillator were made larger by a factor of 8 to minimize the loading of the output amplifier on the node of the ring oscillator. The channel widths in each successive stage in the output buffer were increased by a factor of 2 for design ease. This output amplifier was pinned out separately and placed in Column 14.

For the ring oscillators with NAND gate start-up circuitry, (as in fig. 21), the NAND gate was added in the place of an existing inverter and the dimensions $W_p = 2 \times W_n$ were used. This NAND gate is also pinned out separately and placed in Column 14.

A two-phase shift register was built (fig. 22). It consists of 20 inverters, each separated by a passgate whose gates are alternately connected to one of the two clocks. The last stage is connected to an output amplifier.

The dynamic integrated circuits on this chip were simulated on the CAD system using the event driven switch level simulator, esim [7]. These simulations are fast, interactive, and ensure continuity of the circuit. These simulations also assure the designer that the circuit is hooked up properly (i.e., the correct number of stages) and that the device sizes are sufficient. For more accurate and detailed simulations, especially in the time domain, they can be simulated using SPICE3; however, for the dynamic circuits chosen for NIST4 the simulations using esim are sufficient.

All of the dynamic test structures above were successfully simulated using esim. A six-transistor static RAM cell (fig. 23) was also designed and simulated. However, the simulations showed that it could not overwrite the existing data. This demonstrated that

several device sizes needed modification, and a new approach to rewriting the cell was initiated. A circuit diagram of the resulting cell is given in figure 24 along with the pertinent information to read and write the data in the cell.

All the above-mentioned dynamic test structures were designed using L=6 μm and placed in Column 14. Column 15 was made by modifying each structure in Column 14 to make L=4 μm and placing it in Column 15.

4.5 The Part-III Structures

Part III includes the following transistors to be bonded:

(a) The standard *n*-channel (fig. 25) and *p*-channel MOSFETs
(b) Closed-geometry *n*-channel and *p*-channel MOSFETs (fig. 27) to determine the degree of gate peripheral leakage
(c) Many-fingered *n*-channel and *p*-channel MOSFETs (fig. 26) to determine the degree of gate peripheral leakage

The bond pads along the top and left-hand edges of the chip are for *n*-channel MOSFETs, and the bond pads along the bottom and right-hand edges of the chip are for *p*-channel MOSFETs. Each MOSFET has a substrate contact next to it.

4.6 The Part-IV Structures

The rf transistors, the Part-IV structures, are located at the top and bottom of the chip (inside the bond pads). The *n*-channel rf transistors (fig. 28) are located in the top section, and the *p*-channel rf transistors (fig. 29) are located in the bottom section.

The metal input terminals for these transistors were designed to provide an approximate 50-Ω input impedance to minimize reflections [8]. Computer simulations were performed on a VAX VMS 11/780 to select the optimum dimensions using the program in the appendix. This program uses a simple model that does not account for a multilayer media such as is used here; therefore, variations in the results are expected. After several simulations, it was apparent that by designing three rf transistors, each with a different spacing ($\pm$10 μm with respect to the spacing required to achieve a 50-Ω input impedance), the near-correct spacing could be determined by measuring the reflected rf signal. The tapering of this spacing toward the device was done in 1-μm steps at a 45-deg angle to minimize reflections.

There are three rows of *n*-channel MOSFETs in the top section and three rows of *p*-channel MOSFETs in the bottom section. The first row in both sections uses a "50-Ω" pad spacing of 50 μm, the second row uses 60 μm, and the third row uses 70 μm. The channel length varies as one traverses each row.

Six pads are used for each rf transistor, however, well and substrate connections are not available.

4.7 Miscellaneous Structures

In addition to the test structures mentioned in the previous sections, NIST4 includes the following:

(a) Chip logo in metal (because it is easy to see through a microscope)
(b) Date design was completed in metal
(c) Alignment marks (for clear field masks and dark field masks) designed with respect to the island since this is the first level, and it has processing "height." These alignment marks are located in the upper left-hand corner of the chip. This makes the orientation of the masks easy during processing.
(d) Mask identifiers for each level (On NIST4, these are located in the right central area due to space constraints in the upper left-hand corner.)
(e) Chevrons (On NIST4 these are located in the right central area due to space constraints in the upper left-hand corner.)

5. TEST CHIP NIST3

NIST3 consists of a small number of relatively large test structures. These structures are designed to be probed by a combination of electrical and physical techniques. Therefore, all these devices are connected to bondable pads. These structures along with their critical dimensions and cell names are given in table 19.

The interdigitated MOSFETs (L=10 μm, $W = 7 \times 1500$ μm) with seven fingers are for easy SEM cross section and direct CV measurement of gate-to-drain capacitance. They were designed using large rectangular contacts as opposed to the conventional square contacts. This is to ensure a view of the contacts when the devices are cross-sectioned.

Large square transistors are included on this test chip for charge pumping experiments as well as length/width studies.

Two different varieties of capacitors (500 μm $\times$500 μm) were designed. One was designed to measure the gate oxide capacitance, and the other, to measure the capacitance of the buried oxide.

A bipolar structure (modified to be SIMOX compatible using the design rules) was included. It is an experimental silicon magnetotransistor.

6. CONCLUSIONS

Test chips NIST3 and NIST4 were designed for process monitoring and device parameter extraction for a CMOS-on-SOI process. They contain structures common to a standard CMOS process as well as structures specifically designed for a SIMOX process including MOSFETs, capacitors, interconnects, and pads.

This manual is a testing guide for NIST3 and NIST4. The organization of the tables and

figures helps provide a quick reference for testing these chips. This manual contains a brief overview of the SIMOX process and the design rules. The general architecture of NIST4, which is divided into parts, is given with a description of the structures within those parts. The test structures on NIST3 are also presented.

The design guidelines, technology file modifications, and data output specifications for NIST3 and NIST4 are discussed in the design guide [1].

7. ACKNOWLEDGMENTS

For comments on this report, we thank M. Gaitan and F. F. Oettinger. We appreciate the editorial assistance of J. A. Gonzalez, J. M. Rohrbaugh, and E. J. Walters. Thanks are also due to R. J. Mele for his graphical support.

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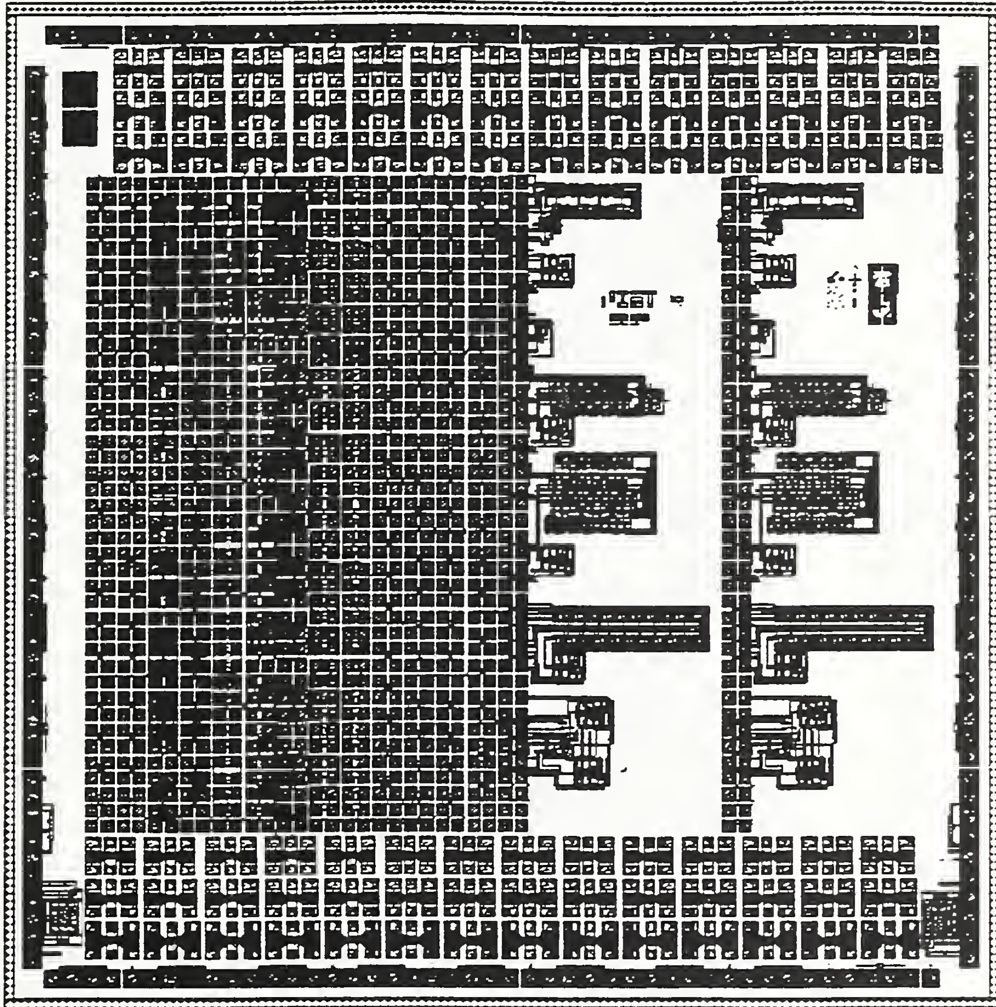


Figure 1. SIMOX Test Chip NIST4.

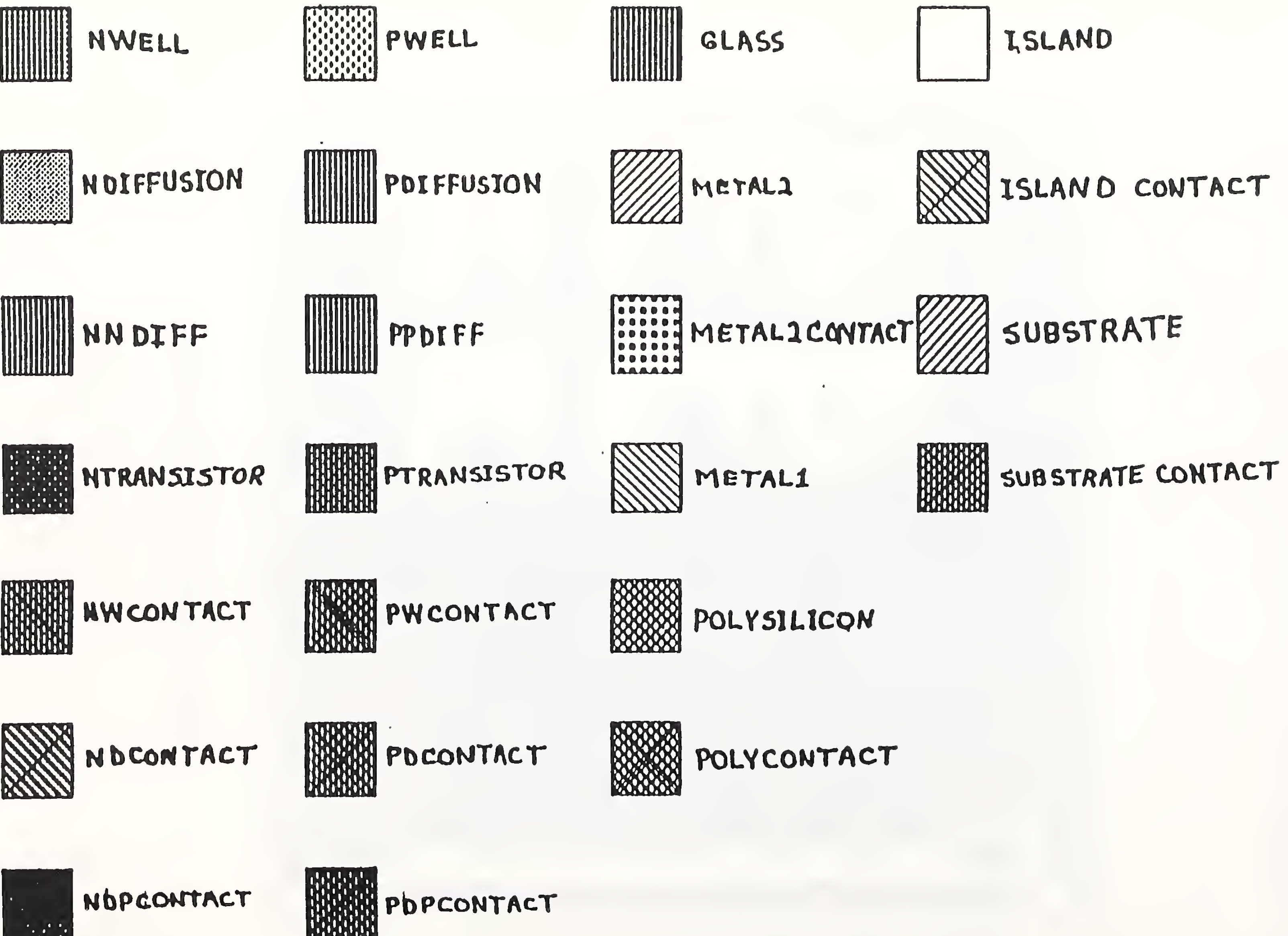


Figure 2. Key to the shading in the figures.

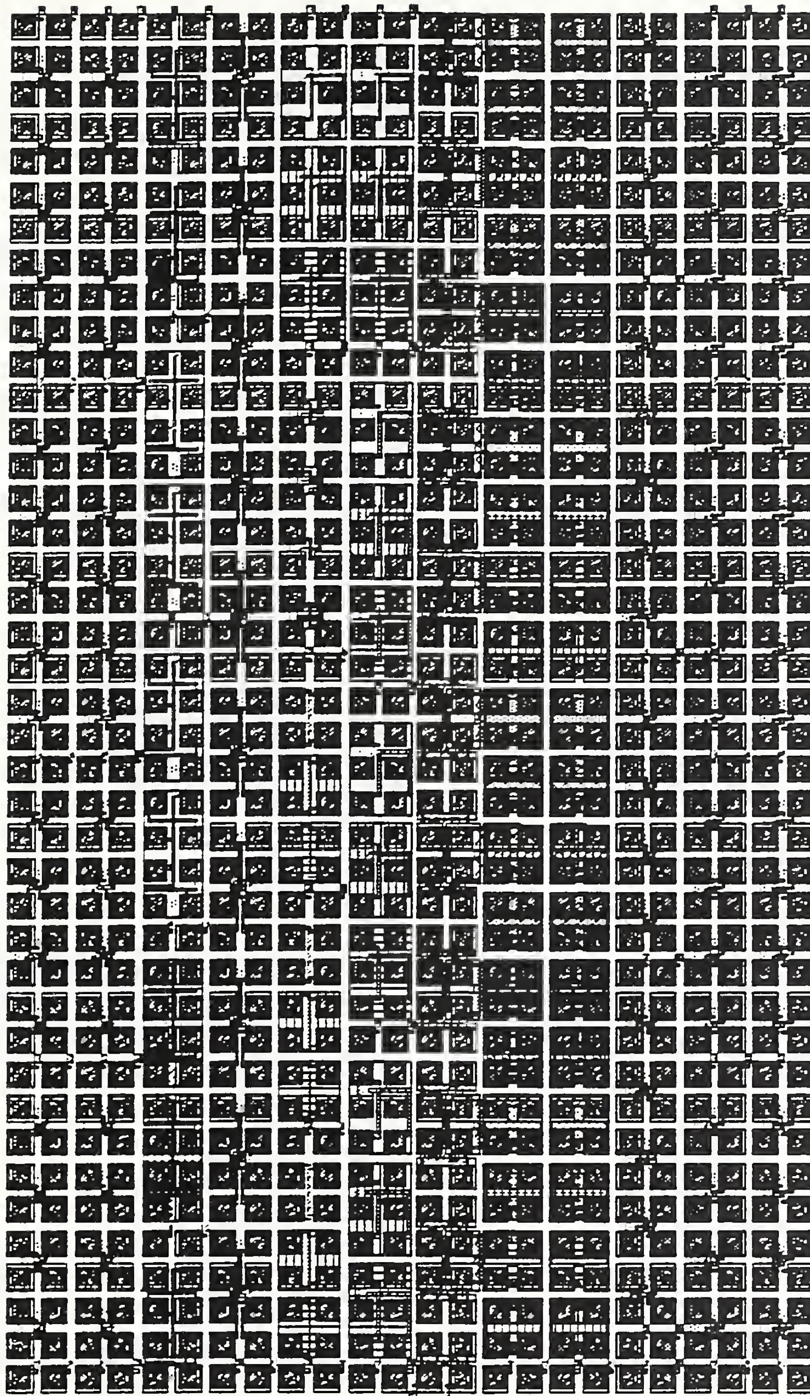


Figure 3. Part-I structures in columns 1 to 12 consist of elemental active devices, inverters, and dc parametric test structures to be probed with a 2 by 10 probe card.

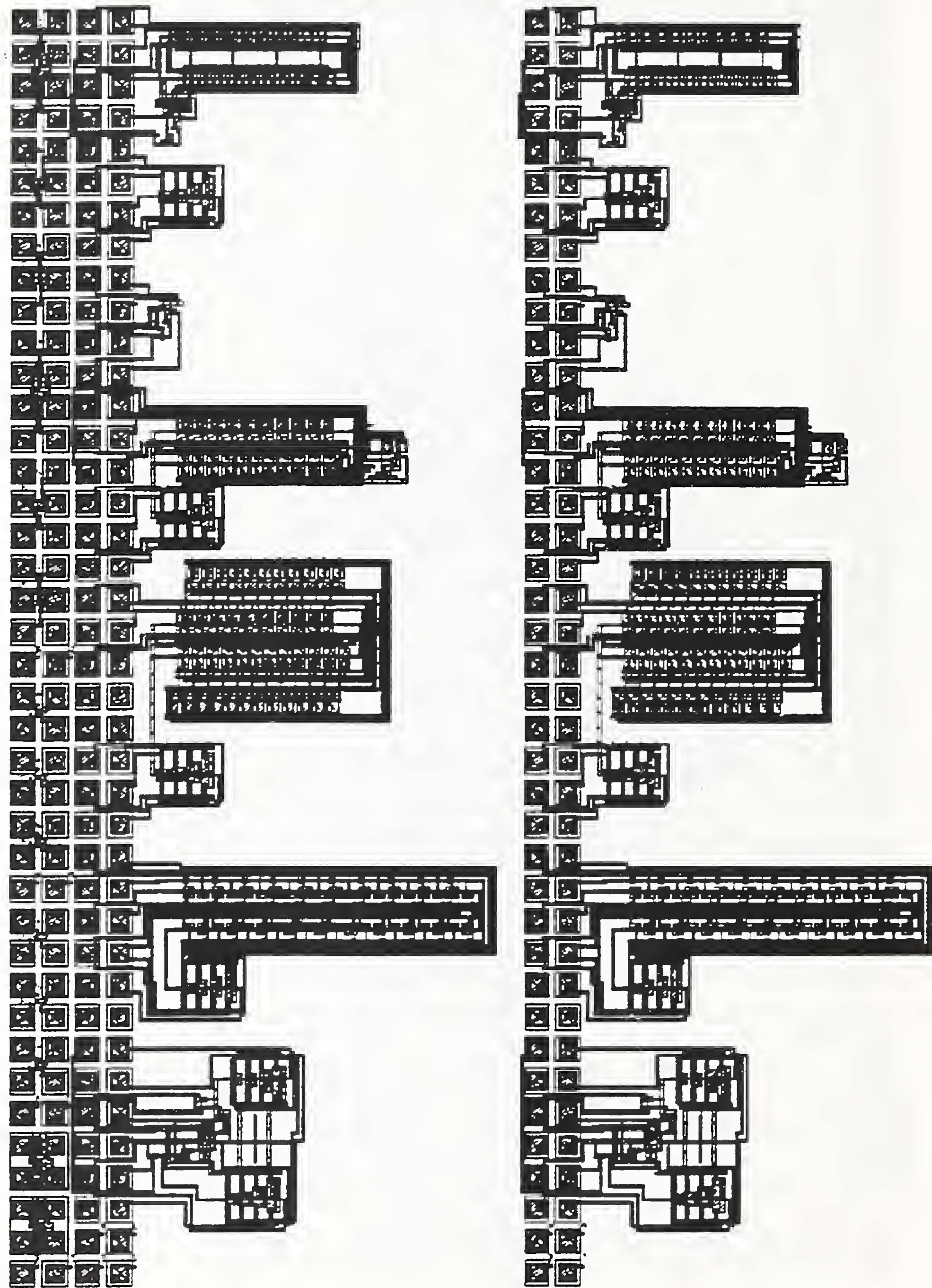


Figure 4. Part-II structures in columns 13 to 15 consist of circuits and their elemental parts.

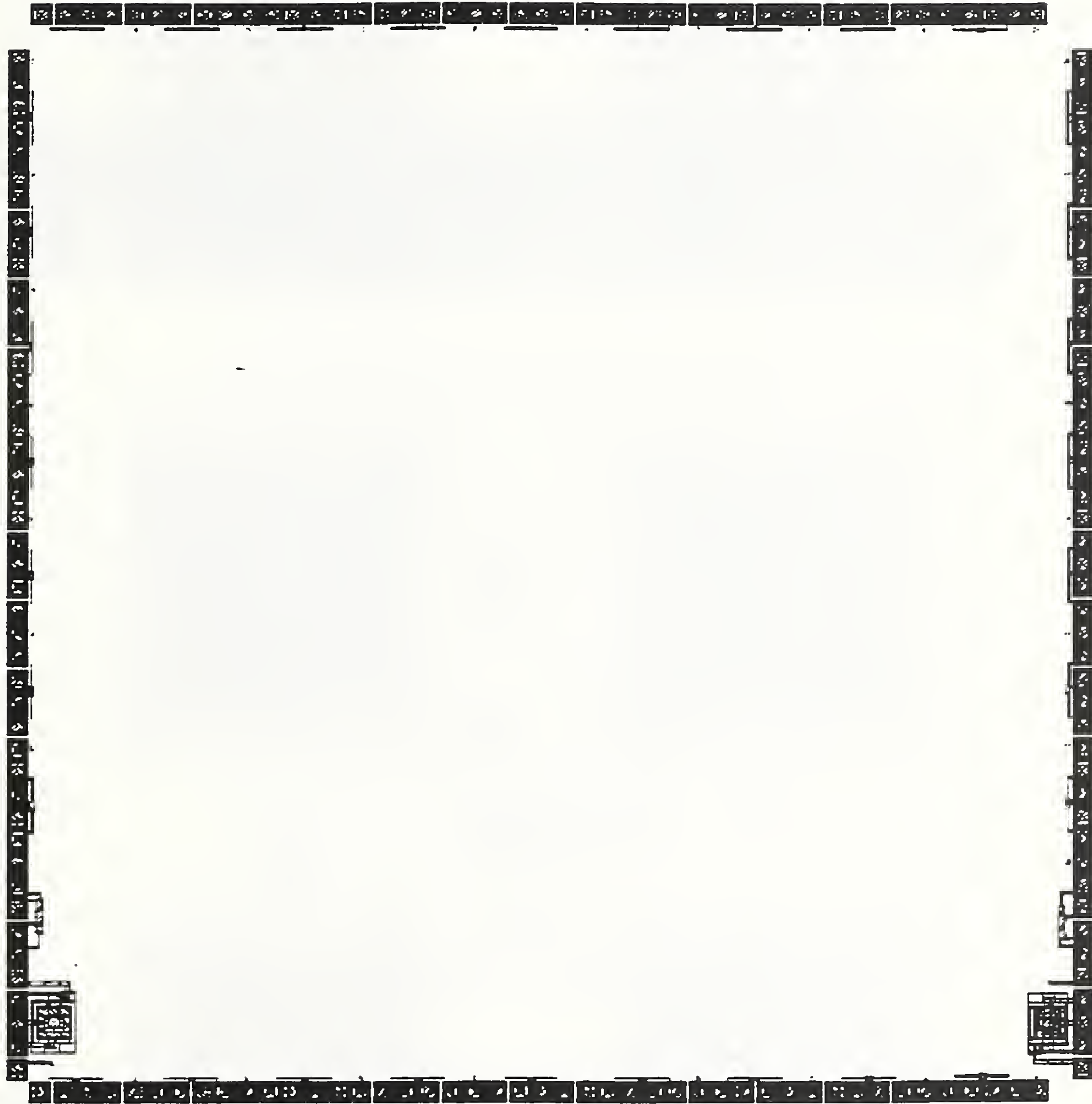
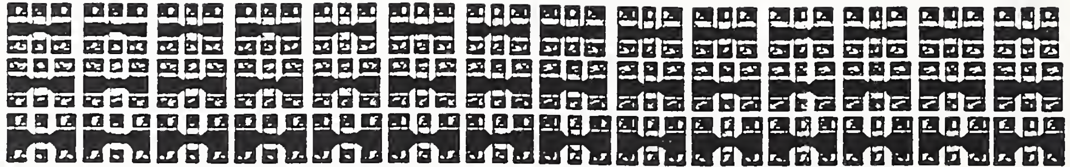


Figure 5. Part-III structures include transistors connected to bondable pads for radiation studies.



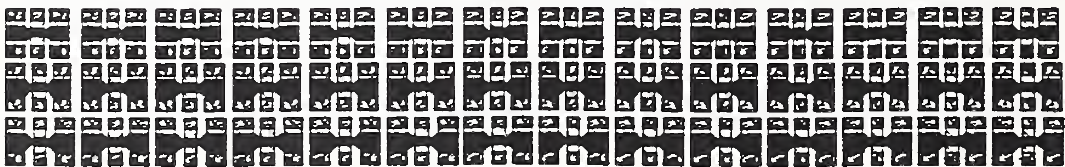


Figure 6. Part-IV structures include transistors padded out to be compatible with rf probe cards for on-wafer rf testing.

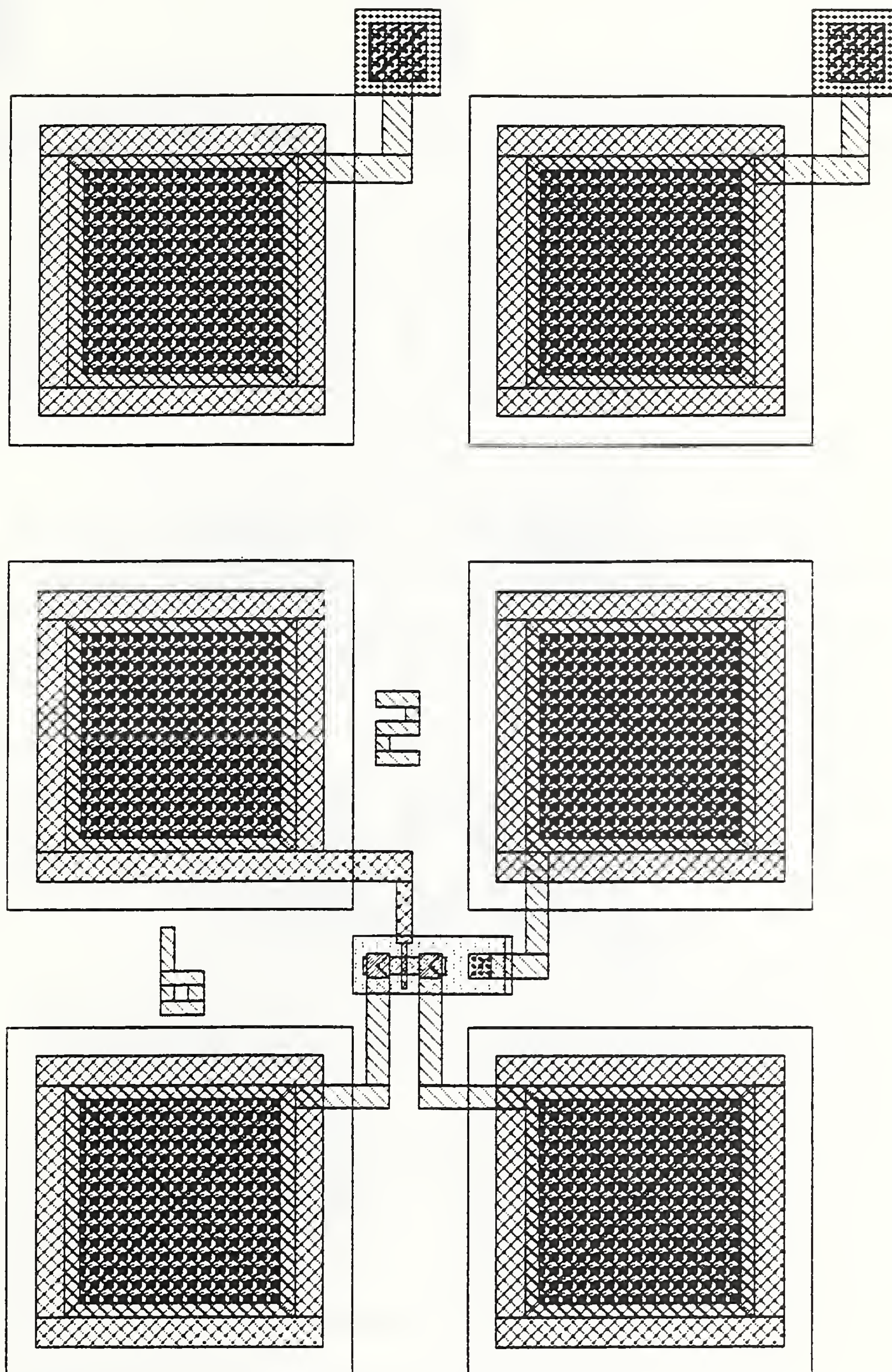


Figure 7. *N*-channel polysilicon gate MOSFET with channel contact beside the drain.

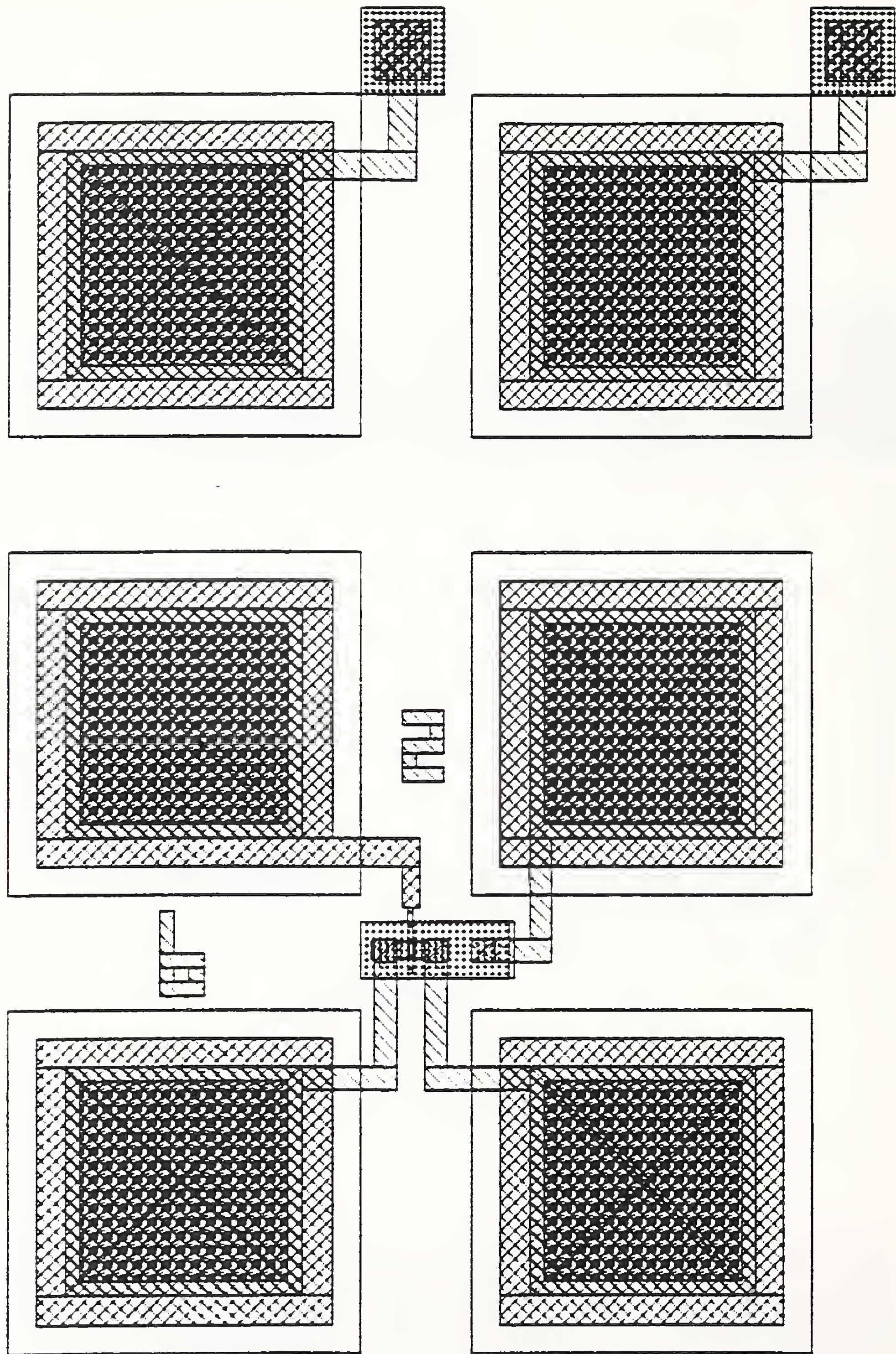


Figure 8. *P*-channel polysilicon gate MOSFET with channel contact beside the drain.

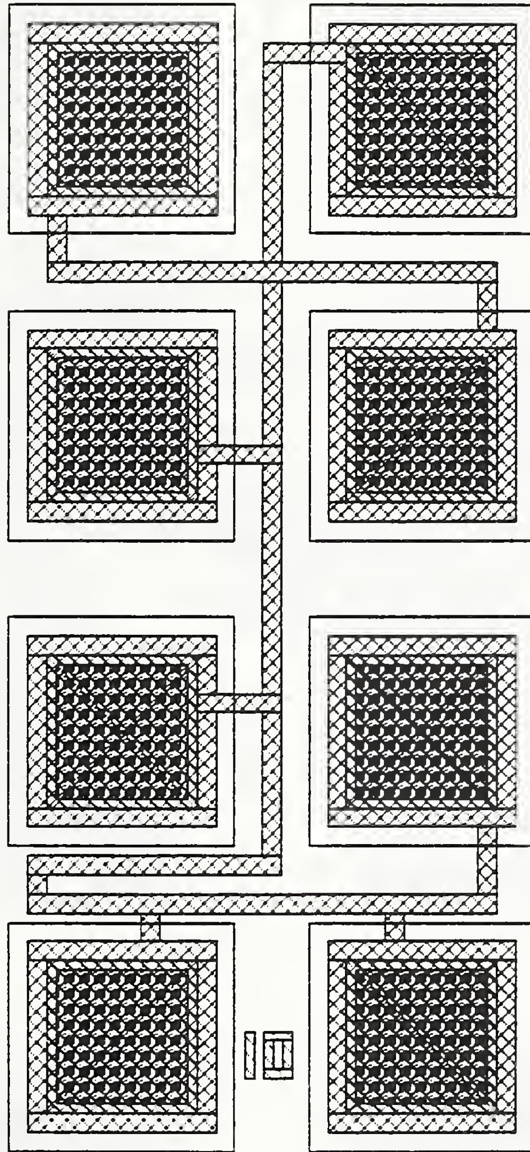


Figure 9. Polysilicon cross-bridge resistor.

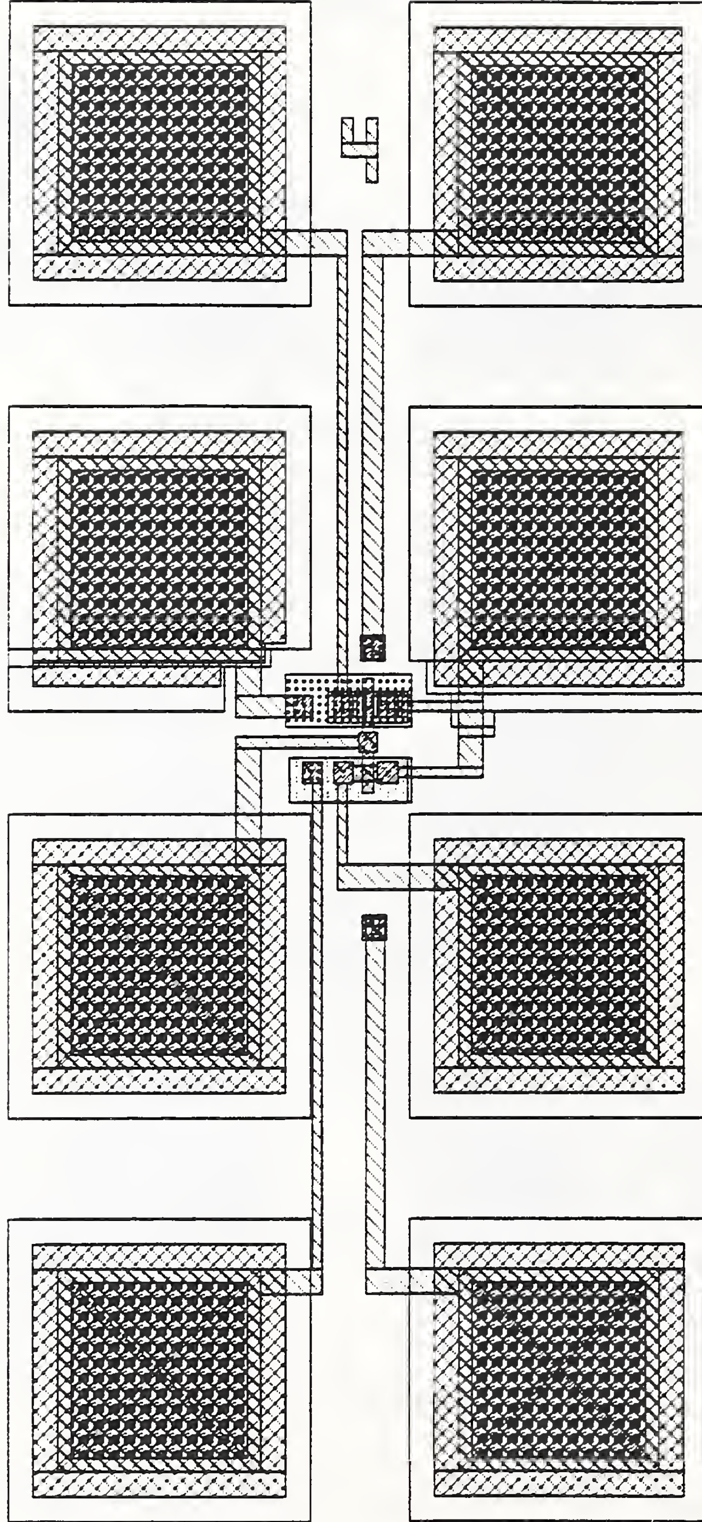


Figure 10. Inverter using L=4 μm.

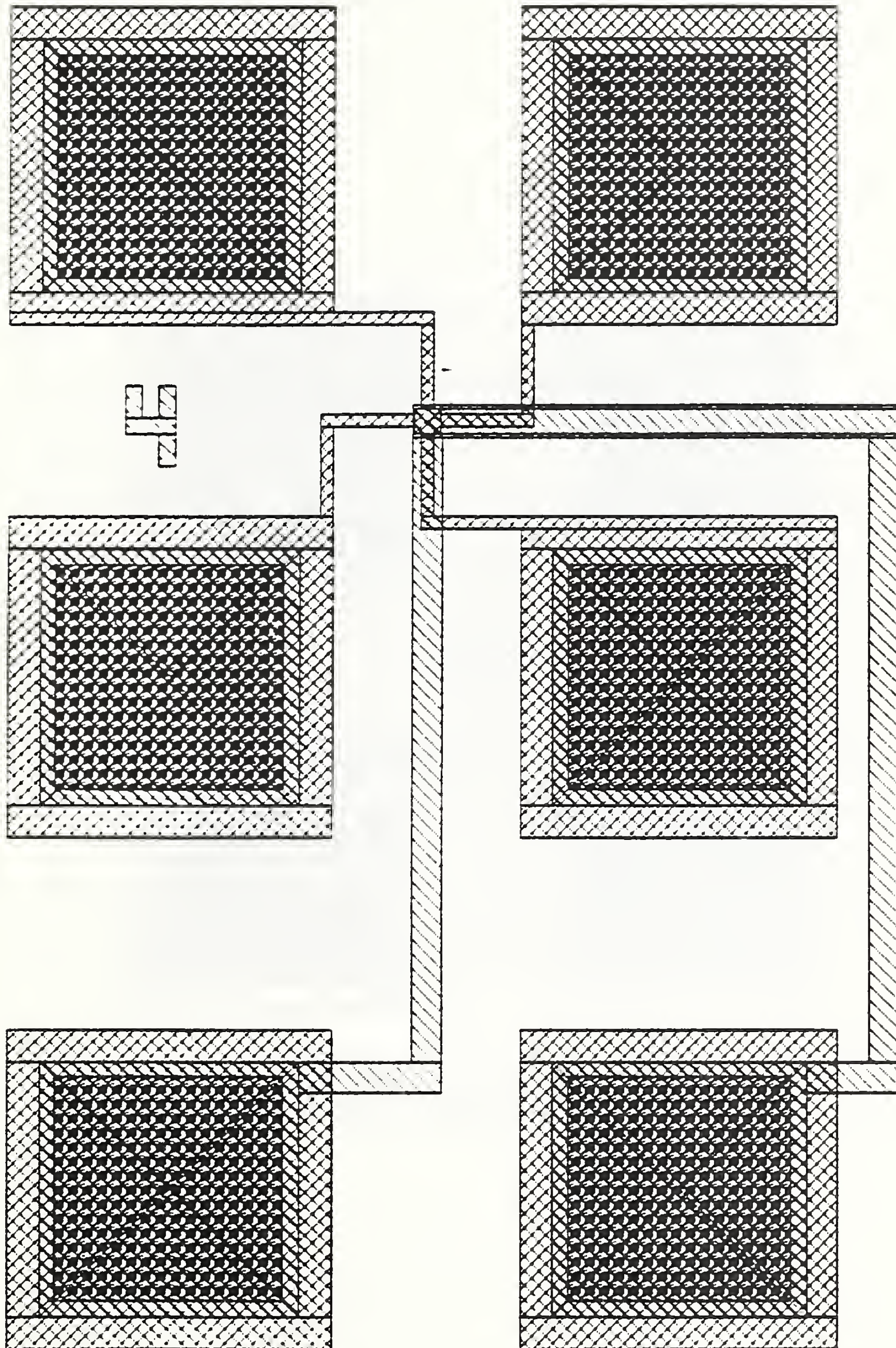


Figure 11. Six-pad contact resistance test structure.

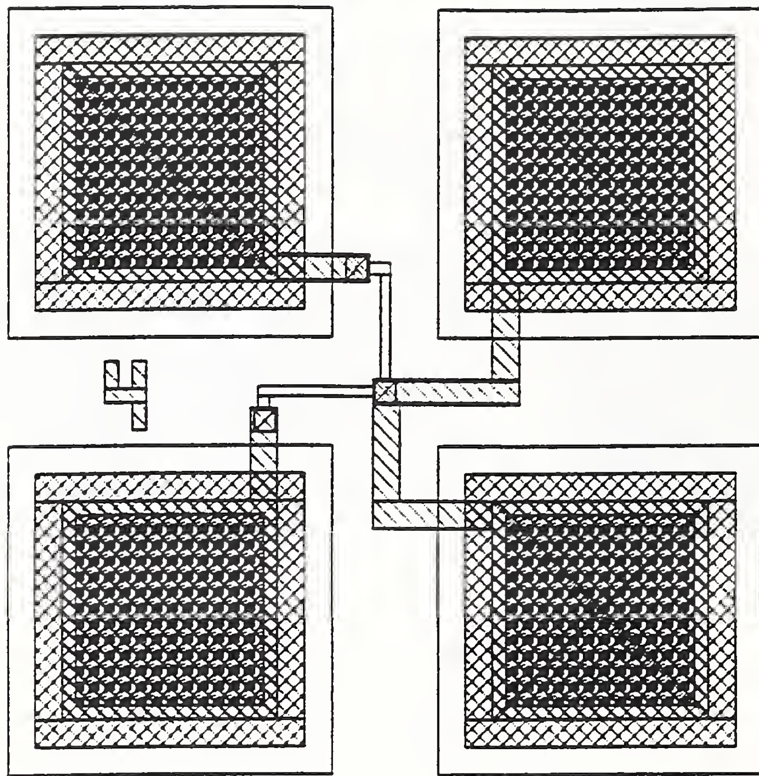


Figure 12. Four-pad contact resistance test structure.

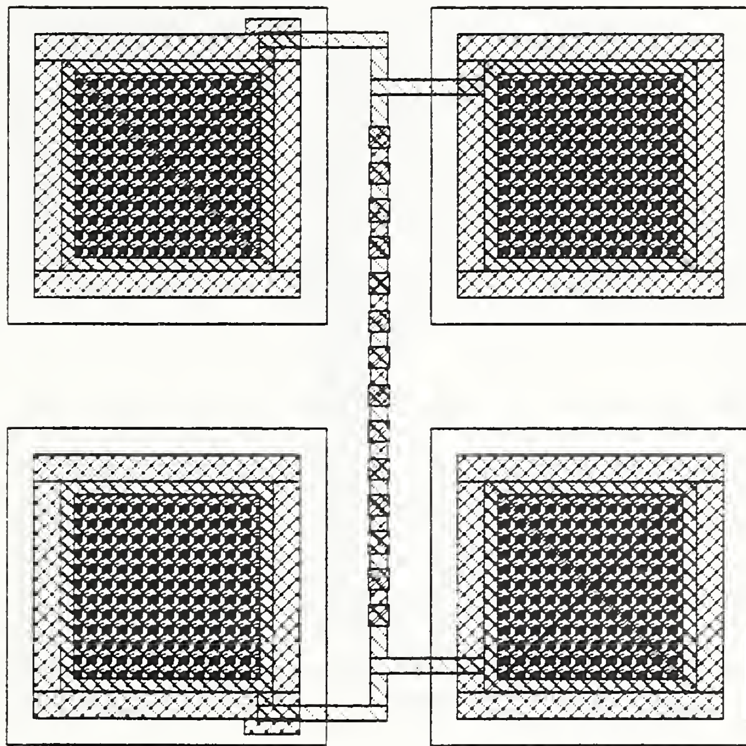


Figure 13. Kelvin chain of 14 contacts.

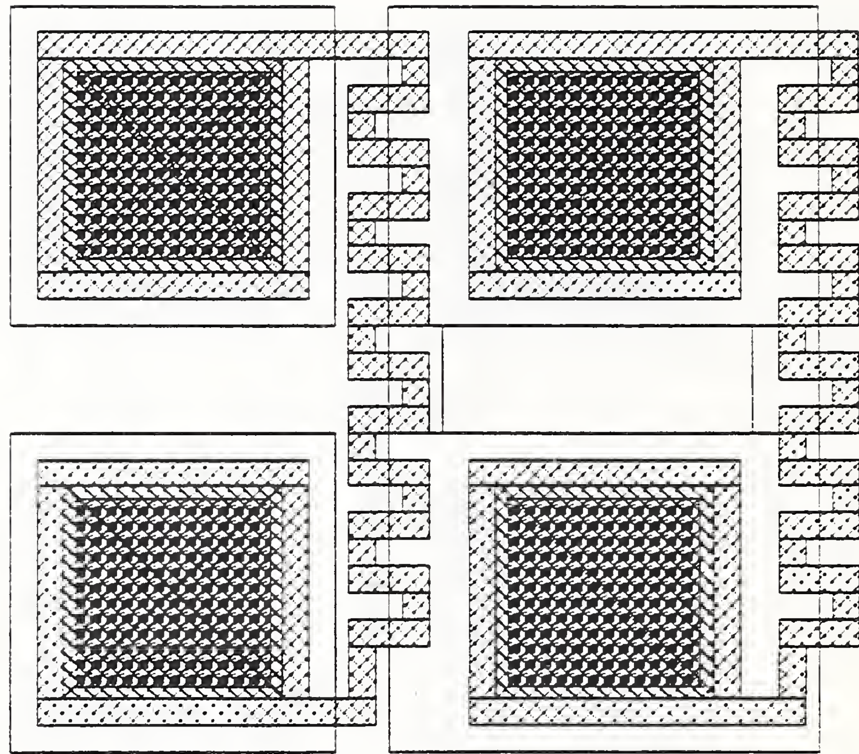


Figure 14. Polysilicon-over-island meander structure.

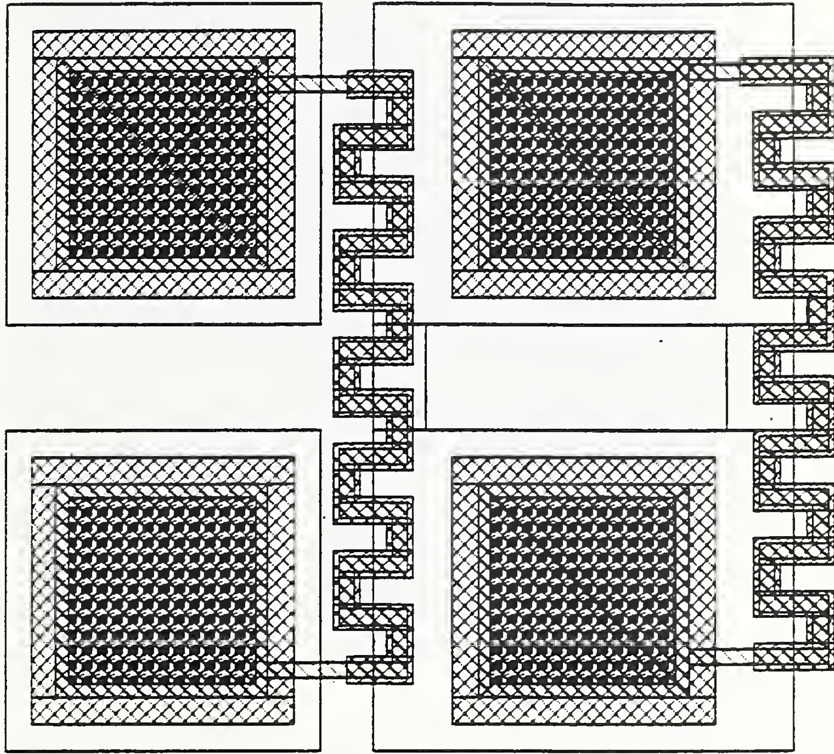


Figure 15. Metal-atop-polysilicon-over-island meander structure.

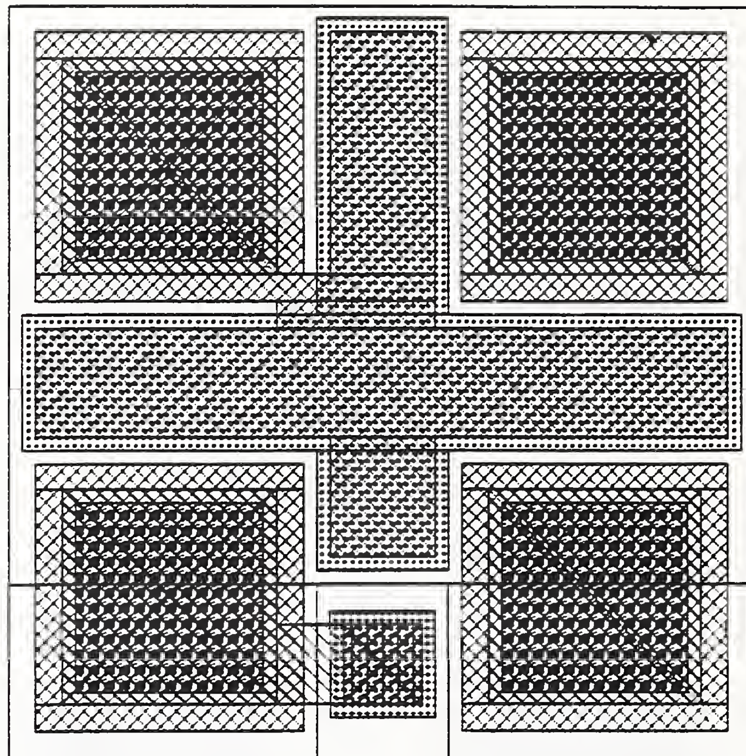


Figure 16. Polysilicon-over-nwell-to-substrate capacitor.

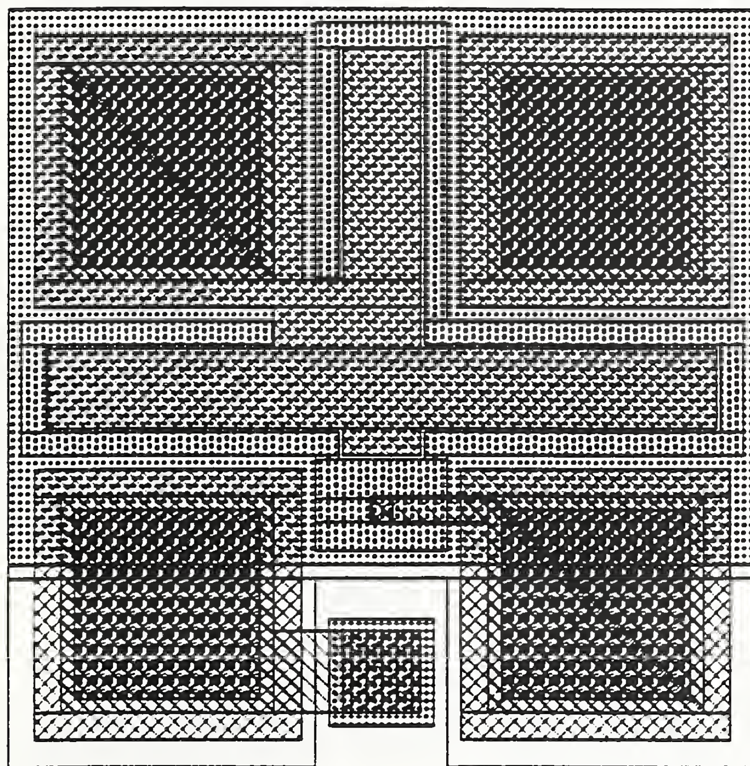


Figure 17. Polysilicon-over-nwell to nearby nndiff in same nwell-to-substrate capacitor.

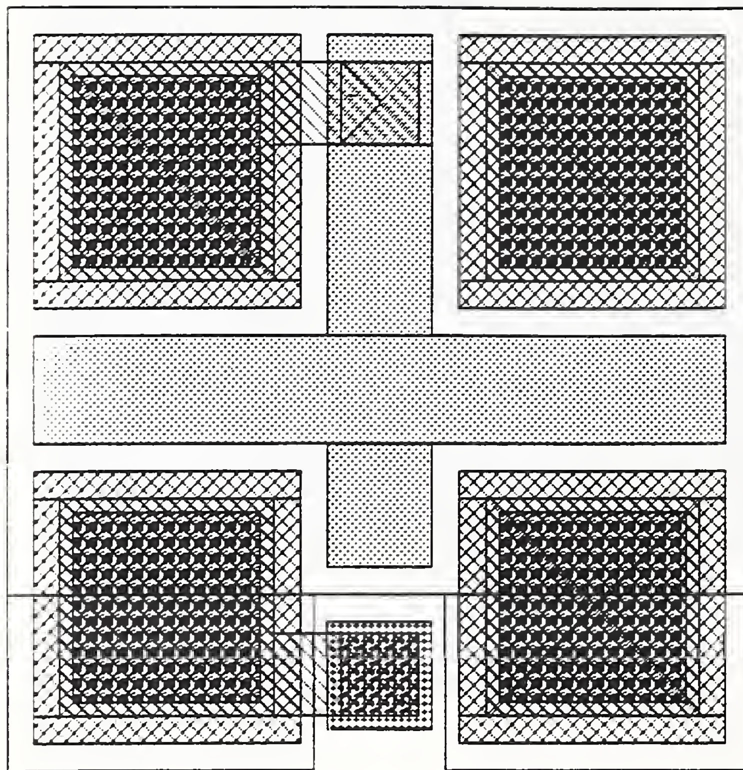


Figure 18. Ndiffusion-to-substrate capacitor.

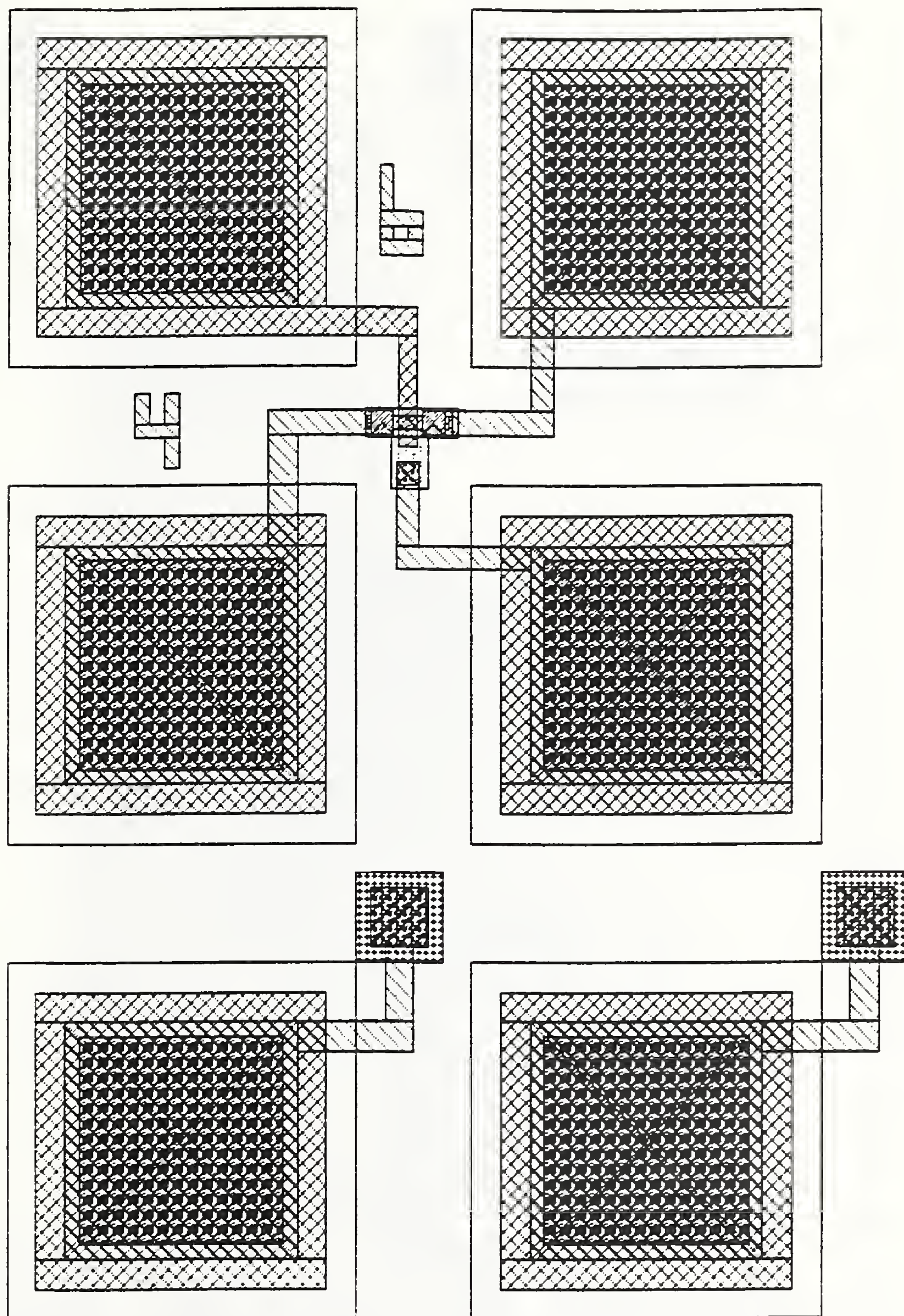


Figure 19. *N*-channel polysilicon gate MOSFET with channel contact near the channel.

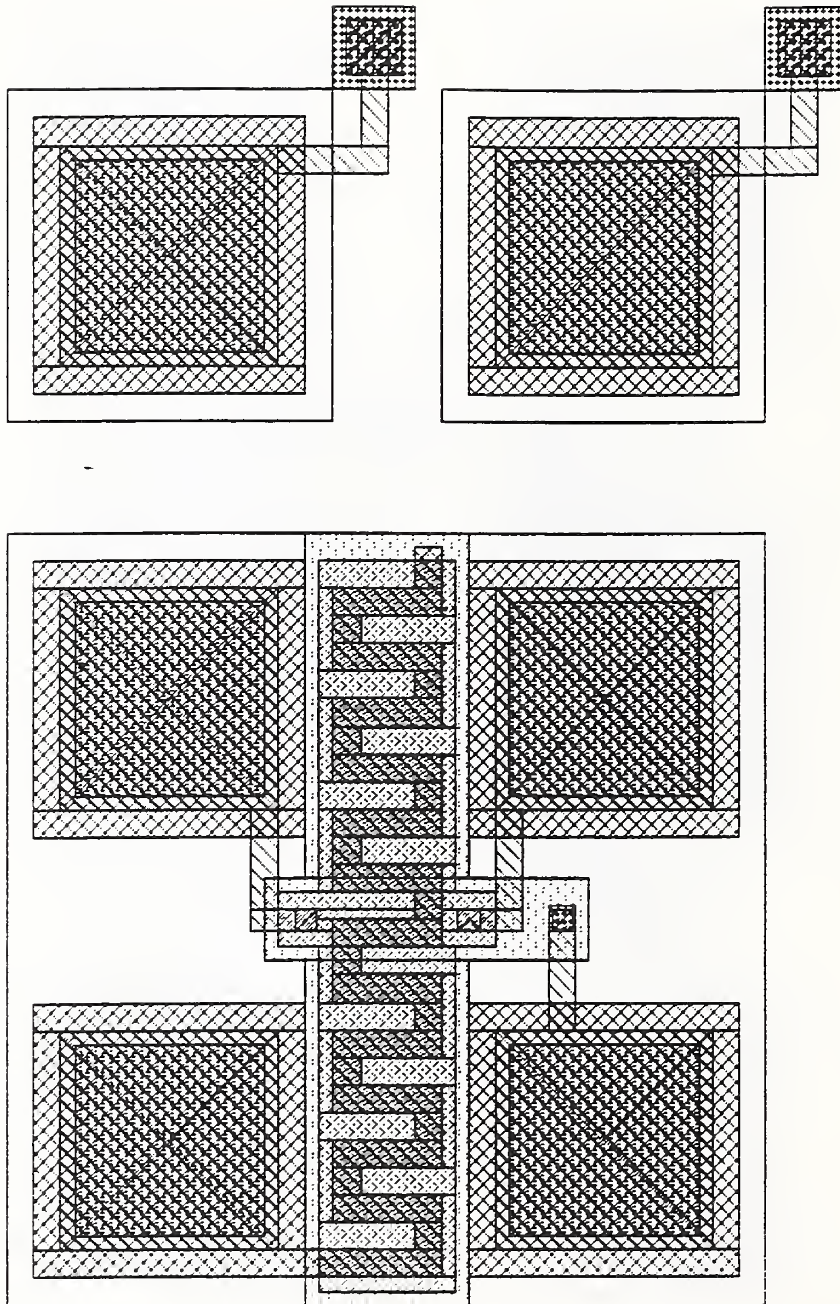


Figure 20. *N*-channel MOSFET with snake-like gate with 25 corners.

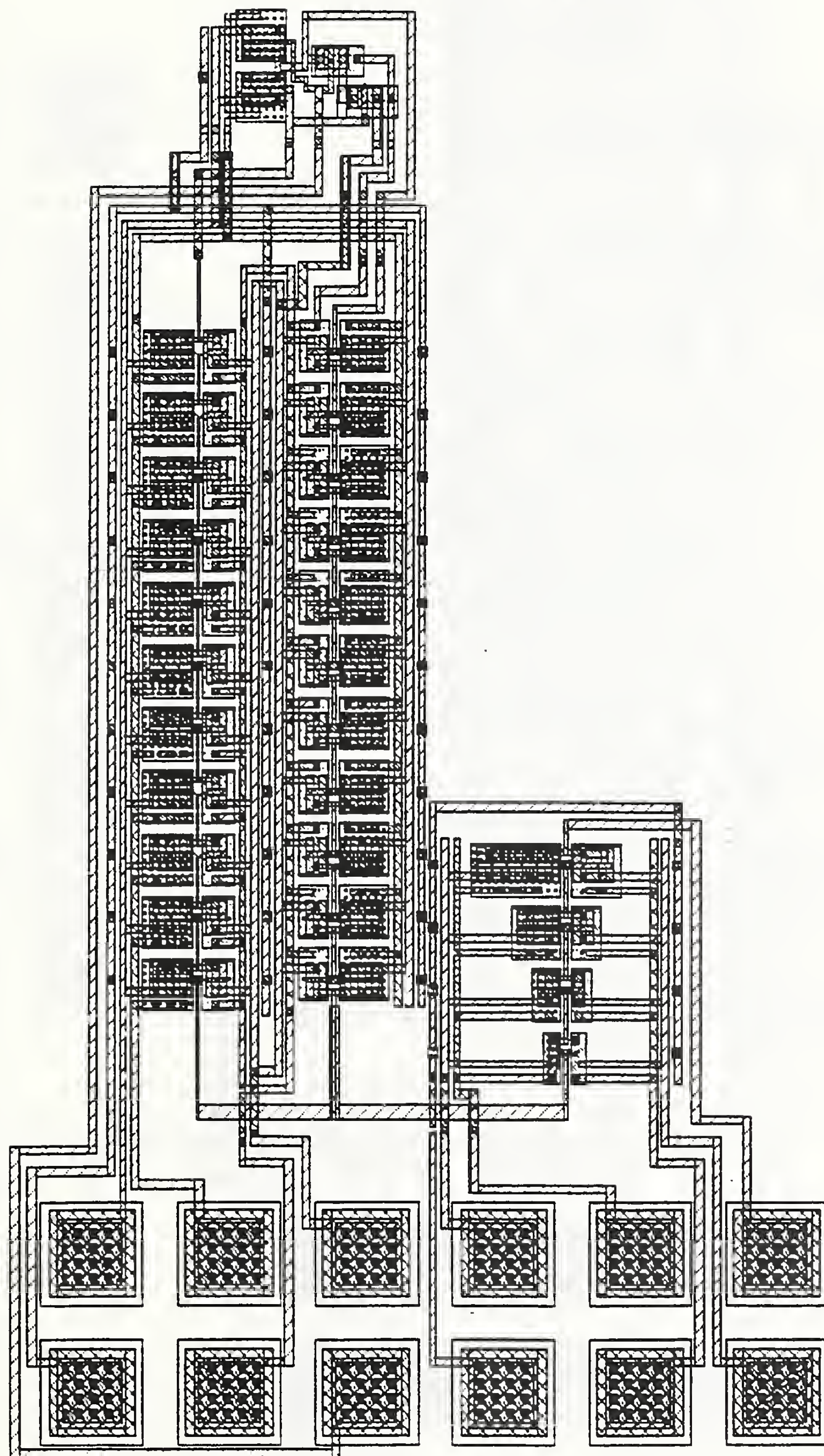


Figure 21. Twenty-three-stage ring oscillator with NAND gate startup and four-stage output amplifier.

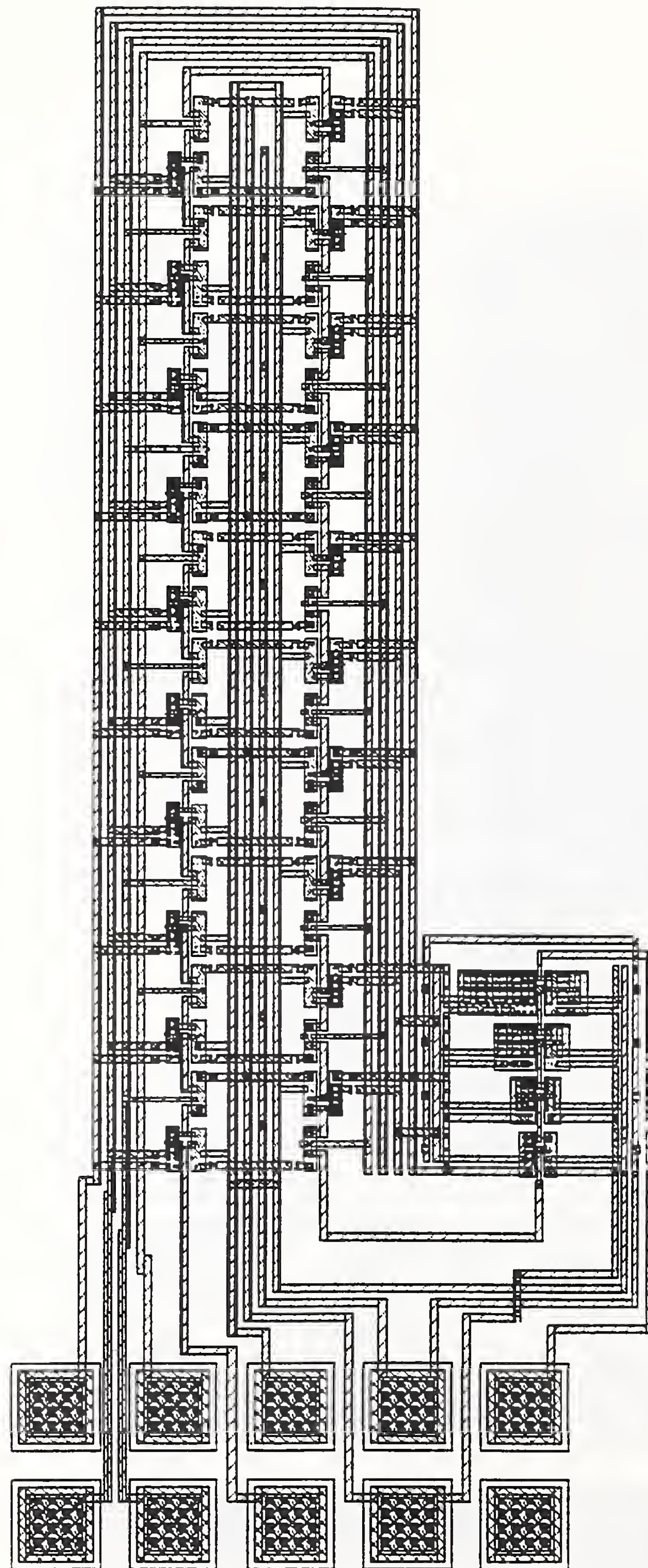


Figure 22. Twenty-stage shift register with two clocks and an output amplifier.

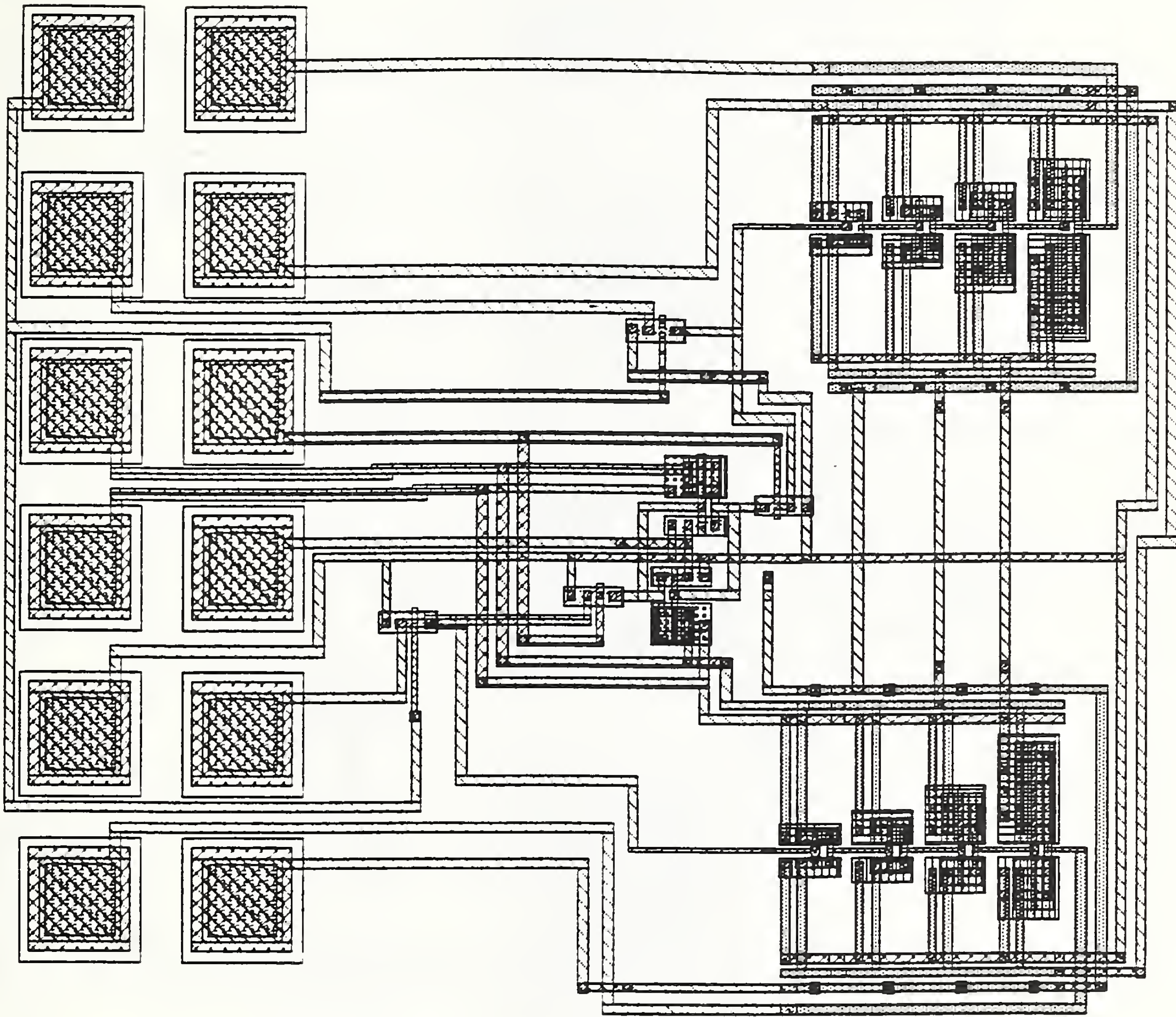


Figure 23. Six-transistor static RAM cell with two four-stage output amplifiers.

UNSELECTED: LATCH = 0
RWSEL = 0
WSEL = 0

TO WRITE: LATCH = 1
RWSEL = 1
WSEL = 1
BIT = data to be written
$\overline{\text{BIT}}$ = $\overline{\text{data to be written}}$

THEN: LATCH = 0
RWSEL = 0
WSEL = 0

TO READ: RWSEL = 1
WSEL = 0
LATCH = 0
DATA = data in cell
$\overline{\text{DATA}}$ = $\overline{\text{data in cell}}$
THEN: RWSEL = 0

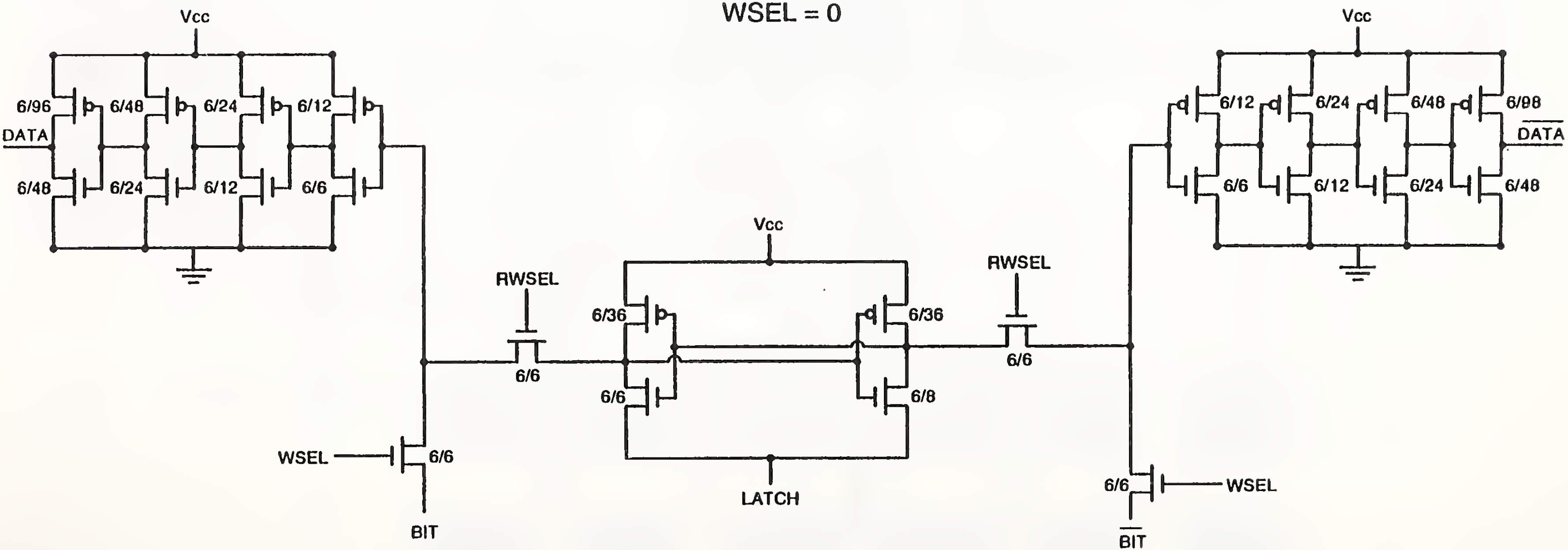


Figure 24. Circuit diagram of the static RAM cell (and how to test it).

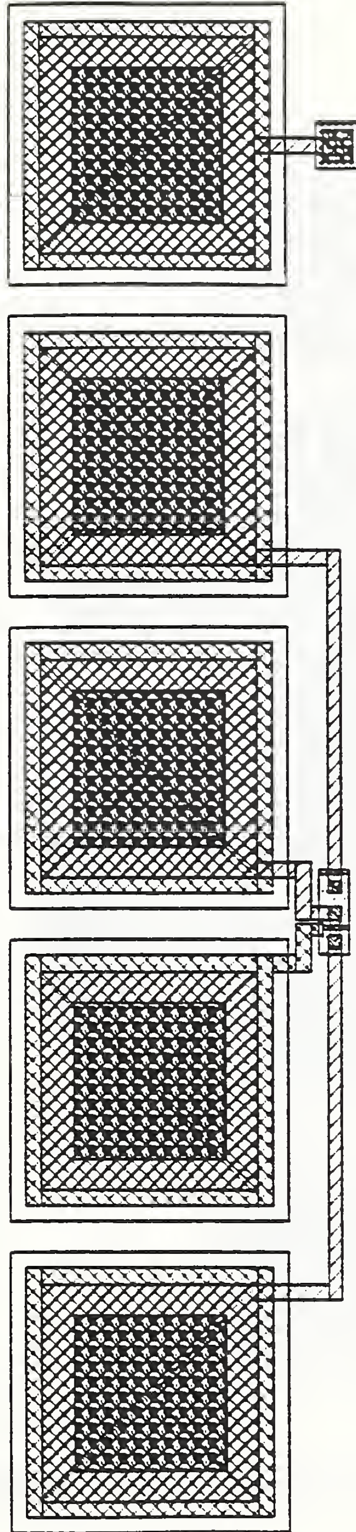


Figure 25. Bonded *n*-channel MOSFET.

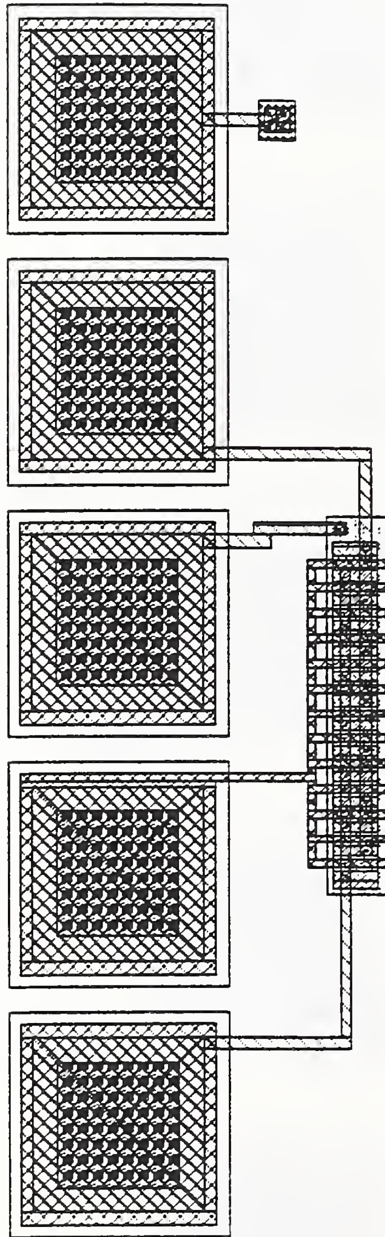


Figure 26. Bonded MOSFET with a comb-shaped gate with 13 teeth.

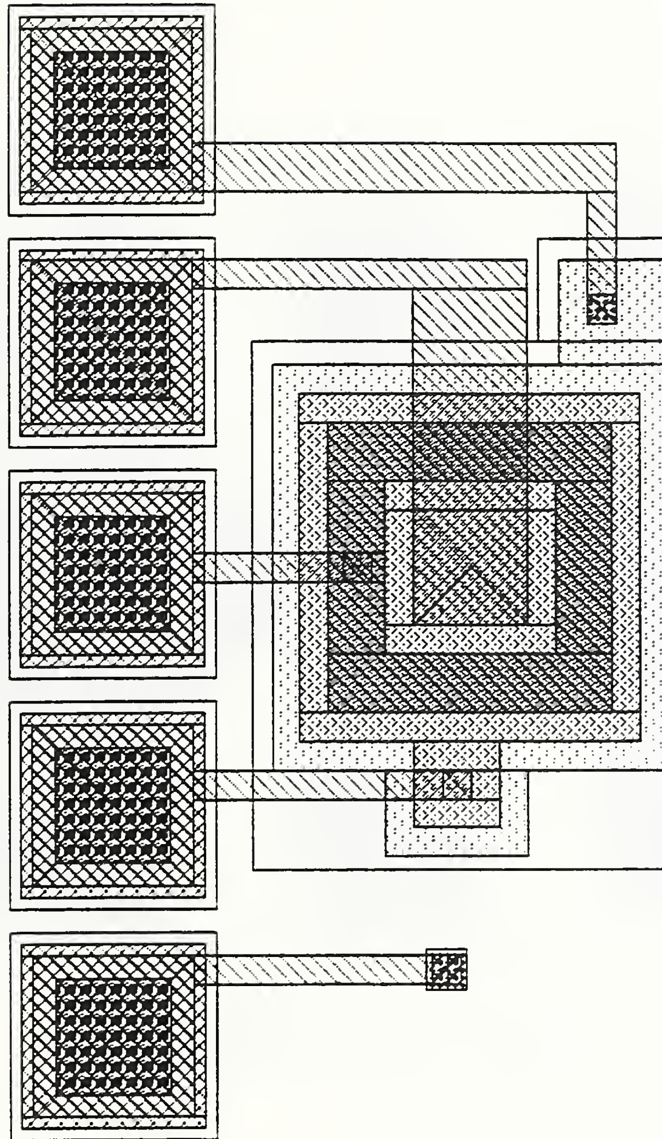


Figure 27. Bonded closed-geometry MOSFET.

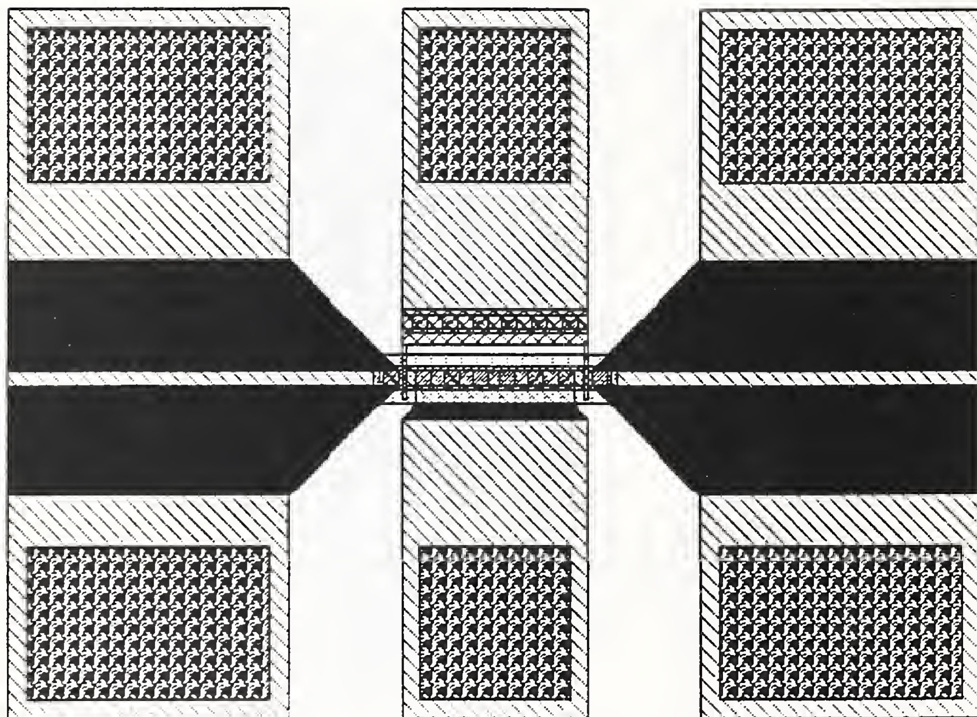


Figure 28. *N*-channel rf transistor.

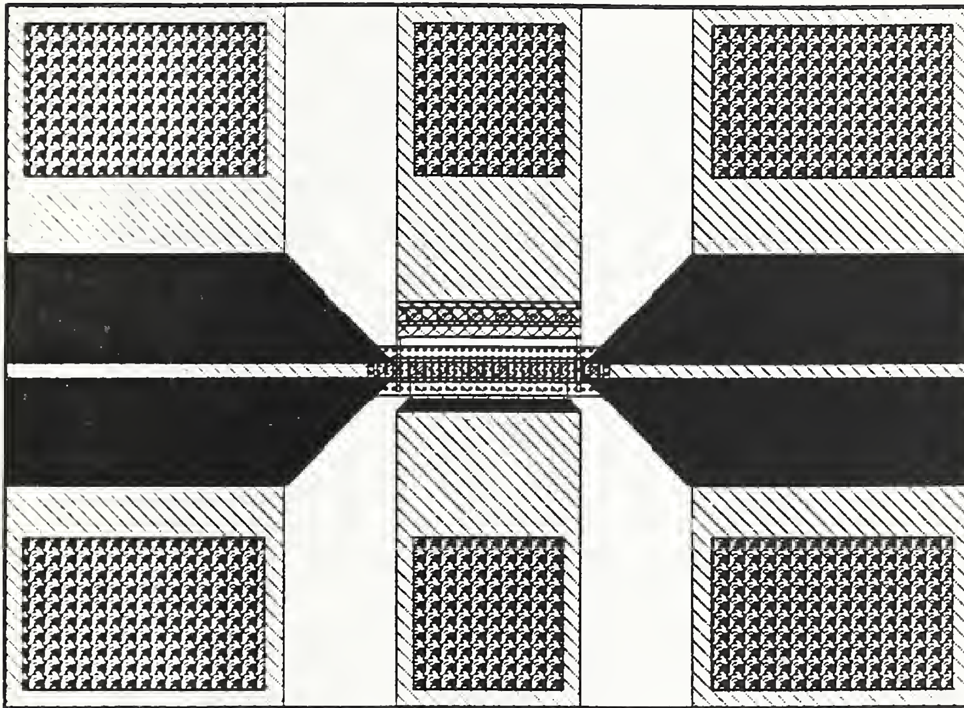


Figure 29. *P*-channel rf transistor.

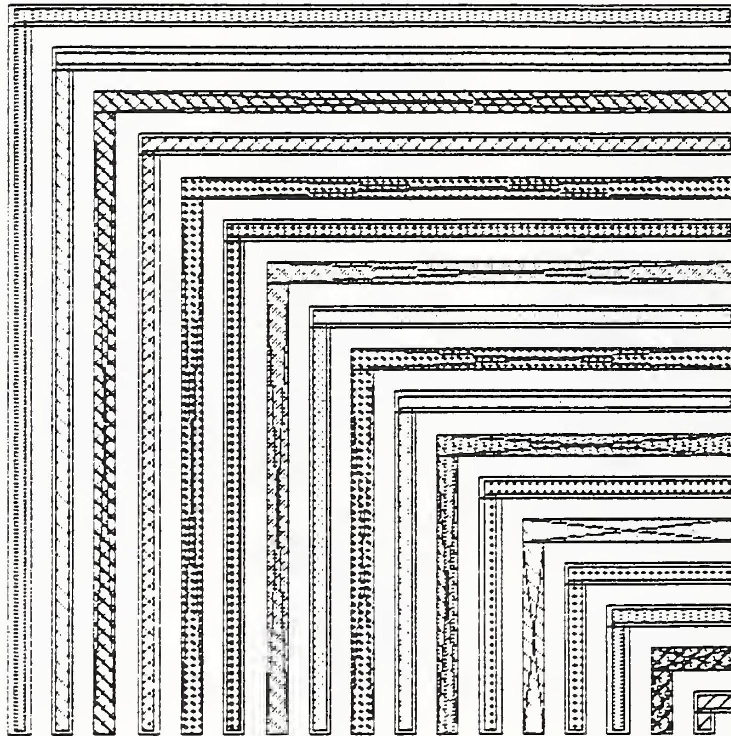


Figure 30. Alignment marks to be used with a clear field mask.

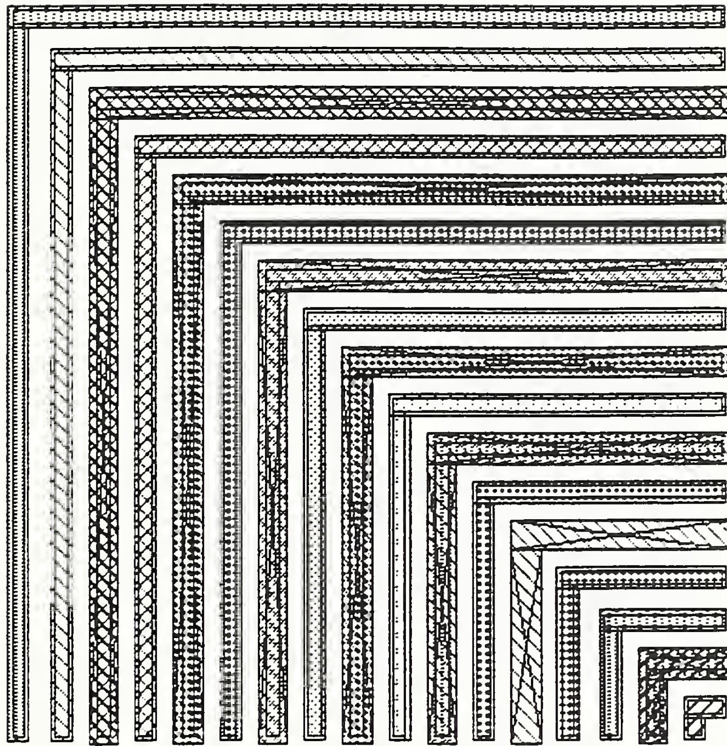


Figure 31. Alignment marks to be used with a dark field mask.

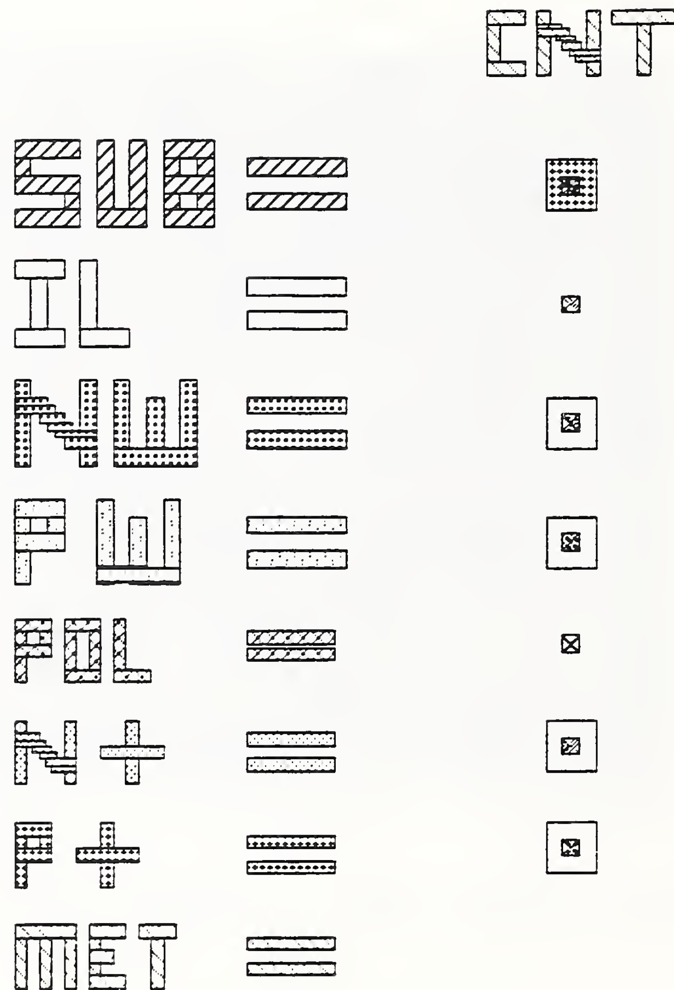


Figure 32. Level identifier.

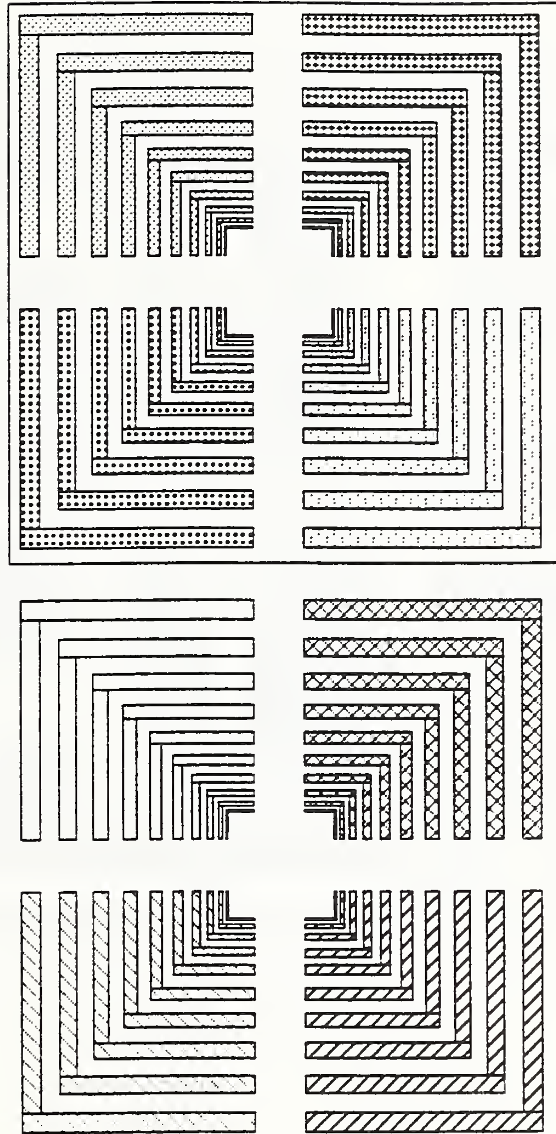


Figure 33. Chevrons.

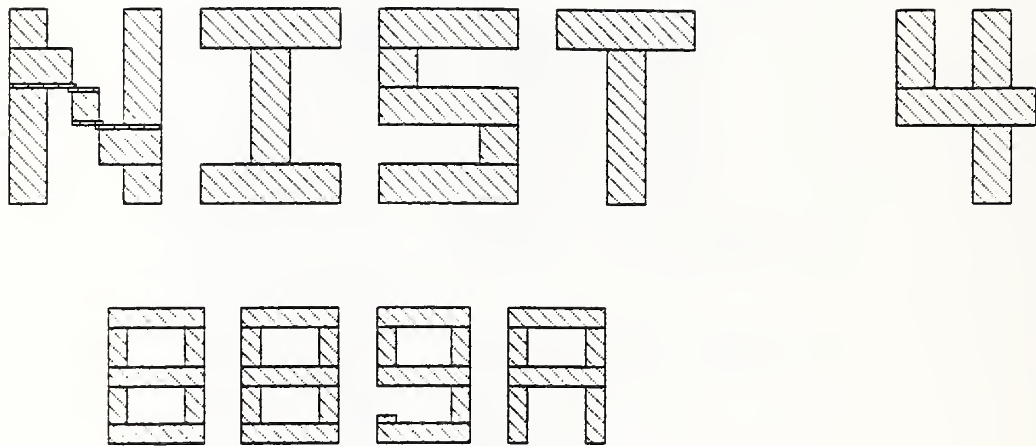


Figure 34. NIST4 identifier.

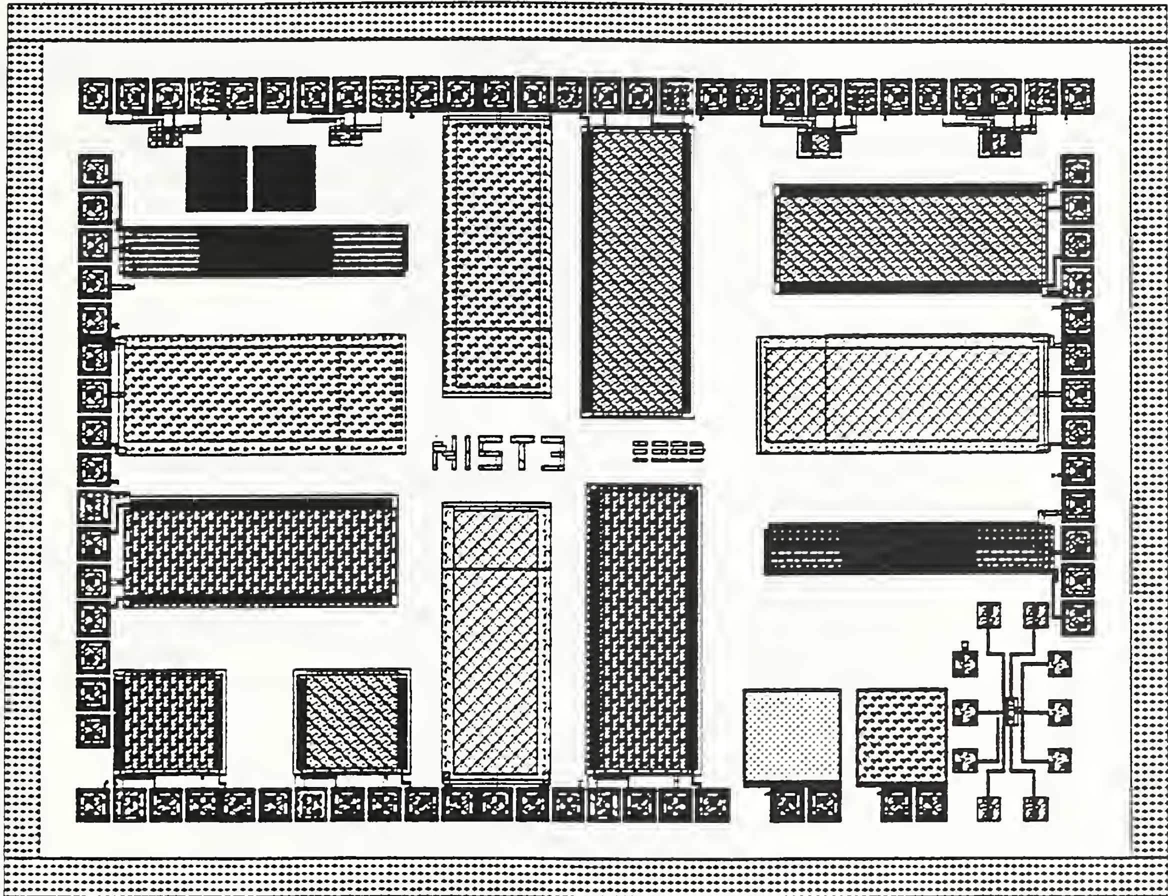


Figure 35. SIMOX Test Chip NIST3.

Figure 36. Cell structure of NIST3.

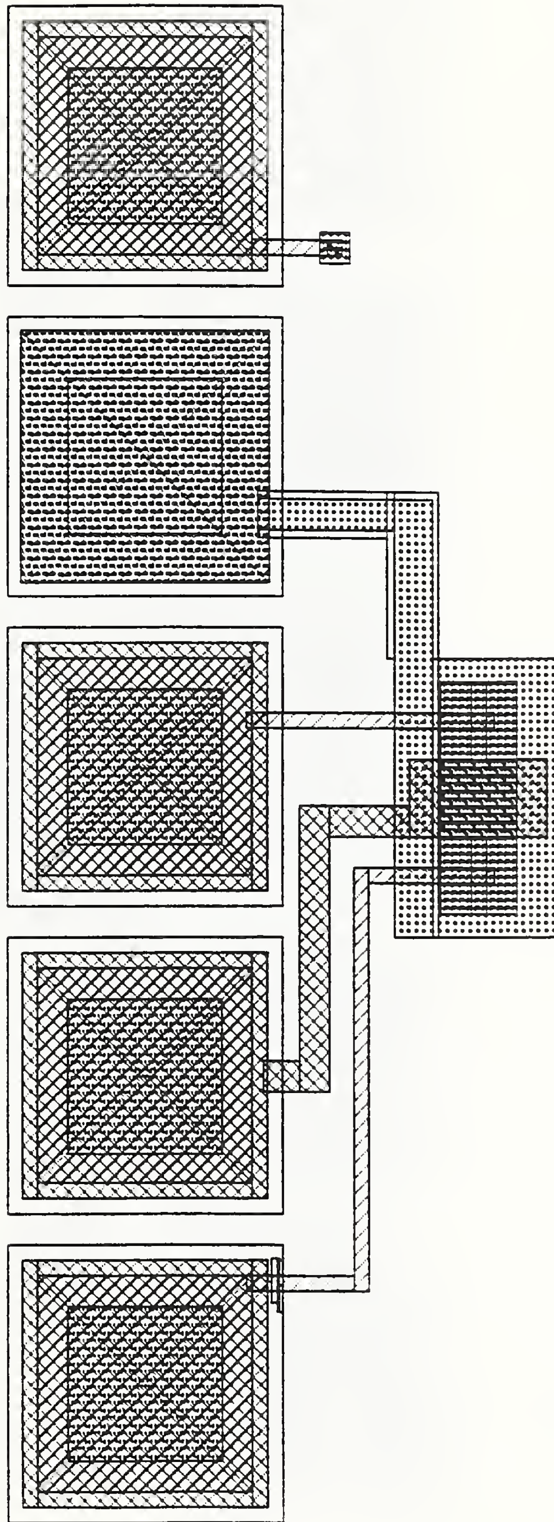


Figure 37. *P*-channel polysilicon gate MOSFET (L=50 μm, W=50 μm).

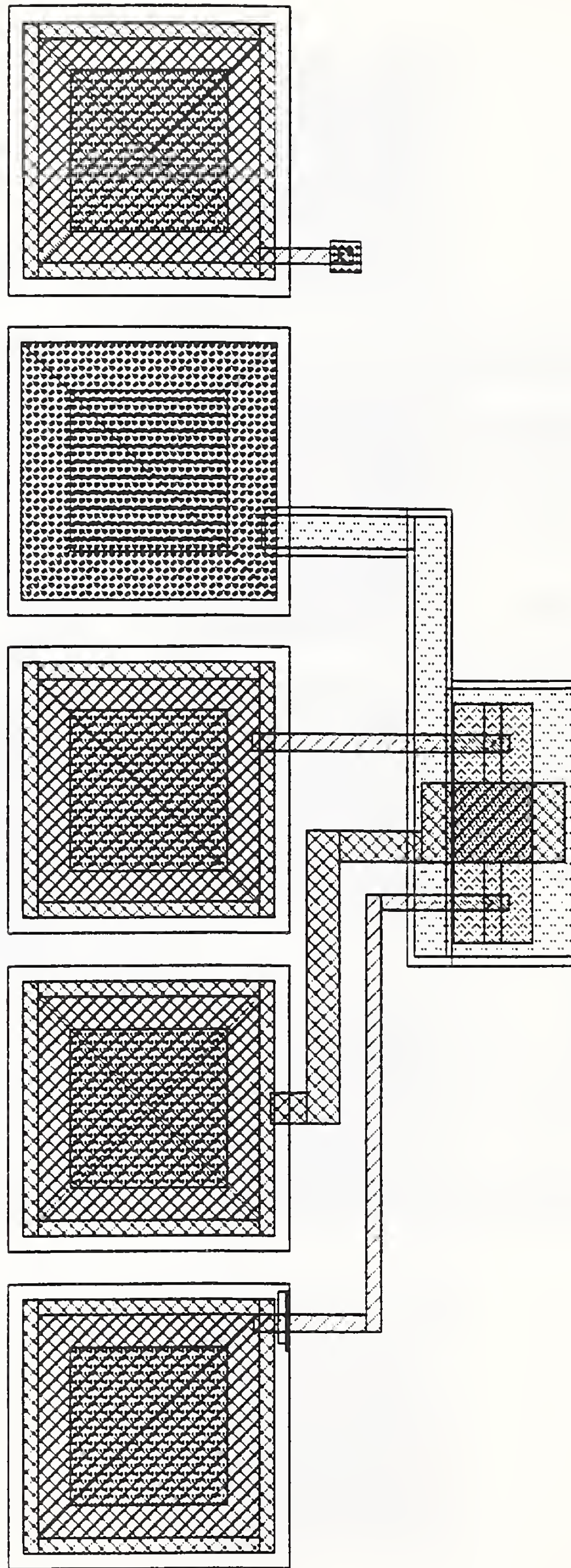


Figure 38. *N*-channel polysilicon gate MOSFET (L=50 μm, W=50 μm).

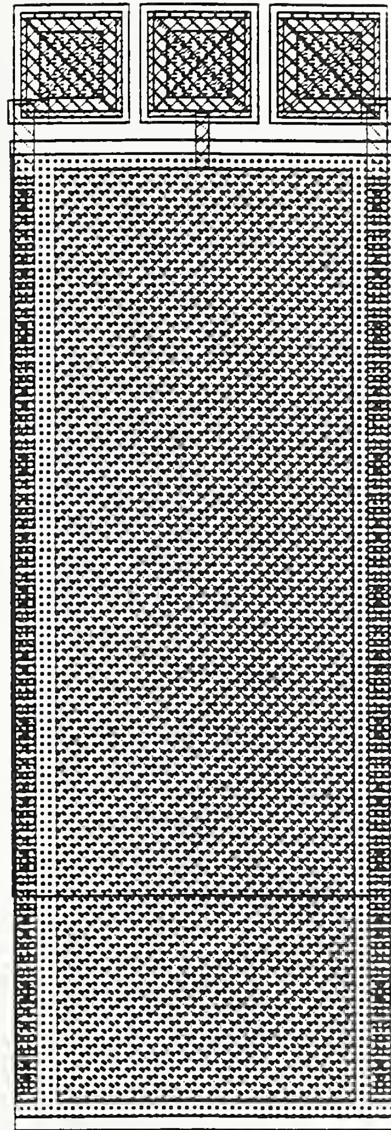


Figure 39. Nwell resistor (Lpoly=460 μm, Wpoly=1410 μm).

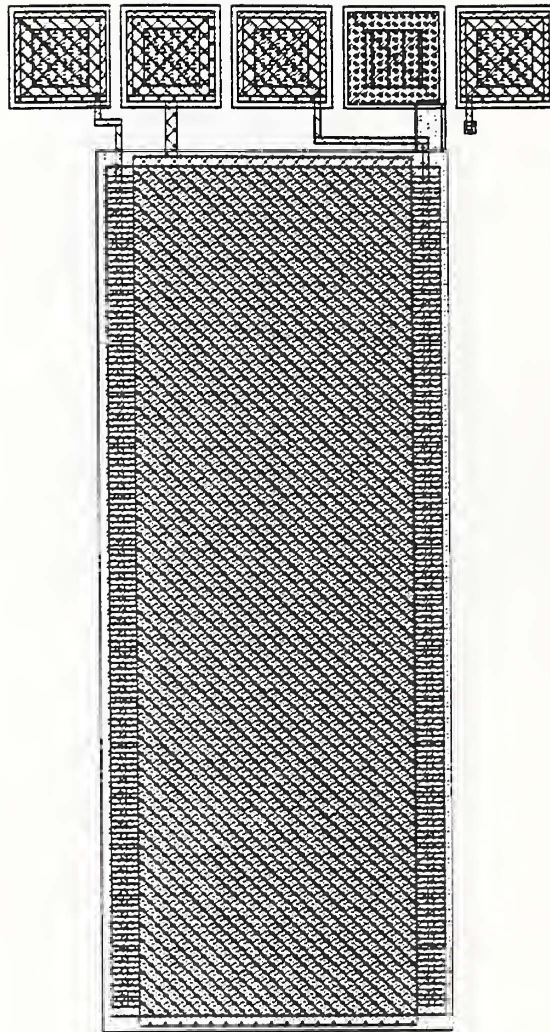


Figure 40. *N*-channel polysilicon gate MOSFET (L=500 μm, W=1500 μm).

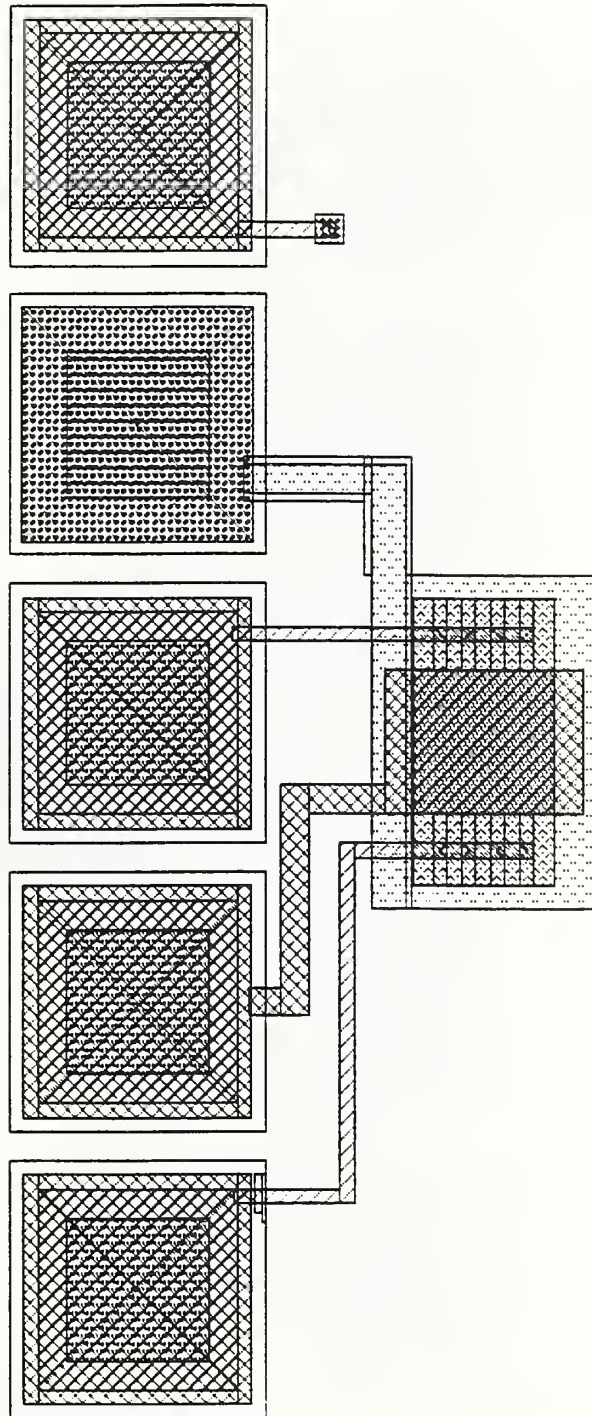


Figure 41. *N*-channel polysilicon gate MOSFET (L=100 μm, W=100 μm).

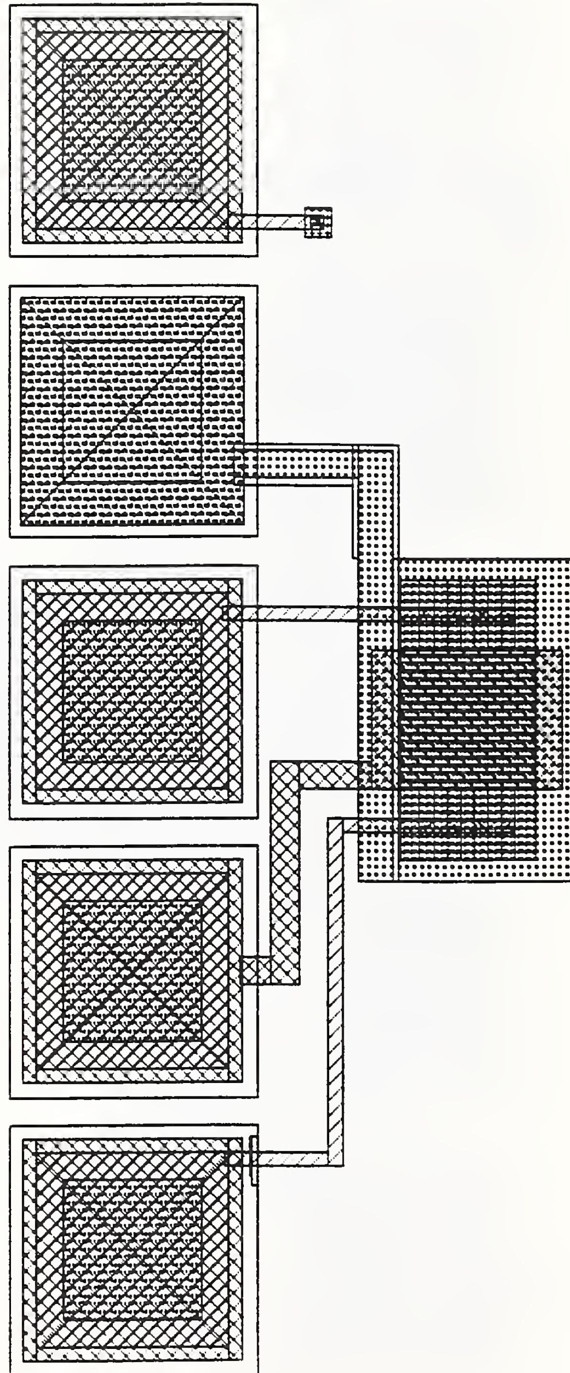


Figure 42. *P*-channel polysilicon gate MOSFET (L=100 μm, W=100 μm).

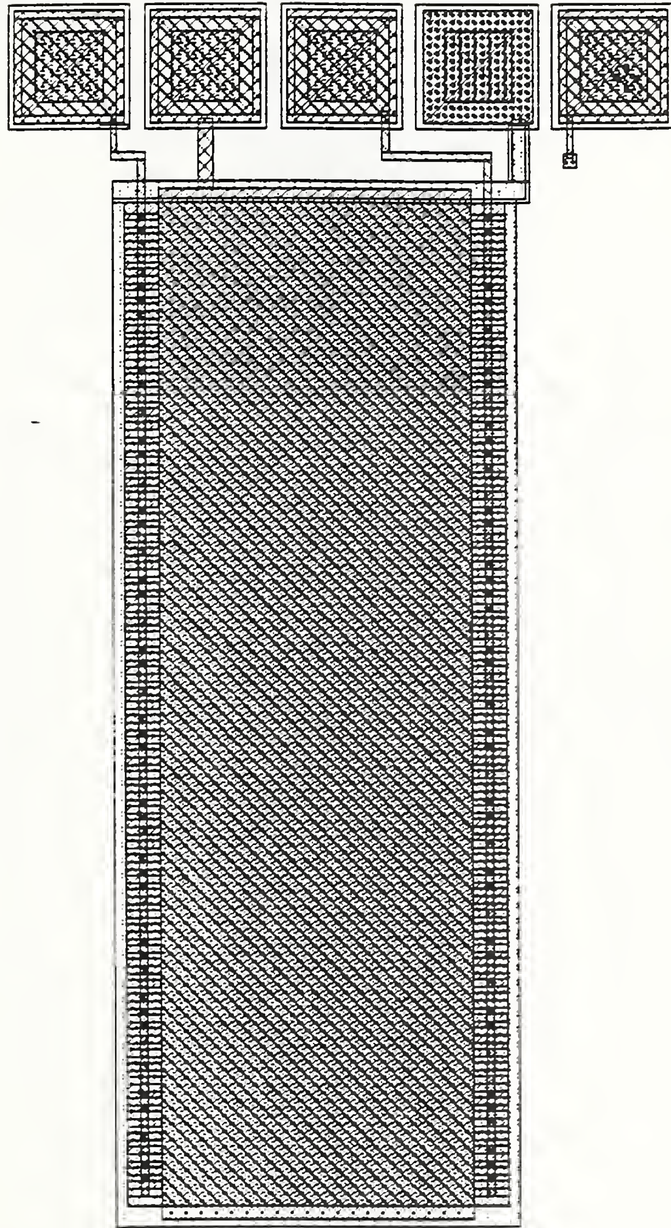


Figure 43. *N*-channel polysilicon gate MOSFET (L=460 μm, W=1440 μm).

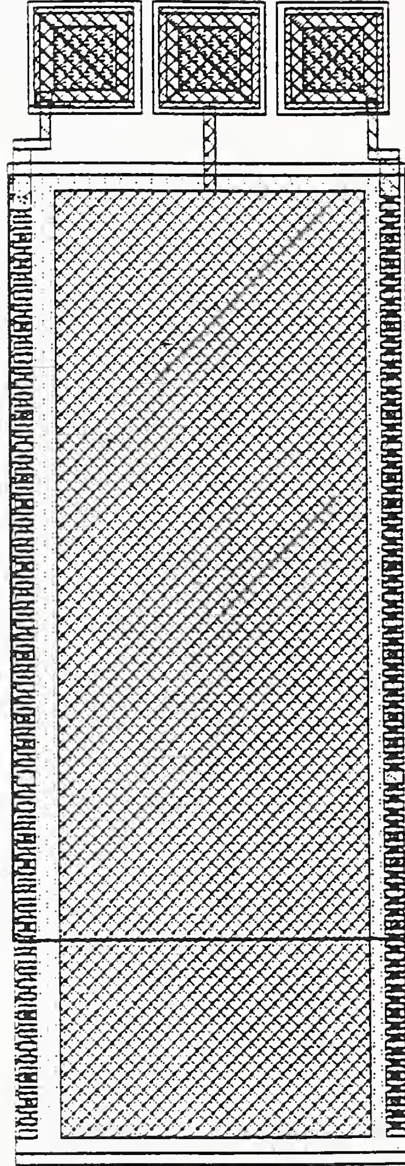


Figure 44. Pwell resistor (Lpoly=500 μm, Wpoly=1500 μm).

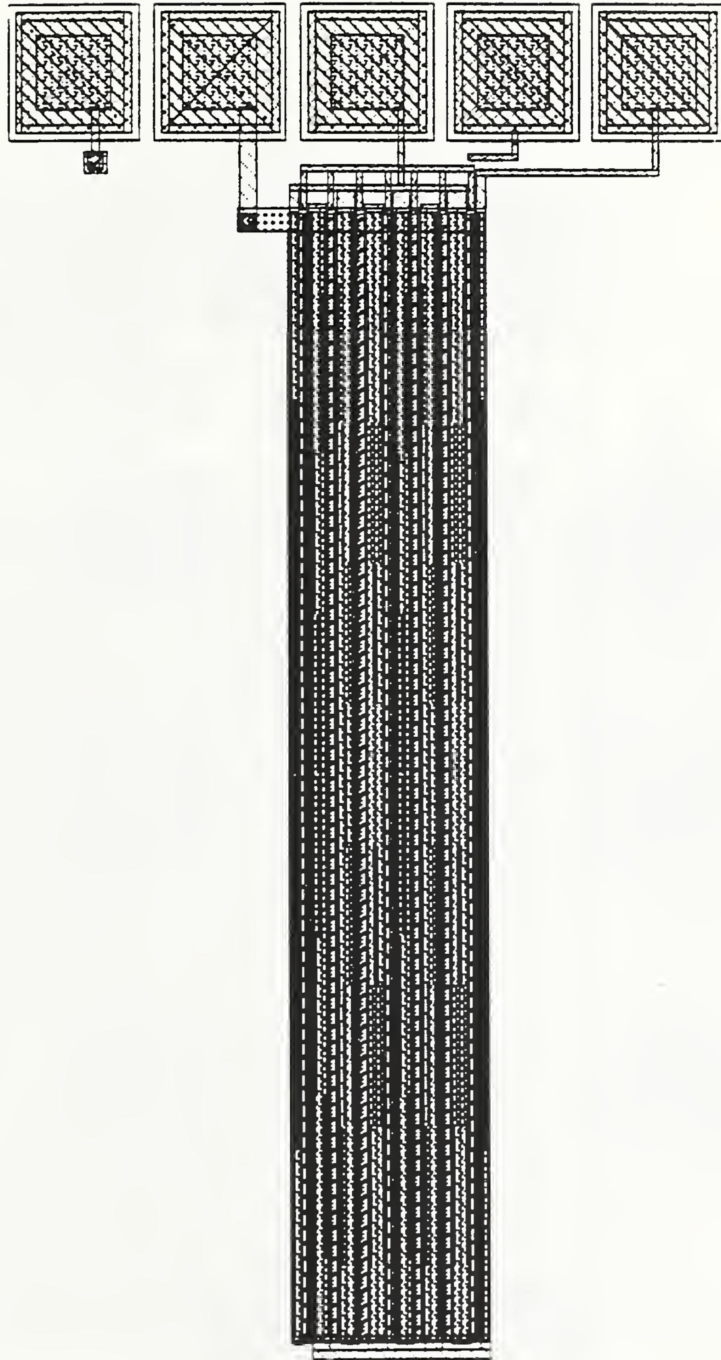


Figure 45. *P*-channel polysilicon gate MOSFET (L=10 μm, W=7 x 1500 μm).

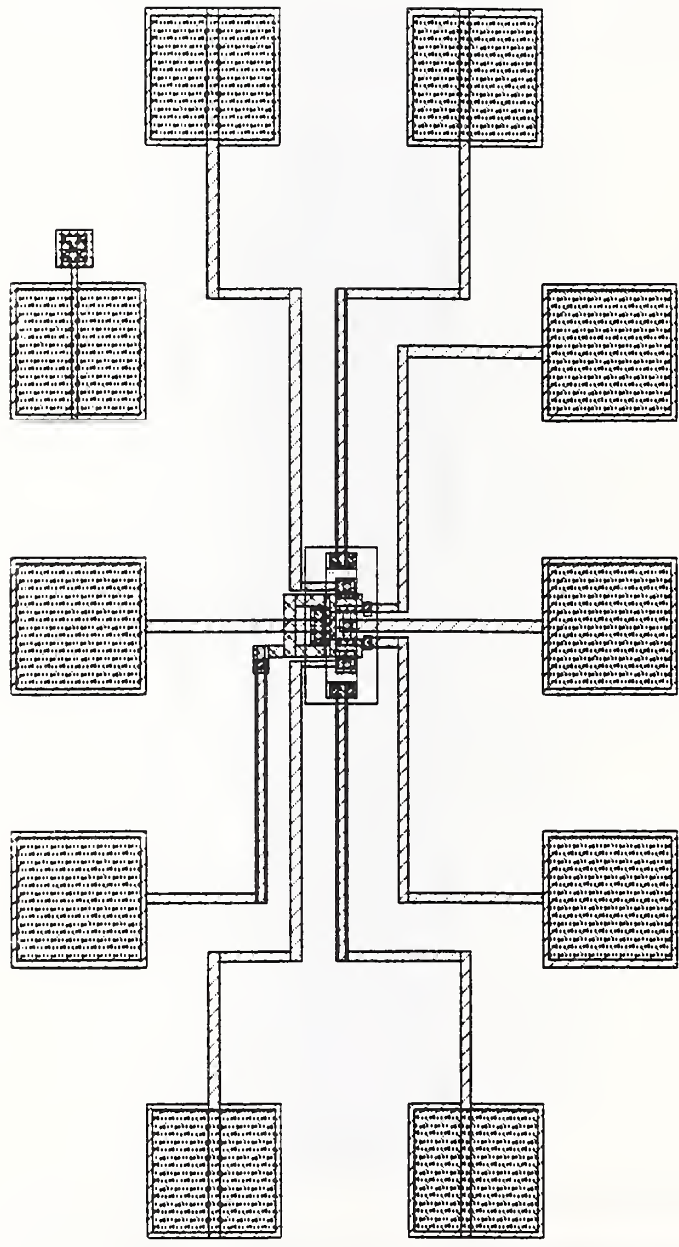


Figure 46. Bipolar magnetotransistor.

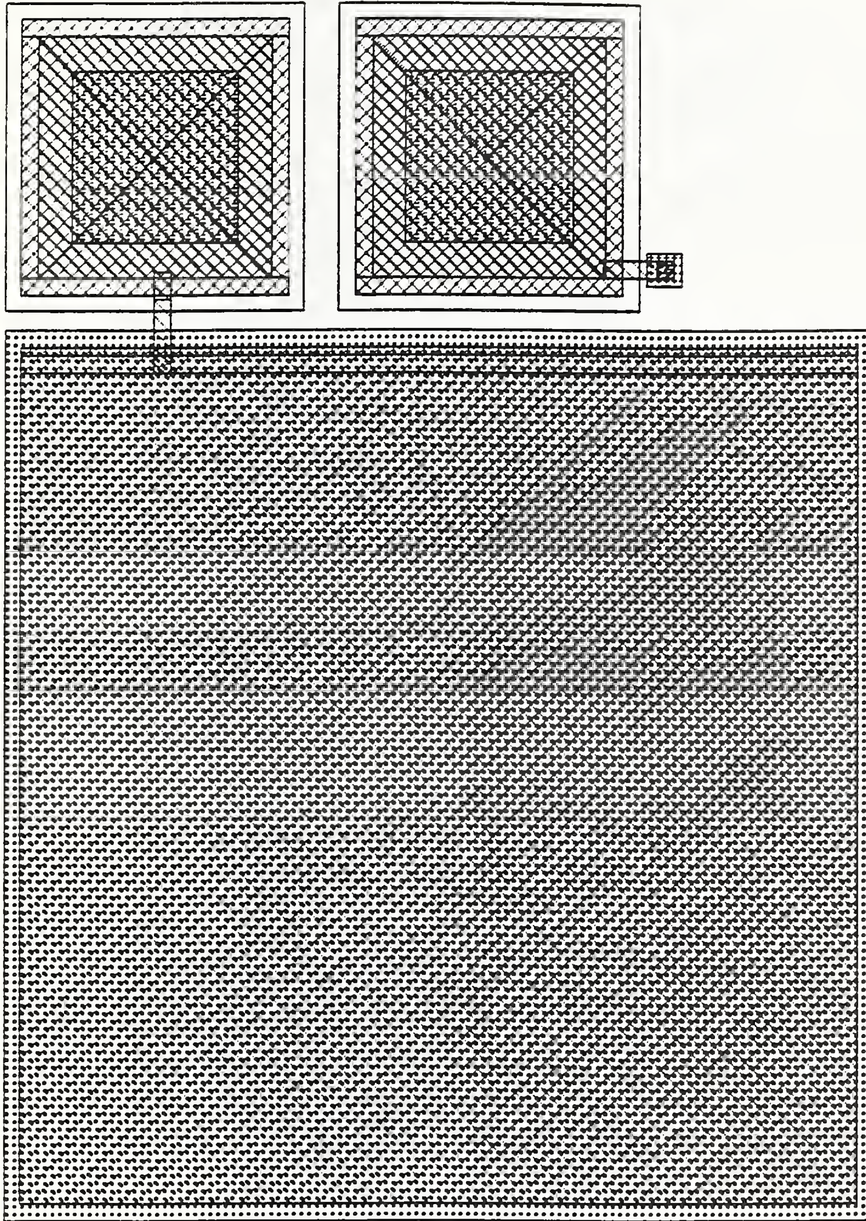


Figure 47. Polysilicon-over-nwell-to-substrate capacitor (Area=500 μm x 500 μm).

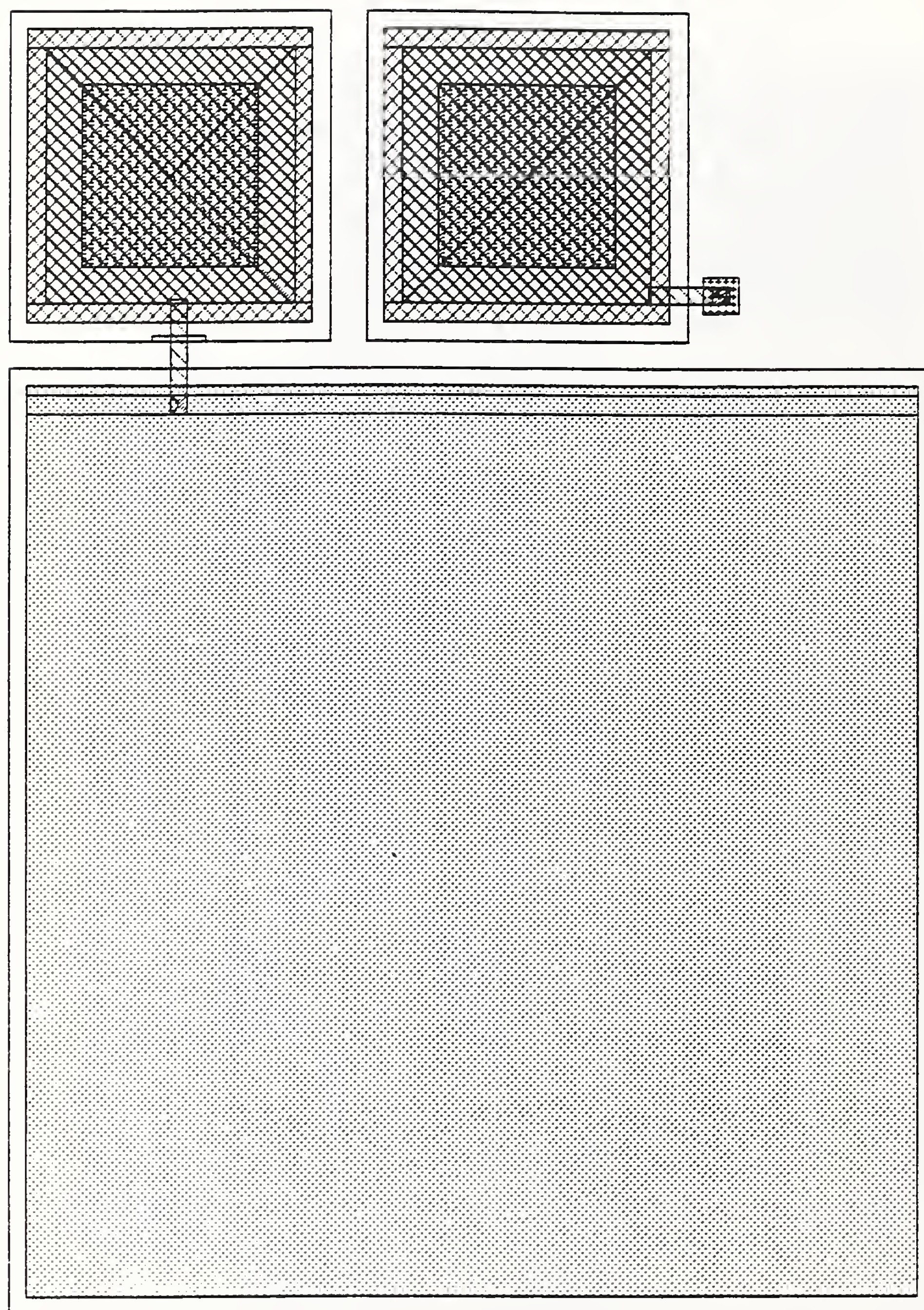


Figure 48. Ndiffusion-to-substrate capacitor (Area=500 μm x 500 μm).

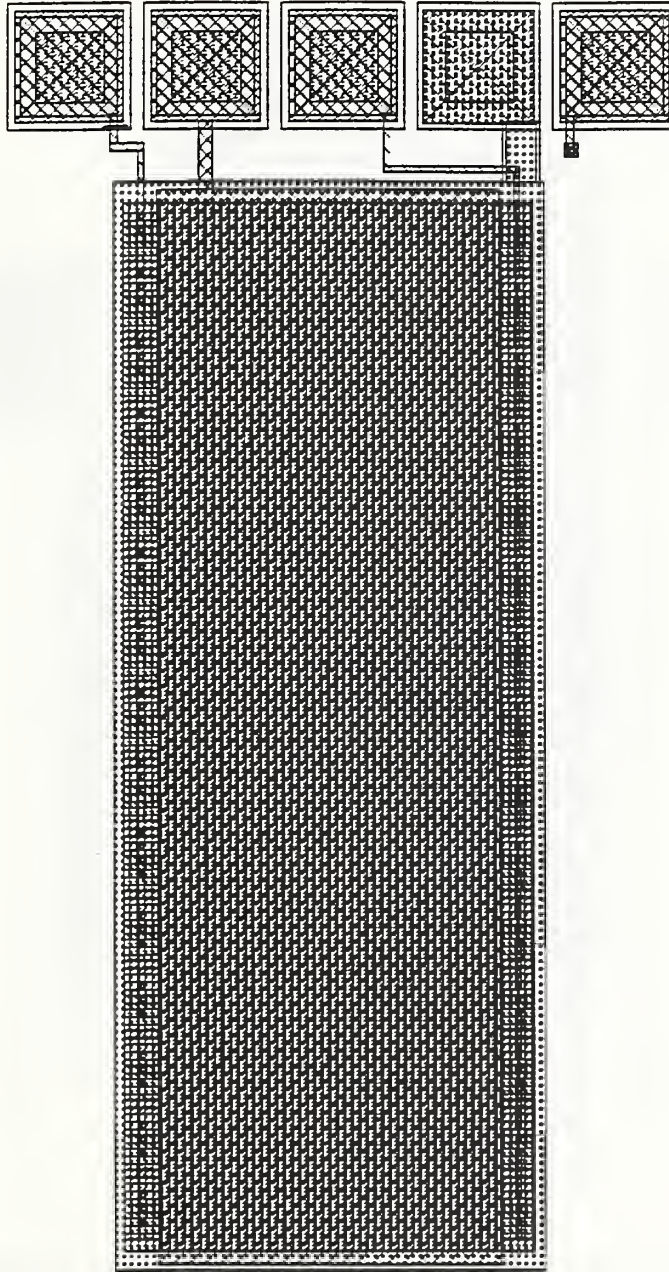


Figure 49. *P*-channel polysilicon gate MOSFET (L=500 μm, W=1500 μm).

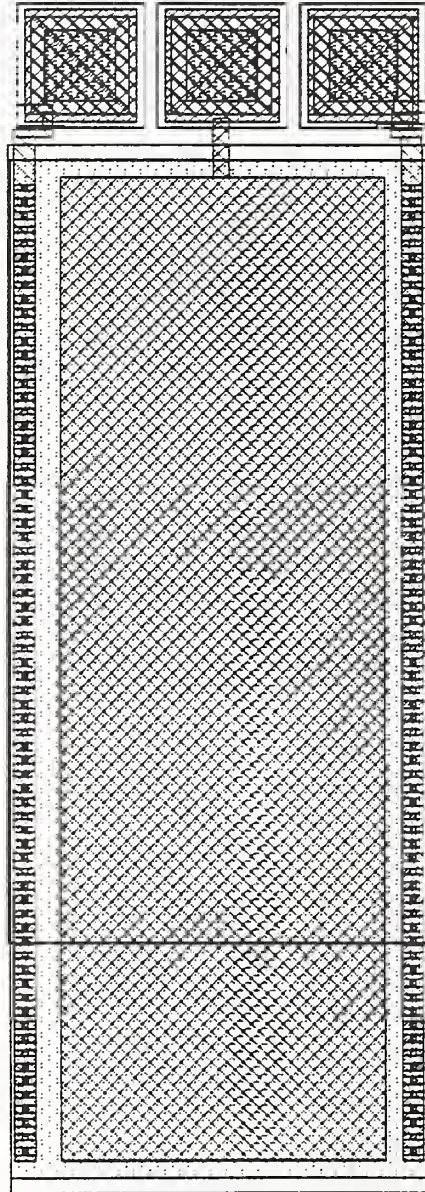


Figure 50. Pwell resistor (Lpoly=460 μm, Wpoly=1410 μm).

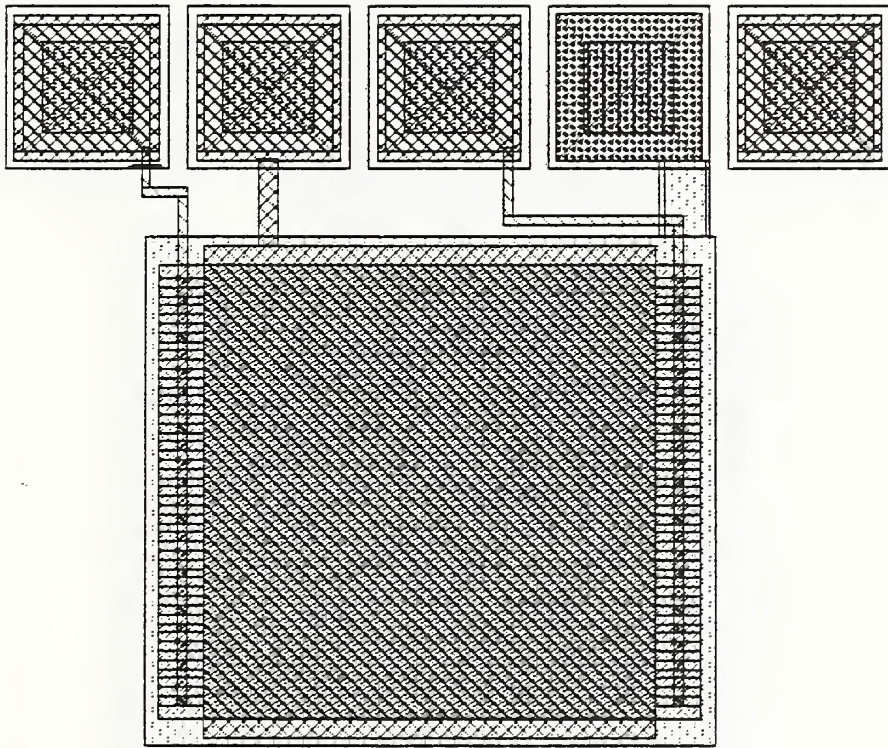


Figure 51. *N*-channel polysilicon gate MOSFET (L=500 μm, W=500 μm).

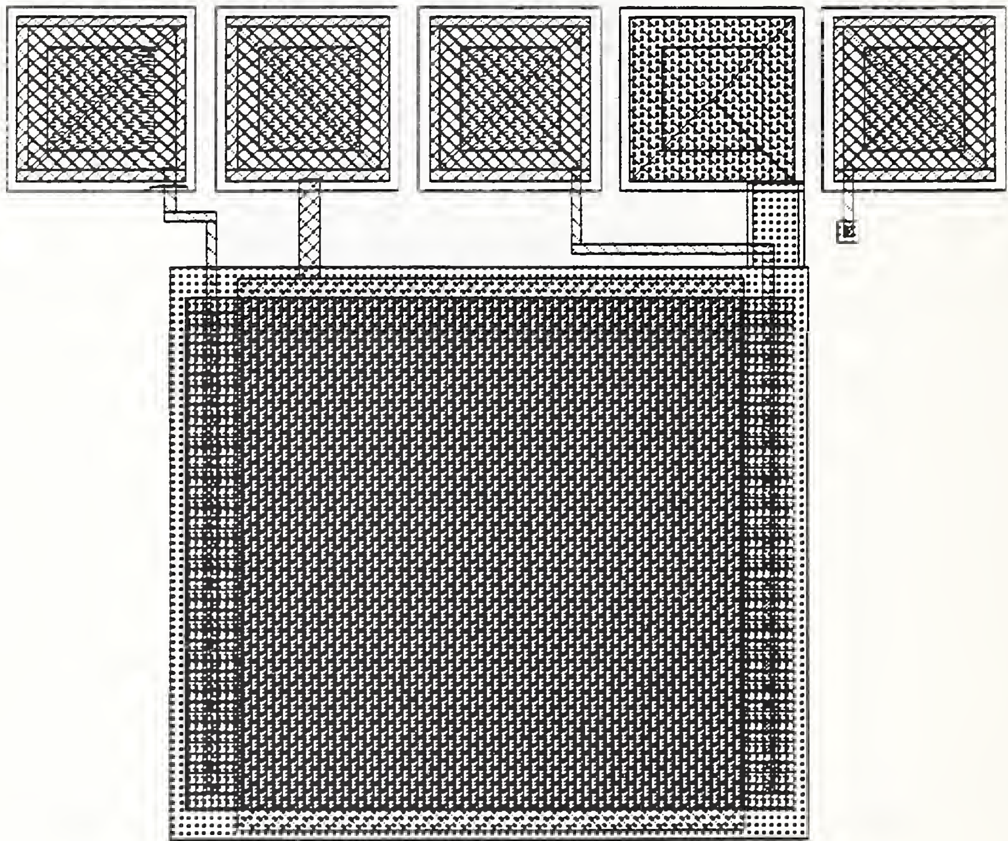


Figure 52. *P*-channel polysilicon gate MOSFET (L=500 μm, W=500 μm).

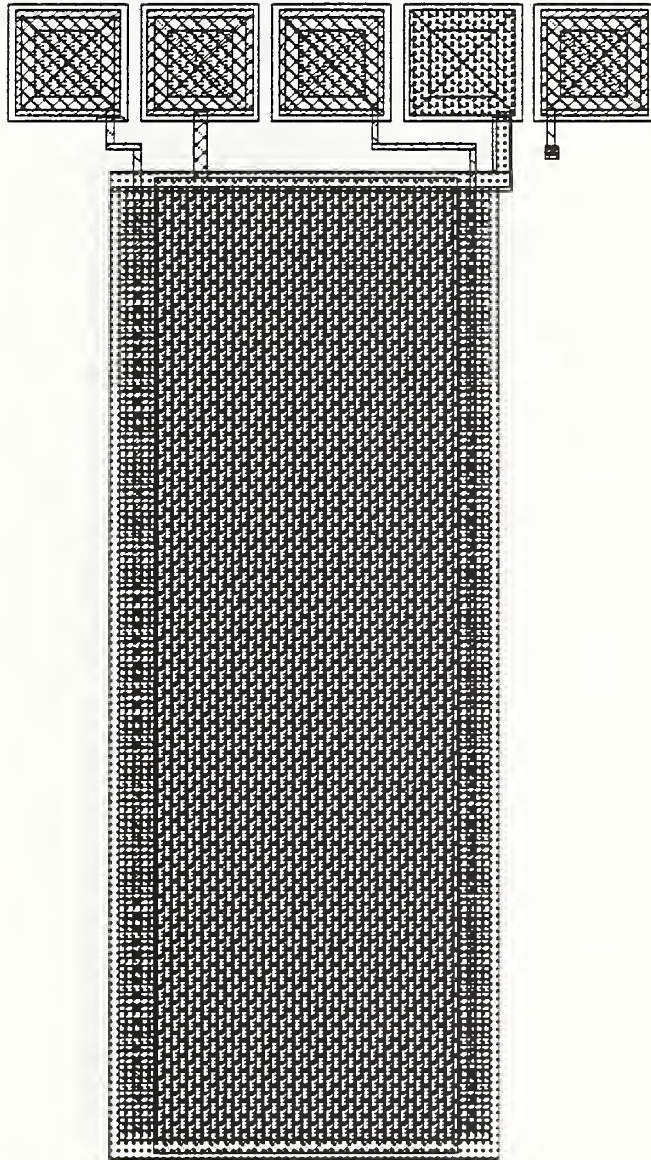


Figure 53. *P*-channel polysilicon gate MOSFET (L=460 μm, W=1440 μm).

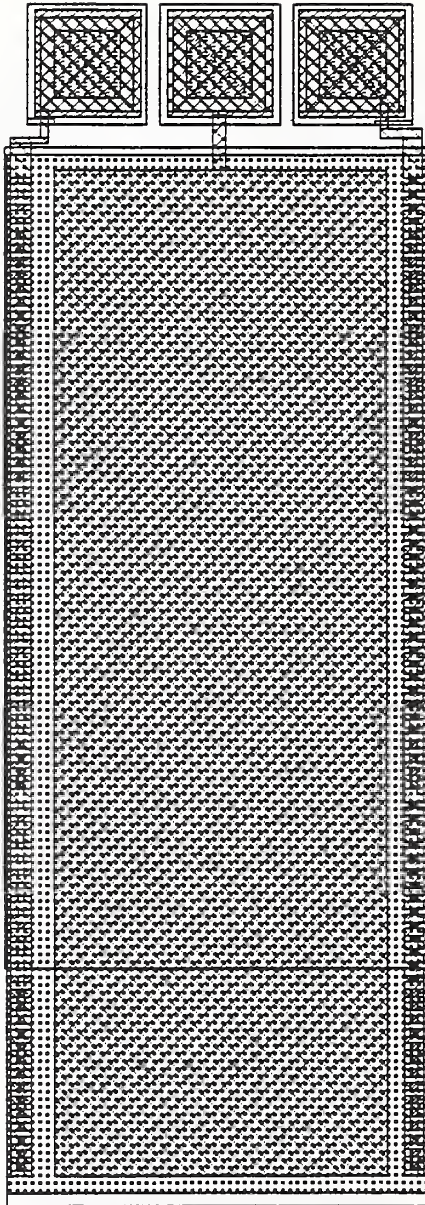


Figure 54. Nwell resistor (Lpoly=500 μm, Wpoly=1500 μm).

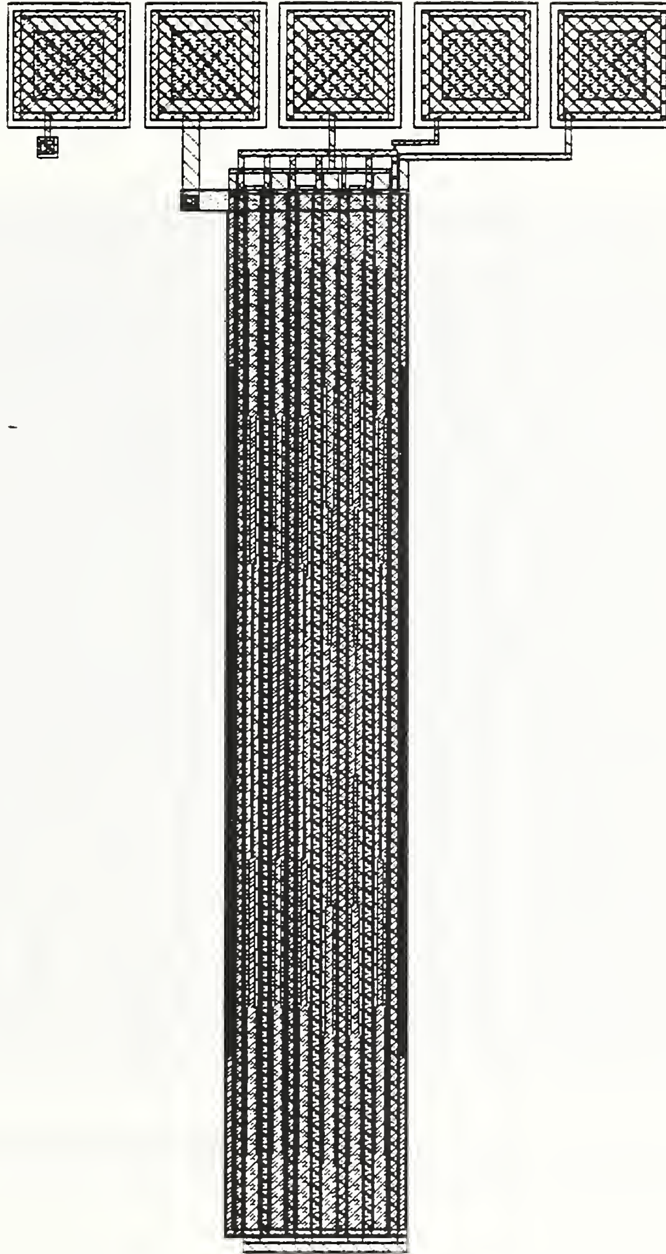


Figure 55. *N*-channel polysilicon gate MOSFET (L=10 μm, W=7 x 1500 μm).

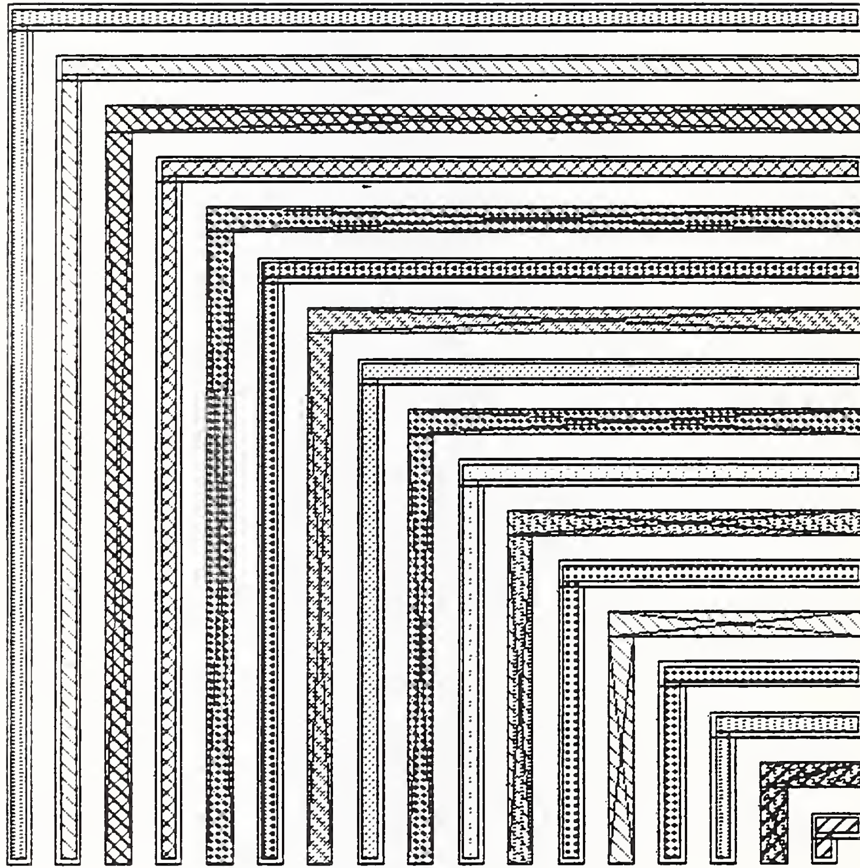


Figure 56. Alignment marks to be used with a clear field mask.

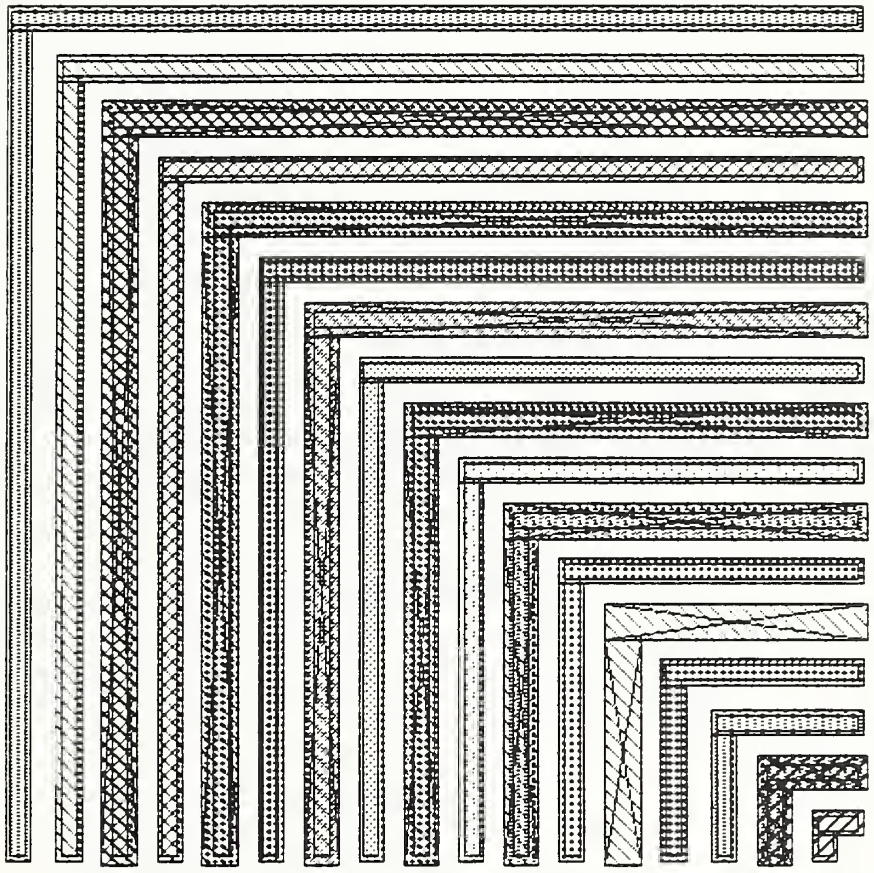
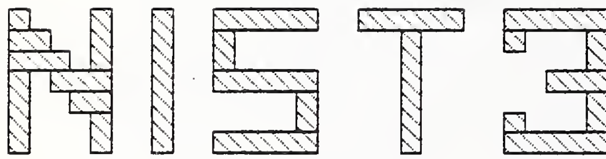


Figure 57. Alignment marks to be used with a dark field mask.



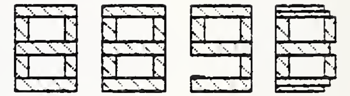


Figure 58. NIST3 identifier.

Table 1. General Location of the Test Structures found on NIST4

Part #	Location	Structures
Part I.		
	Column 1	N-channel MOSFETs with the channel contact beside the drain
	Column 2	P-channel MOSFETs with the channel contact beside the drain
	Column 3	Cross-bridge sheet resistors
	Column 4	Inverters
	Column 5	Contact resistors
	Column 6	Contact resistors
	Column 7	Meanders
	Column 8	Capacitors
	Column 9	Capacitors
	Column 10	Specially-sized MOSFETs
	Column 11	N-channel MOSFETs with the channel contact near the channel
	Column 12	P-channel MOSFETs with the channel contact near the channel
Part II.		
	Column 13	Component parts of the dynamic test structures and miscellaneous structures
	Column 14	Dynamic test structures ($L=6\mu m$)
	Column 15	Dynamic test structures ($L=4\mu m$)
Part III.		
	Bond Pads on Top of the chip	N-channel MOSFETs
	Bond Pads on Left of the chip	N-channel MOSFETs
	Bond Pads on Bottom of the chip	P-channel MOSFETs
	Bond Pads on Right of the chip	P-channel MOSFETs
Part IV.		
	Row 1	N-channel RF transistors (spacing between the electrodes=$50\mu m$)
	Row 2	N-channel RF transistors (spacing between the electrodes=$60\mu m$)
	Row 3	N-channel RF transistors (spacing between the electrodes=$70\mu m$)
	Row 4	P-channel RF transistors (spacing between the electrodes=$50\mu m$)
	Row 5	P-channel RF transistors (spacing between the electrodes=$60\mu m$)
	Row 6	P-channel RF transistors (spacing between the electrodes=$70\mu m$)
Miscellaneous locations		miscellaneous structures

Table 2. Basic Test Structures found on NIST4 (and the parameters measured)

Structure	Parameter(s) Measured	Where on NIST4	Sample Figure(s)	Ref.
Contact resistors	Contact resistance	Part I C 5 & 6	11,12, 13	[4]
Cross-bridge sheet resistors	Sheet resistance Bridge width	Part I C 3	9	[2]
MOSFETs	Transistor characteristics, Gate oxide parameters, Electrical channel length, Interface trapped charge density	Part I C 1 & 2 C 11 & 12 C 13 Part III Top, Left Bottom, Right	7,8 19 20 25 26 27	[9] [10,11]
RF transistors	Switching speed	Part IV R 1-6	28,29	[8]
Inverters	Inverter characteristics	Part I C 4 C 13	10	[3]
Capacitors	Capacitance	Part I C 8 & 9	16,17, 18	[3]
Meanders	Connectivity	Part I C 7	14,15	[5]
Ring oscillators	Frequency Inverter delay	Part II C 14 & 15	21	[3,12]
Shift register	Data retention vs. clocking speed	Part II C 14 & 15	22	[3]
Static RAM cell	Data retention	Part II C 14 & 15	23	[13]

Table 3. Electrical Test Structure Information for Column 1 (N-Channel MOSFETs with channel contact beside the drain) and Column 2 (P-Channel MOSFETs with channel contact beside the drain) (B=substrate,D=drain,S=source,G=gate,W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. subcon		B-B
2. n2tran6 (p2tran6)	(L=2,W=6)	G-W S-D
3. n3tran6 (p3tran6)	(L=3,W=6)	G-W S-D
4. n4tran6 (p4tran6)	(L=4,W=6)	G-W S-D
5. n5tran6 (p5tran6)	(L=5,W=6)	G-W S-D
6. n6tran6 (p6tran6)	(L=6,W=6)	G-W S-D
7. subcon		B-B
8. n7tran6 (p7tran6)	(L=7,W=6)	G-W S-D
9. n8tran6 (p8tran6)	(L=8,W=6)	G-W S-D
10. n9tran6 (p9tran6)	(L=9,W=6)	G-W S-D
11. n10tran6 (p10tran6)	(L=10,W=6)	G-W S-D
12. n15tran6 (p15tran6)	(L=15,W=6)	G-W S-D
13. subcon		B-B
14. n20tran6 (p20tran6)	(L=20,W=6)	G-W S-D
15. n25tran6 (p25tran6)	(L=25,W=6)	G-W S-D
16. n30tran6 (p30tran6)	(L=30,W=6)	G-W S-D

17. n6tran4 (p6tran4)	(L=6,W=4)	G-W S-D
18. subcon		B-B
19. n6tran8 (p6tran8)	(L=6,W=8)	G-W S-D
20. n6tran10 (p6tran10)	(L=6,W=10)	G-W S-D
21. n6tran20 (p6tran20)	(L=6,W=20)	G-W S-D
22. n6tran30 (p6tran30)	(L=6,W=30)	G-W S-D
23. subcon		B-B

Table 4. Electrical Test Structure Information for Column 3
{Cross-Bridge Sheet Resistors (W=10μm, L=130μm)}
(B=substrate)

Designed Cell Name	Bridge Material	Electrical Pad Connections
1. subcon		B-B
2. cbmet	metal	V1-I1 V2-I2 V3-I3 V4-V5
3. cbpol	polysilicon	V1-I1 V2-I2 V3-I3 V4-V5
4. subcon		B-B
5. cbnd	ndiffusion	V1-I1 V2-I2 V3-I3 V4-V5
6. cbpd	pdiffusion	V1-I1 V2-I2 V3-I3 V4-V5
7. subcon		B-B
8. cbnw	n-well	V1-I1 V2-I2 V3-I3 V4-V5
9. cbpn	p-well	V1-I1 V2-I2 V3-I3 V4-V5
10. subcon		B-B
11. cbnfet	n-channel MOSFET	V1-I1 V2-I2 V3-I3 V4-V5
12. cbpfet	p-channel MOSFET	V1-I1 V2-I2 V3-I3

		V4-V5
13. subcon		B-B
14. cbil	island	V1-I1 V2-I2 V3-I3 V4-V5

Table 5. Electrical Test Structure Information for Column 4
{Inverters ($Wn=6\mu m$, $Wp=12\mu m$)}
(SUB=substrate,NW=nwell,PW=pwell)

Designed Cell Name	Channel length (μm)	Electrical Pad Connections
1. inv3	(L=3)	VCC-SUB NW-OUT IN-VSS PW-SUB
2. inv4	(L=4)	VCC-SUB NW-OUT IN-VSS PW-SUB
3. inv5	(L=5)	VCC-SUB NW-OUT IN-VSS PW-SUB
4. inv6	(L=6)	VCC-SUB NW-OUT IN-VSS PW-SUB
5. inv7	(L=7)	VCC-SUB NW-OUT IN-VSS PW-SUB
6. inv8	(L=8)	VCC-SUB NW-OUT IN-VSS PW-SUB
7. inv9	(L=9)	VCC-SUB NW-OUT IN-VSS PW-SUB
8. inv10	(L=10)	VCC-SUB NW-OUT IN-VSS PW-SUB
9. inv11	(L=11)	VCC-SUB NW-OUT IN-VSS PW-SUB

10. inv12	(L=12)	VCC-SUB NW-OUT IN-VSS PW-SUB
11. subcon		SUB-SUB

Table 6. Electrical Test Structure Information for Column 5 (Contact Resistors) (B=substrate)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. subcon	substrate contacts	B-B
2. conpoly4x4w6r	6-pad metal-to-polysilicon (4x4μm contact with 6μm runners)	1-2 3-4 5-6
3. conndiff4x4w6r	6-pad metal-to-ndiffusion in pwell (4x4w6r)	1-2 3-4 5-6
4. conpdiff4x4w6r	6-pad metal-to-pdiffusion in nwell (4x4w6r)	1-2 3-4 5-6
5. subcon	substrate contacts	B-B
6. connw4x4	4-pad metal-to-nwell (4x4μm contact with 4μm runners)	I1-V1 V2-I2
7. conpw4x4	4-pad metal-to-pwell (4x4w4r)	I1-V1 V2-I2
8. conil4x4	4-pad metal-to-island (4x4w4r)	I1-V1 V2-I2
9. consub4x4	4-pad metal-to-substrate (4x4w4r) nonsensical structure	I1-V1 V2-I2
10. subcon	substrate contacts	B-B
11. constringpol	metal-to-polysilicon Kelvin chain (14-4x4μm contacts)	I1-V1 I2-V2
12. constringndiff	metal-to-ndiffusion in pwell Kelvin chain (14-4x4μm contacts)	I1-V1 I2-V2
13. constringpdiff	metal-to-pdiffusion in nwell Kelvin chain (14-4x4μm contacts)	I1-V1 I2-V2
14. subcon	substrate contacts	B-B
15. constringpol	same as 11	
16. constringndiff	same as 12	
17. constringpdiff	same as 13	

18. subcon	substrate contacts	B-B
19. constringpol	same as 11	
20. constringndiff	same as 12	
21. constringpdiff	same as 13	
22. subcon	substrate contacts	B-B

Table 7. Electrical Test Structure Information for Column 6
(Contact Resistors)
(B=substrate)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. subcon	substrate contacts	B-B
2. conpoly4x4	6-pad metal-to-polysilicon (4x4μm contact with 4μm runners)	1-2 3-4 5-6
3. conndiff4x4	6-pad metal-to-ndiffusion in pwell (4x4w4r)	1-2 3-4 5-6
4. conpdiff4x4	6-pad metal-to-pdiffusion in nwell	1-2 3-4 5-6
5. subcon	substrate contacts	B-B
6. conpoly6x6	6-pad metal-to-polysilicon (6x6w6r)	1-2 3-4 5-6
7. conndiff6x6	6-pad metal-to-ndiffusion in pwell (6x6w6r)	1-2 3-4 5-6
8. conpdiff6x6	6-pad metal-to-pdiffusion in nwell (6x6w6r)	1-2 3-4 5-6
9. subcon	substrate contacts	B-B
10. conpoly8x8	6-pad metal-to-polysilicon (8x8w8r)	1-2 3-4 5-6
11. conndiff8x8	6-pad metal-to-ndiffusion in pwell (8x8w8r)	1-2 3-4 5-6
12. conpdiff8x8	6-pad metal-to-pdiffusion in nwell (8x8w8r)	1-2 3-4 5-6
13. subcon	substrate contacts	B-B

14. conpoly16x16	6-pad metal-to-polysilicon (16x16w16r)	1-2 3-4 5-6
15. conndiff16x16	6-pad metal-to-ndiffusion in pwell (16x16w16r)	1-2 3-4 5-6
16. conpdiff16x16	6-pad metal-to-pdiffusion in nwell (16x16w16r)	1-2 3-4 5-6
17. subcon	substrate contacts	B-B

Table 8. Electrical Test Structure Information for Column 7 (Meanders)
(L=left edge, R=right edge, T=top edge, B=bottom edge, SUB=substrate)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. meanpol	polysilicon over island left/right edges (Wpoly=10μm)	L-R L-R
2. meanpola	polysilicon over island top/bottom edges (Wpoly=10μm)	T-T B-B
3. meanmet	metal over island left/right edges (Wmet=10μm)	L-R L-R
4. meanmeta	metal over island top/bottom edges (Wmet=10μm)	T-T B-B
5. meanmp	metal atop polysilicon over island left/right edges (Wpoly=10μm, Wmet=6μm)	L-R L-R
6. meanmpa	metal atop polysilicon over island top/bottom edges (Wpoly=10μm, Wmet=6μm)	T-T B-B
7. meanpol	same as 1	
8. meanpola	same as 2	
9. meanmet	same as 3	
10. meanmeta	same as 4	
11. meanmp	same as 5	
12. meanmpa	same as 6	
13. meanpol	same as 1	
14. meanpola	same as 2	
15. meanmet	same as 3	
16. meanmeta	same as 4	
17. meanmp	same as 5	
18. meanmpa	same as 6	
19. meanmp	same as 5	
20. meanmpa	same as 6	
21. subcon	substrate contacts	SUB-SUB

Table 9. Electrical Test Structure Information for Columns 8 and 9 (Capacitors)
(B=substrate, M=metal, P=polysilicon, ND=ndiffusion, PD=pdiffusion, NW=nwell, PW=pwell, NND=nndiff, PPD=ppdiff, X=not used)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. capmet	metal-substrate (Area=16900μm^2)	M-X B-X
2. cappolnw	polysilicon over nwell-substrate (Area=16775μm^2)	P-X B-X
3. cappolpw	polysilicon over pwell-substrate (Area=16775μm^2)	P-X B-X
4. capmetpol	metal-polysilicon-substrate (Areamet=16650μm^2, Areapoly=21300μm^2)	M-X B-P
5. capchann	polysilicon over nwell-nearby nndiff in same nwell-substrate (Areapoly=11625μm^2, Areanndiff=9611μm^2)	P-X B-NND
6. capchanp	polysilicon over pwell-nearby ppdiff in same pwell-substrate (Area=11625μm^2, Areanndiff=9611μm^2)	P-X B-PPD
7. capn	ndiffusion-substrate (Area=16600μm^2)	ND-X B-X
8. capp	pdiffusion-substrate (Area=16600μm^2)	PD-X B-X
9. capnw	nwell-substrate (Area=17050μm^2)	NW-X B-X
10. cappw	pwell-substrate (Area=17050μm^2)	PW-X B-X
11. capmet	same as 1	
12. cappolnw	same as 2	
13. cappolpw	same as 3	
14. capmetpol	same as 4	
15. capchann	same as 5	
16. capchanp	same as 6	
17. capn	same as 7	
18. capp	same as 8	
19. capnw	same as 9	
20. cappw	same as 10	

Table 10. Electrical Test Structure Information for Column 10
(Specially-sized Polysilicon Gate MOSFETs)
(B=substrate, D=drain, S=source, G=gate, W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. nl3w3	n-channel MOSFET (L=3,W=3)	G-W S-D
2. nl4w4	n-channel MOSFET (L=4,W=4)	G-W S-D
3. nl5w5	n-channel MOSFET (L=5,W=5)	G-W S-D
4. nl6w6	n-channel MOSFET (L=6,W=6)	G-W S-D
5. subcon		B-B
6. nl10w10	n-channel MOSFET (L=10,W=10)	G-W S-D
7. nl20w20	n-channel MOSFET (L=20,W=20)	G-W S-D
8. nl30w30	n-channel MOSFET (L=30,W=30)	G-W S-D
9. nl6w30	n-channel MOSFET (L=6,W=30)	G-W S-D
10. nl30w6	n-channel MOSFET (L=30,W=6)	G-W S-D
11. subcon		B-B
12. pl3w3	p-channel MOSFET (L=3,W=3)	G-W S-D
13. pl4w4	p-channel MOSFET (L=4,W=4)	G-W S-D
14. pl5w5	p-channel MOSFET (L=5,W=5)	G-W S-D
15. pl6w6	p-channel MOSFET (L=6,W=6)	G-W S-D
16. subcon		B-B

17. pl10w10	p-channel MOSFET (L=10,W=10)	G-W S-D
18. pl20w20	p-channel MOSFET (L=20,W=20)	G-W S-D
19. pl30w30	p-channel MOSFET (L=30,W=30)	G-W S-D
20. pl6w30	p-channel MOSFET (L=6,W=30)	G-W S-D
21. pl30w6	p-channel MOSFET (L=30,W=6)	G-W S-D
22. subcon		B-B
23. subcon		B-B

Table 11. Electrical Test Structure Information for Column 11 (n-channel MOSFETs with the channel contact near the channel) and Column 12 (p-channel MOSFETs with the channel contact near the channel) (B=substrate,D=drain,S=source,G=gate,W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. subcon		B-B
2. n2tran6a (p2tran6a)	(L=2,W=6)	G-D S-W
3. n3tran6a (p3tran6a)	(L=3,W=6)	G-D S-W
4. n4tran6a (p4tran6a)	(L=4,W=6)	G-D S-W
5. n5tran6a (p5tran6a)	(L=5,W=6)	G-D S-W
6. n6tran6a (p6tran6a)	(L=6,W=6)	G-D S-W
7. subcon		B-B
8. n7tran6a (p7tran6a)	(L=7,W=6)	G-D S-W
9. n8tran6a (p8tran6a)	(L=8,W=6)	G-D S-W
10. n9tran6a (p9tran6a)	(L=9,W=6)	G-D S-W
11. n10tran6a (p10tran6a)	(L=10,W=6)	G-D S-W
12. n15tran6a (p15tran6a)	(L=15,W=6)	G-D S-W
13. subcon		B-B
14. n20tran6a (p20tran6a)	(L=20,W=6)	G-D S-W
15. n25tran6a (p25tran6a)	(L=25,W=6)	G-D S-W
16. n30tran6a (p30tran6a)	(L=30,W=6)	G-D S-W

17. n6tran4a (p6tran4a)	(L=6,W=4)	$\overline{\text{G-D}}$ S-W
18. subcon		$\overline{\text{B-B}}$
19. n6tran8a (p6tran8a)	(L=6,W=8)	$\overline{\text{G-D}}$ S-W
20. n6tran10a (p6tran10a)	(L=6,W=10)	$\overline{\text{G-D}}$ S-W
21. n6tran20a (p6tran20a)	(L=6,W=20)	$\overline{\text{G-D}}$ S-W
22. n6tran30a (n6tran30a)	(L=6,W=30)	$\overline{\text{G-D}}$ S-W
23. subcon		$\overline{\text{B-B}}$

Table 12. Electrical Test Structure Information for Column 13 (Component Parts of the Dynamic Test Structures and Miscellaneous Structures) (SUB=substrate, NW=nwell, PW=pwell, G=gate, S=source, D=drain, X=not used)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. invringamp	inverter from ring with amplifier (L_n=6μm, L_p=6μm, W_n=24μm, W_p=48μm)	VCC-SUB NW-OUT IN-VSS PW-SUB
2. ninvringamp	n-channel MOSFET from inverter in No.1	X-D G-S PW-SUB
3. pinvringamp	p-channel MOSFET from inverter in No.1	S-SUB NW-D G-X
4. invringamp4	inverter from ring with amplifier (L_n=4μm, L_p=4μm, W_n=24μm, W_p=48μm)	VCC-SUB NW-OUT IN-VSS PW-SUB
5. ninvringamp4	n-channel MOSFET from inverter in No.4	X-D G-S PW-SUB
6. pinvringamp4	p-channel MOSFET from inverter in No.4	S-SUB NW-D G-X
7. subcon	substrate contacts	SUB-SUB
8. nl6w24	n-channel MOSFET (L=6μm, W=24μm)	G-PW S-D
9. pl6w12	p-channel MOSFET (L=6μm, W=12μm)	G-W S-D
10. pl6w48	p-channel MOSFET (L=6μm, W=48μm)	G-W S-D
11. subcon	substrate contacts	SUB-SUB
12. nl4w24	n-channel MOSFET (L=4μm, W=24μm)	G-W S-D
13. pl4w12	p-channel MOSFET (L=4μm, W=12μm)	G-W S-D

14. pl4w48	p-channel MOSFET (L=4μm, W=48μm)	G-W S-D
15. subcon	substrate contacts	SUB-SUB
16. lgperimn	n-channel MOSFET with snake-like gate with lots of corners (L=10μm)	S-D G-W
17. lgperimp	p-channel MOSFET with snake-like gate with lots of corners (L=10μm)	S-D G-W
18. subcon	substrate contacts	SUB-SUB
19. subcon	substrate contacts	SUB-SUB

Table 13. Electrical Test Structure Information for Column 14 (Dynamic Test Structures (Ln=6μm, Lp=6μm)) and Column 15 (Dynamic Test Structures (Ln=4μm, Lp=4μm)) (SUB=substrate, PW=pwell, NW=nwell, PH1=phase 1 clock, PH2=phase 2 clock, X=not used)

Designed Cell Name	Structure Identification	Electrical Pad Connections
1. ring6 (ring4)	Ring Oscillator (Wn=6μm, Wp=12μm) 23-stages same NAND gate startup as in No.3 when A=0 oscillations disabled when A=1 oscillations enabled	SUB-VCC PW-NW VSS-OUT X-A
2. amp (amp4)	4-stage output amplifier (Wnmin=6μm, Wpmin=12μm, Wnmax=48μm, Wpmax=96μm) amplification factor=2	X-SUB VCC-NW PW-IN VSS-OUT
3. nand (nand4)	NAND gate (Wn=6μm, Wp=12μm)	VCC-SUB IN-NW A-VSS PW-OUT
4. ringamp (ringamp4)	Ring Oscillator (Wn=24μm, Wp=48μm) 23-stages same 4-stage output amplifier as in No.2 NAND gate startup (Wn=24μm, Wp=48μm) when A=0 oscillations disabled when A=1 oscillations enabled	SUB-VCC PW-NW A-VSS SUBa-VCCa PWa-NWa VSSa-OUT
5. ringfan2 (ring4fan2)	Ring Oscillator (Wn=24μm, Wp=48μm) 23-stages fanout of 2 same 4-stage output amplifier as in No.2	SUB-VCC PW-NW VSS-X X-X X-X SUBa-VCCa PWa-NWa VSSa-OUT
6. shift (shift4)	Shift Register 20-stages 2-clocks same 4-stage output amplifier as in No.2	VCC-NW PH1-PH2 IN-VSS PW-SUB X-OUT X-X
7. sramcell (sramcell4)	6-T Static RAM cell (Wn=6μm, Wp=36μm) Two 4-stage output amplifiers as in No.2	Wsel-data bit-VSS

	RESTING STATE: latch=0,rwsel=0,wsel=0 TO READ: rwsel=1,data=data in cell databar=databar TO WRITE: latch=1,rwsel=1,wsel=1, Then - latch=0,rwsel=0,wsel=0	VCC-RWsel NW-latch databar-SUB
8. subcon	substrate contacts	SUB-SUB
9. subcon	substrate contacts	SUB-SUB
10. subcon	substrate contacts	SUB-SUB

Table 14. Electrical Test Structure Information for Bond Pads Top (n-channel MOSFETs) and Bond Pads Bottom (p-channel MOSFETs) (SUB=substrate, D=drain, S=source, G=gate, W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. bondnl2w6 (bondpl2w6)	(L=2, W=6)	D-G-S-W
2. bondsubcon (bondsubcona)		SUB
3. bondnl4w6 (bondpl4w6)	(L=4, W=6)	D-G-S-W
4. bondsubcon (bondsubcona)		SUB
5. bondnl6w6 (bondpl6w6)	(L=6, W=6)	D-G-S-W
6. bondsubcon (bondsubcona)		SUB
7. bondnl8w6 (bondpl8w6)	(L=8, W=6)	D-G-S-W
8. bondsubcon (bondsubcona)		SUB
9. bondnl10w6 (bondpl10w6)	(L=10, W=6)	D-G-S-W
10. bondsubcon (bondsubcona)		SUB
11. bondnl20w6 (bondpl20w6)	(L=20, W=6)	D-G-S-W
12. bondsubcon (bondsubcona)		SUB
13. bondnl30w6 (bondpl30w6)	(L=30, W=6)	D-G-S-W
14. bondsubcon (bondsubcona)		SUB
15. bondnl6w10 (bondpl6w10)	(L=6, W=10)	D-G-S-W

16. bondsubcon (bondsubcona)		SUB
17. bondnl6w30 (bondpl6w30)	(L=6,W=30)	D-G-S-W
18. bondsubcon (bondsubcona)		SUB

Table 15. Electrical Test Structure Information for Bond Pads Left (n-channel MOSFETs) (SUB=substrate, D=drain, S=source, G=gate, W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. bondsubconb		SUB
2. bondnl3w3	(L=3,W=3)	W S G D
3. bondsubconb		SUB
4. bondnl4w4	(L=4,W=4)	W S G D
5. bondsubconb		SUB
6. bondnl5w5	(L=5,W=5)	W S G D
7. bondsubconb		SUB
8. bondnl8w8	(L=8,W=8)	W S G D
9. bondsubconb		SUB
10. bondnl10w10	(L=10,W=10)	W S G D
11. bondsubconb		SUB
12. bondnl20w20	(L=20,W=20)	W S G D
13. bondsubconb		SUB

14. bondnl30w30	(L=30,W=30)	W S G D
15. bondsubconb		SUB
16. bondleakn	a MOSFET with a comb-shaped gate to measure the leakage around the edge of the gate (L=6,W=36x13 teeth)	D W G S
17. bondsubconb		SUB
18. circxtorn	a MOSFET with a square-shaped gate (L=50) the central source area is 150μm x 150μm	W S G D SUB
19. bondsubconb		SUB

Table 16. Electrical Test Structure Information for Bond Pads Right (p-channel MOSFETs) (SUB=substrate, D=drain, S=source, G=gate, W=well)

Designed Cell Name	MOSFET Dimensions(μm)	Electrical Pad Connections
1. bondsubconc		SUB
2. bondpl3w3	(L=3,W=3)	D G S W
3. bondsubconc		SUB
4. bondpl4w4	(L=4,W=4)	D G S W
5. bondsubconc		SUB
6. bondpl5w5	(L=5,W=5)	D G S W
7. bondsubconc		SUB
8. bondpl8w8	(L=8,W=8)	D G S W
9. bondsubconc		SUB
10. bondpl10w10	(L=10,W=10)	D G S W
11. bondsubconc		SUB
12. bondpl20w20	(L=20,W=20)	D G S W
13. bondsubconc		SUB

14. bondpl30w30	(L=30,W=30)	D G S W
15. bondsubconc		SUB
16. bondleaky	a MOSFET with a comb-shaped gate to measure the leakage around the edge of the gate (L=6,W=36x13 teeth)	S G W D
17. bondsubconc		SUB
18. circxtorp	a MOSFET with a square-shaped gate (L=50) the central source area is 150μm x 150μm	SUB D G S W
19. bondsubconc		SUB

Table 17. Electrical Test Structure Information for:
Row 1 {n-channel rf transistors (W=24μm, spacing=50μm)},
Row 2 {n-channel rf transistors (W=24μm, spacing=60μm)},
Row 3 {n-channel rf transistors (W=24μm, spacing=70μm)},
Row 4 {p-channel rf transistors (W=24μm, spacing=50μm)},
Row 5 {p-channel rf transistors (W=24μm, spacing=60μm)}, and
Row 6 {p-channel rf transistors (W=24μm, spacing=70μm)}
(D=drain, S=source, G=gate)

Designed Cell Name (x=50 for rows 1 and 4) (x=60 for rows 2 and 5) (x=70 for rows 3 and 6)	Channel Length (μm)	Electrical Pad Connections
1. rfxnl2w24 (rfxpl2w24)	(L=2)	S-G-S S-D-S
2. rfxnl3w24 (rfxpl3w24)	(L=3)	S-G-S S-D-S
3. rfxnl4s24 (rfxpl4w24)	(L=4)	S-G-S S-D-S
4. rfxnl5w24 (rfxpl5w24)	(L=5)	S-G-S S-D-S
5. rfxnl6w24 (rfxpl6w24)	(L=6)	S-G-S S-D-S
6. rfxnl7n24 (rfxpl7w24)	(L=7)	S-G-S S-D-S
7. rfxnl8w24 (rfxpl8w24)	(L=8)	S-G-S S-D-S
8. rfxnl9w24 (rfxpl9w24)	(L=9)	S-G-S S-D-S
9. rfxnl10w24 (rfxpl10w24)	(L=10)	S-G-S S-D-S
10. rfxnl11w24 (rfxpl11w24)	(L=11)	S-G-S S-D-S
11. rfxnl12w24 (rfxpl12w24)	(L=12)	S-G-S S-D-S
12. rfxnl10w24 (rfxpl10w24)	(L=10)	S-G-S S-D-S

13. rfxnl11w24 (rfxpl11w24)	(L=11)	S-G-S S-D-S
14. rfxnl12w24 (rfxpl12w24)	(L=12)	S-G-S S-D-S

Table 18. Miscellaneous Structures and Pertinent Information

Designed Cell Name	Remarks
1. alignlight	Alignment marks to be used with a clear field mask Located in the upper left portion of the chip.
2. aligndark	Alignment marks to be used with a dark field mask Located in the upper left portion of the chip.
3. ident	An identification of the levels located Located in the middle left portion of the chip.
4. chevron	Chevrons to check the minimum feature sizes and spaces organized as follows: ndiffusion pdiffusion nwell pwell island polysilicon metal
5. none	The NIST4 identifier

Table 19. Test Structure List with Critical Dimensions for the SIMOX Test Chip, NIST3

Designed Cell Name	Structure	Critical Dimensions(μm)
1. ptr50x50	p-channel MOSFET	(L=50,W=50)
2. ntr50x50	n-channel MOSFET	(L=50,W=50)
3. nresist	nwell resistor	(Lpoly=460, Wpoly=1410)
4. ntr500x1500	n-channel MOSFET	(L=500,W=1500)
5. ntr100x100	n-channel MOSFET	(L=100,W=100)
6. ptr100x100	p-channel MOSFET	(L=100,W=100)
7. ntrans	n-channel MOSFET	(L=460,W=1440)
8. pres1500x500	pwell resistor	(Lpoly=500, Wpoly=1500)
9. ptran7x1500x10	p-channel MOSFET	(L=10,W=7x1500)
10. jontran	a bipolar structure	
11. cappoly500x500	polysilicon over nwell - substrate capacitor	(Area=500μmx500μm)
12. capn500x500	ndiffusion - substrate capacitor	(Area=500μmx500μm)
13. ptr500x1500	p-channel MOSFET	(L=500,W=1500)
14. presist	pwell resistor	(Lpoly=460, Wpoly=1410)
15. ntr500x500	n-channel MOSFET	(L=500,W=500)
16. ptr500x500	p-channel MOSFET	(L=500,W=500)
17. ptrans	p-channel MOSFET	(L=460,W=1440)
18. nres1500x500	nwell resistor	(Lpoly=500, Wpoly=1500)
19. ntran7x1500x10	n-channel MOSFET	(L=10,W=7x1500)

20. alignlight3	alignment marks to be used with a clear field mask
21. aligndark3	alignment marks to be used with a dark field mask
22. none	NIST3 identifier

Appendix - A Computer Program to Determine the Appropriate Dimensions for the RF Transistors

```
C
C     FILENAME:  RFP.FOR
C
C     PURPOSE:  THIS PROGRAM OBTAINS THE DIMENSIONS FOR AN RF TRANSISTOR.

C               A 50 OHM INPUT IMPEDANCE NEEDS TO BE MATCHED.
C               NOTE: USE MICRONS !
C
      DIMENSION NUMFILE(50), FILN1(50), FILN2(50)
C
      open(unit=10, file='in.dat', status='old')
      open(unit=20, file='out.dat', status='old')
C
      c=3.06e8*1.e6                   ! speed of light
      e0=8.85e-14*100e-6              ! in F/micron
      ersio2=3.9                      ! for SiO2
      esi=11.8                        ! for Si
C     ersio2=11.6                     ! for GaAs
C
C     read the data in.....
C
      read (10,*) s                   ! electrode width
      read (10,*) w0                  ! electrode spacing
      w=w0
C
C     perform the following calculations
C
500   er=esi
      ak=s/(s+2*w)
      akp=sqrt(1.-ak**2.)
C
      if ((ak .ge. 0.) .and. (ak .le. (sqrt(2.))/2.)) go to 10
      if ((ak .ge. (sqrt(2.))/2.) .and. (ak .le. 1.)) go to 11
C
      write (20,702)
702   format(1x,'ak in the wrong ballpark')
      go to 900
C
10    akratio=1./((1./3.1416)*alog(2.*(1.+sqrt(akp))/(1.-sqrt(akp))))
      go to 16
11    akratio=(1./3.1416)*alog(2.*(1.+sqrt(ak))/(1.-sqrt(ak)))
C
16    z0=1./(2.*sqrt(2.)*e0*c*sqrt(er+1.)*akratio)
C
C     write the value of z0 in out.dat
C
      write (6,700) s,w,z0
70    format(1x,'s=',F8.2,15x,'w=',F8.2,15x,'z0=',F8.2)
C
```

```
      if (z0 .lt. 50.) w=w+10.
      if (z0 .lt. 50.) go to 500
      write (20,700) s,w,z0
C
      s=s+10.
      w=w0
      if (s .gt. 200.) go to 900
      go to 500
C
900   CONTINUE
      END
```