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The Design Guide For CMOS-On-SIMOX Test Chips NIST3 and NIST4

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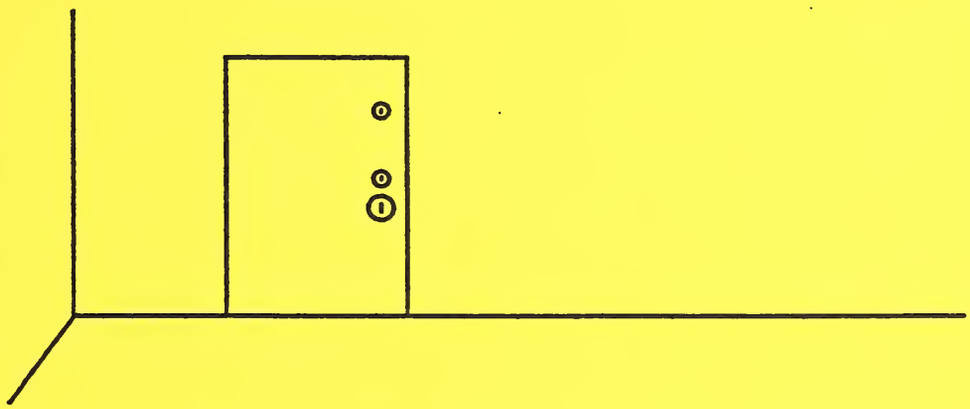

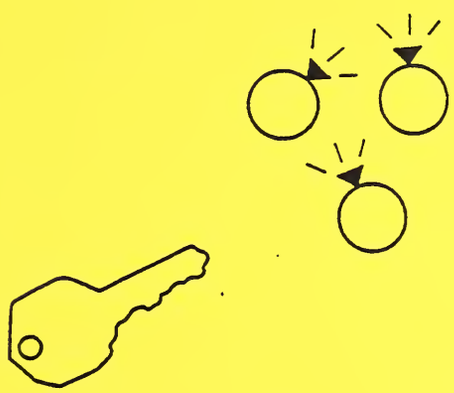

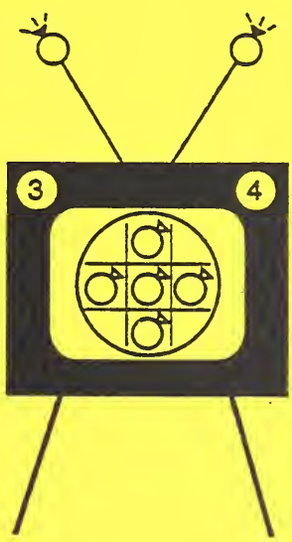

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THE DESIGN GUIDE FOR CMOS-ON-SIMOX TEST CHIPS NIST3 and NIST4

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ABSTRACT

The design guidelines for test chips NIST3 and NIST4 are specified in this manual. These chips were designed for process monitoring and device parameter extraction for a CMOS (Complementary Metal-Oxide-Semiconductor)-on-SOI (Silicon-On-Insulator) process. The chips contain structures which are common to a standard CMOS process as well as structures specifically designed for a SIMOX (Separation by the IMplantation of OXygen) process. In order to facilitate the CAD process, a unique "technology file" was created for the Magic VLSI layout editor used on a Sun-3/280 system running Sun Version 3.5. This SIMOX technology file is very general and can be used to build CMOS as well as SIMOX chips.

NIST3 is 6380 μm $\times$ 4780 μm and contains several large-geometry MOSFETs, resistors, and capacitors. NIST4 is 1 cm $\times$ 1 cm and contains approximately 300 small-geometry test structures. The SIMOX specific structures found on these chips include MOSFETs, capacitors, interconnects, and pads to be discussed in more detail.

The test guide for the test structures on NIST3 and NIST4 is included in a separate manual [1].

Key words: CAD; Magic; MOSFET; NIST3; NIST4; SIMOX; SOI; test chip; test structure

1. INTRODUCTION

The design of test chips NIST3 and NIST4 has been developed for a SIMOX (Separation by the IMplantation of OXygen) process. This design can be used to monitor or evaluate different SIMOX processes. Since SIMOX is a relatively new technology, new or modified test structures are needed to obtain the process and device parameters. These chips were designed for process monitoring and device parameter extraction. NIST3 contains several large-geometry MOSFETs, resistors, and capacitors and NIST4 contains approximately 300 small-geometry test structures. The SIMOX specific structures found on these chips include MOSFETs (metal-oxide-semiconductor field-effect transistors), capacitors, interconnects, and pads. Test procedures for these test chips can be found in ref. [1].

A unique "technology file" was created for the CAD graphic layout editor Magic* [2], the VLSI layout editor used on a Sun-3/280 system running Sun Version 3.5. This SIMOX technology file is very general and can be used to build CMOS as well as SIMOX chips. It is assumed that the reader is already familiar with Magic, CAD techniques, and the fundamentals of SIMOX processing.

In this report, section 2 presents a brief overview of the SIMOX process. SIMOX design considerations for NIST3 and NIST4 are discussed in section 3. Sections 4 and 5 describe the design rules, and technology file changes and Magic installation, respectively. The organization of NIST4 is discussed in section 6 along with CAD organizational specifics. Section 7 describes how NIST3 was built, and section 8 discusses outputting the data for mask generation. Appendices A through C present the ten SIMOX processing steps, the SIMOX design rules, and the SIMOX technology file, respectively. Appendix D presents the Magic layers, CIF (Caltech Intermediate Form) names and Calma numbers associated with the SIMOX masks, and Appendix E contains the computer program to determine the dimensions for the rf transistors.

The tables and figures in this report are arranged to provide a quick reference. The tables and figures associated with NIST4 are given first, followed by the tables and figures for NIST3. NIST4 is shown in figure 1, followed by the key to the shading in figure 2. Table 1 lists the structures found according to their general vicinity in the four parts comprising NIST4. Figures 3, 4, 5, and 6 illustrate Parts I, II, III, and IV, respectively. Table 2 lists the basic structures found on NIST4 and the parameters measured. The basic structures found on NIST4 are illustrated in figures 7 through 29. Additional test structure information is given in table 3.

NIST3 is shown in figure 30 followed by its cell structure in figure 31. The test structure list is given in table 4.

For completeness, some of the sections found in the testing manual [1] are included in this design guide.

2. THE SIMOX PROCESS

The mask set was designed for positive photoresist and subtractive etching. Positive photoresist is initially crosslinked, and exposure to UV light to areas selected by the masks breaks this crosslinking, enabling the exposed photoresist to be removed by an alkaline-aqueous developer. Since only positive photoresist is used, some masks are clear field while others are dark field. The dark areas on the mask do not allow UV light to penetrate. In general, for any features with layer height (i.e., island, polysilicon, and metal), everything but the feature needs to be etched; therefore, a clear field mask is needed. For the other

* In this paper commercial equipment, instruments, and computer programs are identified to specify adequately the procedure. This does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment or program is the best available for the purpose.

features, where the photoresist and/or SiO_2, glass, or passivation needs to be etched away, thus creating a "hole" for a contact or an area in which to implant a dopant, a dark field mask is needed.

The masks were made by the mask vendor from a tape of the digitized features. The masks must be specified to the mask vendor as clear field or dark field. Dark field masks imply the features defined in Magic are clear with an opaque background. Conversely, clear field masks imply the features defined in Magic are opaque with a clear background. Below is a list of processing masks, in the order in which they are used, with the appropriate clear or dark fields (Appendix A contains the processing sideviews for these steps):

1. ISLAND (clear field mask)
2. NWELL (dark field mask)
3. PWELL (dark field mask)
4. POLYSILICON (clear field mask)
5. NDIFFUSION (dark field mask)
6. SUBSTRATE CONTACT (dark field mask)
7. PDIFFUSION (dark field mask)
8. SUBSTRATE CONTACT (dark field mask)
   OTHER CONTACTS (dark field mask)
9. METAL (clear field mask)
10. GLASS (dark field mask)

The contact mask in Step 8 does not include the substrate contact cuts; therefore, the substrate contact mask must be reused to expose these regions.

The distinction between locos and mesa isolation is mainly determined by the process sequence, not by the mask polarity. The island mask for a mesa process is similar, yet not equivalent, to the active area mask in a locos process.

In SIMOX processing, the implanted, annealed film does not retain the initial substrate doping level after the high-temperature anneal. The substrate should be lightly doped (in this case, the substrate is p-type) to minimize capacitive coupling, while the scaling rules for submicrometer MOSFETs dictate relatively high-channel doping. Therefore, the mask set is designed to use four implants with the following Magic names: nwell, pwell, ndiffusion, and pdiffusion. The polysilicon gates and interconnects are doped n^{++} by $POCl_3$ (phosphorus oxychloride) annealing. N-channel MOSFETs have a p^- implant in the channel area (which Magic calls pwell) with an n^+ source/drain implant (which Magic calls ndiffusion), while the p-channel MOSFETs have an n^- implant in the channel area (nwell) with a p^+ source/drain implant (pdiffusion).

3. THE SIMOX DESIGN

3.1 The Twin Tub Approach

NIST3 and NIST4 were designed for a "twin tub" process. There were two reasons for this

approach.

CMOS design is more versatile when a twin tub device layout is used. Regardless of the actual process being used (i.e., *n*-well, *p*-well, or twin tub), the design does not need to be changed. Using a twin tub design, the appropriate CIF layers can be deleted, resulting in a single tub circuit implementation. When sending a CIF file to the mask vendor, the cifoutput section of the technology file can be changed to reflect the appropriate layers, the output CIF file can be edited to delete the appropriate layers, or the mask vendor can ignore unwanted layers.

In SIMOX, the design should be treated like a twin tub CMOS on SIMOX process. In SIMOX, the tubs are not used for isolation; rather, the tub implant is used as the channel threshold-adjust implant. Separate channel implants are required for the *n*- and *p*-channel transistors.

3.2 The Island and Substrate Contact

The main difference between the CMOS and SIMOX design is the addition of the island (called "island" in the technology file) and substrate contact (called "subcon") in the technology file to create the SIMOX process. In the SIMOX technology, the island is not equated with the "active area" defined by Magic. In CMOS, the active area includes ndiffusion, ndiffusion contact, pdiffusion, pdiffusion contact, nfet, pfet, nwell contact, pwell contact, and the appropriate bloats and shrinks. Also, the active area layer which is created for the CMOS process in the cifoutput section of the technology file from the existing designed areas is not used in the SIMOX processing. In SIMOX, the islands include the nwell and pwell. Also, the dimensions of the island with respect to these features are optimized using a separate island layer for increased versatility. A separate island contact is also useful for selected test structure purposes.

The designed SIMOX layers are equivalent to designed CMOS layers with the addition of an island and substrate contact. The island includes the wells, and for isolation purposes, one well per island and one device per well were chosen.

On test chip NIST4, the well edges were made coincident with the island edges on all but one side. On this one side, the island edge extends 1 μm. This is intended to eliminate ambiguity caused by coincident edges during inspection.

The substrate contacts are located in regions between the islands. The SIMOX substrates are assumed to be lightly doped (10 to 30 Ω-cm) *p*-type. To make a good substrate contact, the substrate is doped with pdiffusion before depositing the metal. Therefore, all substrate contacts are designed with pdiffusion encompassing them.

3.3 SIMOX MOSFET Design

Two MOSFET variations of design in SIMOX are included on NIST4. The difference between the two approaches is the placement of the "well" contact.

The approach used in Columns 1 and 2 (and illustrated in figs. 7 and 8) is similar to CMOS designs, and the other approach is demonstrated in Columns 11 and 12 (and illustrated in fig. 19) which is more characteristic of the SIMOX process. This second approach more accurately treats the "well" contacts as contacts to the channel of the MOSFET. Since the height of the islands is only 0.1 to 0.3 μm, the ndiffusion and pdiffusion used as sources and drains, for n-channel and p-channel MOSFETs, respectively, are not imbedded in the wells but are surrounded by them. Therefore, a "well" contact placed as close to the channel as possible is found in Columns 11 and 12.

All the MOSFETs have five terminals: source, drain, gate, well, and substrate. The MOSFETs were designed to be probed using a 2 by 10 probe card. Therefore, contact to the substrate is possible for each MOSFET even though the substrate contact may not be directly next to the MOSFET being tested. As an example, figure 7 shows an n-channel SIMOX transistor in a p-well imbedded in an island.

3.4 Some Basic Design Concepts

Several concepts or guidelines were employed during the design. They are:

a. When possible, avoid crossing the island and polysilicon edges with metal or polysilicon. This is a difficult processing step; therefore, minimize any potential places for error.
b. Only put the island where it is needed. Do not place it under the interconnects.
c. Use the same contact size throughout the design because it is hard to optimize the process for more than one contact size.
d. Separate contacts by one contact spacing (before CIF). Avoid using rectangular contacts because the metal has a tendency to lift off these areas.
e. Use metal as an interconnect before polysilicon (due to the desirable lower resistance and capacitance-to-the-substrate of the metal).
f. Avoid using ndiffusion or pdiffusion as an interconnect.
g. Choose the shortest path for the interconnect between the islands while trying to minimize the number of contacts.
h. Avoid coincident edges amongst island, polysilicon, and metal.
i. Use metal2 and via in the pads in case the masks will be used in a bulk CMOS (MOSIS) process.

4. THE DESIGN RULES

Conservative design rules were used for designing NIST3 and NIST4 [1]. The design rules that were followed are given in Appendix B. These rules include a polysilicon width of 6 μm. This allowed for considerable overetch to occur and still have working parts. Also the ndiffusion contact (called ndc in the technology file) to n-channel MOSFET gate (nfet) and pdiffusion contact (pdc) to p-channel MOSFET gate (pfet) spacing rules were 2 μm apart.

After the design rules were chosen, the technology file was modified to reflect them. Therefore, any violations will be flagged interactively.

5. TECHNOLOGY FILE CHANGES FOR SIMOX AND MAGIC INSTALLATION

A new SIMOX "Technology File" was created and is listed in Appendix C. This file enables the full power of the Magic CAD system to be used in SIMOX design. A critical factor in the design of this test chip set was the ability of the technology file to create specific features such as island and substrate contacts common to SIMOX technology. The technology file assists the designer by allowing the CAD system to interpret the actual features being created and categorize them into layers for masks. Ten masks are used for this technology. (Appendix D gives the Magic layers, CIF name, and Calma number associated with the SIMOX masks.) The technology file also allows for design rule checking and circuit extraction for simulation using the event-driven switch level simulator called esim [2].

The SIMOX technology file was created by first simplifying and then modifying the CMOS technology file supplied with Magic. Starting with a working technology file, in the cifoutput and cifinput sections, all but the general twin tub (lambda=1.0) styles were deleted. Next, the keyword for each Magic layer was made consistent throughout the file.

In addition to the island (called island in the technology file) and substrate contact (called subcon) levels, the substrate layer (called substrate) was created. In Magic, contacts are defined as connecting two layers. Therefore, the substrate contact connects the substrate layer with the metal layer. The subcon is used for the CIF of the substrate contact; however, the CIF of the substrate layer is not needed.

Some processes are not double metal; therefore, metal2 and m2c (metal2 contact) are not always needed. However, these layers are included in the pads for compatibility with CMOS (MOSIS) processing.

On NIST4, closed-geometry MOSFETs were used to study the degree of leakage around the gate edge of a regular MOSFET. To design a closed-geometry MOSFET, a polysilicon-to-metal contact is needed on the gate of the MOSFET. The processing design rules usually do not allow this construction since the metal could spike through the polysilicon, leaving a device with a gate-to-channel short. Any such structures are modified and flagged as an error in the current CMOS technology file. A modification of the technology file allowed for these structures, thereby giving the processing line the option of improving the process using this mask set. The ndpc (ndiffusion under polycontact) and pdpc (pdiffusion under polycontact) Magic layers were created for this purpose.

In Magic, the number of planes is minimized to improve the speed of operation of the CAD system when dealing with very complex chips. Due to the additional layers, the number of planes was changed from 8 to 10. To do this, an editor was used to change the MAXPLANES assignment statement in /usr/cad/src/magic/database/database.h and

/usr/cad/src/magic/include/database.h. Once this change was made, "make install" in the /usr/cad/src/magic/database/database.h directory was typed. Then, the default directory was assigned to be /usr/cad/src/magic, and "make magic" was typed. Since no errors were found, a new runnable version of Magic was in /usr/cad/src/magic/magic. The executable file "magic" was then copied to the directory /usr/cad/bin/magic.

The above procedure needs to be followed when installing this technology file due to its additional two planes. In addition to the above installation procedure for this technology file and for the installation of any new technology file, the default directory is changed to /usr/cad/src/magic/tech. Then, the new technology file is copied to this directory and its owner changed to 500 by typing "chown 500 simox.tech". This new technology file is then installed by typing ":techinstall simox.tech 20 /usr/cad/lib/magic/sys" [2].

6. NIST4

6.1 The General Architecture

The general architecture of NIST4 consists of four parts. The first part is the left side of the central area of figure 1 and is detailed in figure 3. It has twelve columns (2 pads wide) of four placements of 2 by 10 pads on 160-μm centers. These provide access to elemental active devices, inverters, and dc parametric test structures. An extra row of substrate contact test structures is included in the columns to assure contact to the substrate for each probe card placement. The right side of the central area has three columns of four 2 by 10 pad placements for circuits and their elemental parts. These Part-II structures are shown in figure 4. Again, an extra row of substrate contact test structures is included in the columns.

On the chip, the first and second parts of the design are surrounded by the third and fourth parts. Both occupy a flange about 1.6 mm wide which makes the composite layout consistent with a total step-and-repeat distance of 1 cm (not including the separation between chips). The size of the test chips was actually determined by the number, size, and spacing of the bondable pads required for each chip as well as the number of test chips possible per wafer given their size. The Part-III structures (shown in fig. 5) include the transistors connected to bondable pads for radiation studies. The Part-IV structures (shown in fig. 6) comprise the area between the bonded transistors and the core area. This area is used for systematic variations of new test structures. On NIST4, this area includes transistors padded out to be compatible with rf-probe cards for on-wafer rf testing.

The structures found on NIST4 are listed in table 2.

6.2 The Part-I Structures

6.2.1 The organization of the structures into the layout

The test structures in Part I were designed to be probed with 2 by 10 probes using 80-μm square probe pads on 160-μm centers. The test structures were organized on a column-

by-column basis as follows:

Column 1	18 n-channel MOSFETs with different channel lengths/widths and with the channel contact beside the drain
2	18 p-channel MOSFETs with different channel lengths/widths and with the channel contact beside the drain
3	9 cross-bridge resistors
4	10 inverters with different channel lengths
5	16 contact resistors
6	12 contact resistors
7	10 island-edge and other meanders
8	20 capacitors
9	20 capacitors
10	18 specially-sized (fat-FET, big square, etc.) MOSFETs
11	Repeat Column 1 (with channel contact near the channel)
12	Repeat Column 2 (with channel contact near the channel)

The rationale behind Columns 11 and 12 is to enable active transistor parameter mapping when used in conjunction with Columns 1 and 2 and to explore a design variation regarding channel (well) contact placement.

Metal numbers were placed near the test structures identifying the channel lengths and widths to facilitate optical and SEM inspection.

In order to minimize layout confusion, these guidelines were followed:

(a) Do a detailed design check of the first cell for each column.

(b) Determine the number of structures/column given the number of available pads/column and the need for substrate contacts at least every 10 pads. (Add substrate contacts to fill up partially filled columns unless there is room for another structure.)

(c) Determine the critical dimension(s) or feature(s) per structure in the column and an appropriate identifying name for each cell. Order these in such a way as to make the design work easy (i.e., changing one dimension at a time). The general order from top to bottom of the test structures that merely change the material used is similar to the construction from top to bottom of a dissected structure, namely:
   (1) Metal2 (optional)
   (2) Metal1
   (3) Polysilicon
   (4) Ndiffusion (n^+ source/drain) – always before pdiffusion
   (5) Pdiffusion (p^+ source/drain)
   (6) Nwell (channel implant for p-channel MOSFETs) – always before pwell
   (7) Pwell (channel implant for n-channel MOSFETs)
   (8) Island

   If contacts are considered, the order would be:

(a.) Metal2-to-metal1 contact (optional)
(b.) Polysilicon contact
(c.) Ndiffusion contact
(d.) Pdiffusion contact
(e.) Nwell contact
(f.) Pwell contact
(g.) Island contact
(h.) Substrate contact

6.2.2 CAD system setup

A new directory was created for NIST4 and all its cells. This directory is called nist4 and the main file is called nist4.mag.

NIST4 was blocked out by setting up a skeletal structure for Part I, Columns 1 through 12, by placing 80- by 80-μm^2 metal pads on 160-μm centers. A 200-μm wide pdiffusion structure was then put around these pads such that the outer box dimension of the chip was 1 cm. Pdiffusion was chosen because this level has no layer height in the processing, and its color on the Sun is brown, which clearly marks the edge. This was all done in the main file. Then the structures were built in individual cells, placed and spaced according to the existing metal pads, and after it was built, the metal pads that were used for spacing were deleted.

A cell consisting of four probe pads placed appropriately was always used as the starting point for each design since a probe pad takes some time to build given its hierarchical structure of island, polysilicon, polycontact, metal1, and glass. The metal2 and via layers were added to these layers later in the main file once it was decided to convert this SIMOX design to CMOS. This was easily done using the macro command to select the glass layer in the pads one at a time and to paint the metal2 and via layers on top. "Grows" and "shrinks" were then performed on the CIF of the metal2 and via layers to obtain reasonable dimensions given the fact that probe pads and bond pads were being considered simultaneously.

The bond pads and contact pads for both test chips were designed as a composite structure of glass, metal, polysilicon contact, polysilicon, and island. The polysilicon level was included to add extra strength to the pads for multiple probing purposes. The polysilicon contact enables the designer to interface the test structures with the pad in polysilicon as well as metal without using an extra contact. The island level was included to minimize capacitive coupling to the substrate.

The bond pads are located around the periphery of both chips, and the contact pads are in the center of NIST4 organized such that a 2 by 10 probe card can be used. The center of the contact pads are 160 μm apart. The dimensions for these pads (after CIF) are:

(a) Island (120 $\times$ 120 μm)
(b) Polysilicon (100 $\times$ 100 μm)

(c) Polysilicon contact (76 × 76 μm)
(d) Metal1 (80 × 80 μm)
(e) Via (72 × 72 μm)
(f) Metal2 (76 × 76 μm)
(g) Glass (70 × 70 μm)

The island level was made small enough to allow for test structures between the pads. This level can still be made smaller considering the amount of overetch associated with the polysilicon layer.

The bonding pads are considerably larger to allow room for bonding. Their dimensions (after CIF) are:

(a) Island (180 × 180 μm)
(b) Polysilicon (160 × 160 μm)
(c) Polysilicon contact (136 × 136 μm)
(d) Metal1 (140 × 140 μm)
(e) Via (102 × 102 μm)
(f) Metal2 (106 × 106 μm)
(g) Glass (100 × 100 μm)

The island level in the bonding pads is 200 μm away from the edge of the chip, a lenient spacing for the bonding process which requires at least 100 μm.

Assuming a 2 by 10 probe card will be used to test the devices, a substrate contact is needed at least every 10 pads so that for every test structure a contact to the substrate is possible. Therefore, a cell containing a substrate contact was created and used multiple times.

When observing a test structure through a microscope, it is difficult to identify the critical dimensions. By labeling the test structures in metal with the critical dimension, these dimensions can then be read through a microscope. Cells named zero.mag through nine.mag were created using metal in the shape of the appropriate number, combined as needed, and placed between the pads of the pertinent structure in the main file. This was done after all the cells were placed.

Placing the numbers inside each cell, as opposed to inside the main file as mentioned above, has additional advantages. For example, it would be easier to relocate the test structures. One cell can be selected and moved, as opposed to two or three. Since the original architecture was adhered to, the shuffling around of test structures was minimized. Also the identifying marks were included after all the cells were placed to further minimize any reshuffling.

6.2.3 Predesign work

The design rules and conventions (e.g., pad construction) must be established as firmly as

possible at this point. These design rules can then be placed in the technology file to flag any errors interactively.

While designing, a record was kept of where and what the smallest design feature sizes were for each CIF layer (the mask vendor needs this information). A separate record was kept of the smallest actual dimension used in the design rule test areas. It was easier to keep track of this information while designing as opposed to finding these features later.

In addition to test structures, each chip includes the following:

(a) Chip logo in metal (because it is easy to see through a microscope) created in the main file
(b) Date design complete in metal created in the main file
(c) Alignment marks (for clear field masks and dark field masks) designed with respect to the island since this is the first level and it has processing "height." These alignment marks should be located in the upper left-hand corner of the chip. This makes the orientation of the masks easy during processing.
(d) Mask identifiers for each level located in the upper left-hand corner. (On NIST4 these are located in the right central area due to space constraints in the upper left-hand corner.)
(e) Any structures required during fabrication should be put in the upper left-hand corner (e.g., the chevrons). (On NIST4 these were located in the right central area due to space constraints in the upper left-hand corner.)

At this point, the following was prepared:

(a) An installed technology file.
(b) A paper describing the architecture of the chip.
(c) The names of the future cells in each column.
(d) The agreed-upon design rules and design conventions.
(e) A sheet of paper on which to write the location and dimension of the smallest design feature size for each layer. (If the design rules are being tested, note the smallest actual dimension as well with their corresponding locations.)
(f) A skeletal pad placement in the main file with surrounding pdiffusion.
(g) A cell with a substrate contact connected to a pad.
(h) Cells named zero.mag through nine.mag with the numbers in them designed in metal of the appropriate height to fit nicely between two pads.
(i) The above-mentioned structures that are used for every chip (i.e., logo, alignment marks, etc.) roughly placed in the upper left-hand corner of the main file.
(j) A scratch cell containing four probe pads spaced appropriately.

With the above completed, the design proceeded.

6.2.4 The one-cell-per-column approach

Using the scratch cell containing the four probe pads, the first structure in Column 1 was

designed following the design rules and design conventions. The resulting cell was saved under a preselected name.

Starting again with the same scratch cell, the first structure in another column was designed and stored under the agreed-upon name. This procedure was continued until the first structure in each column was designed.

The design of these structures was then approved by the design team, or a portion thereof, before continuing. Below is a review of the basic design concepts for the devices not yet considered:

a. Cross-bridge resistors (Column 3)

An example of a cross-bridge resistor [3] in polysilicon is given in figure 9. Other materials can be used for the cross-bridge resistor such as metal2, metal1, nfet, pfet, ndiffusion, pdiffusion, nwell, pwell, and island. To make these other varieties, the polysilicon would be replaced with the appropriate material, and this material would be connected to the pads with metal1 using the appropriate contact (if needed). The diffusions and wells require the presence of the island layer in which to implant the dopants. The cross-bridge resistors were constructed with the same layers as would appear in an integrated circuit. For example, the opposite well with the diffusion cross-bridge resistors was included to simulate realistic device properties.

From the van der Pauw [3] cross in the cross-bridge resistor, one determines the sheet resistance of the material using the formula:

$$R_s(\Omega/\square) = \frac{\pi \times f \times V}{I \times ln2}, \tag{1}$$

where I is the current forced, V is the voltage difference, and f is a correction factor (approximately one) that is related to the geometrical asymmetry of the structure. By repeating the measurements, reversing the current direction, and rotating the contacts by 90 deg, one can determine the effects of geometrical asymmetry, measurement voltage offsets, and Joule heating on the measurement.

From the bridge, the effective electrical linewidth (W_e) is calculated from the measurements and the sheet resistance using the formula:

$$W_e(\mu m) = \frac{R_s \times L_m \times I}{V}, \tag{2}$$

where R_s is the sheet resistance from (1), L_m is the design length between the bridge voltage taps (this dimension can be designed between 80 and 200 μm with negligible effect on the results), I is the current forced, and V is the voltage difference.

Effective linewidth, W_e, can also be expressed as:

$$W_e = W_m + ax_j \pm W_o, \tag{3}$$

where W_m is the designed photomask dimension, ax_j is the increase in width due to lateral diffusion for the implanted cross-bridges (note: $ax_j = 0$ for all other bridges), and W_o is the width offset due to the over or under etching in the photolithographic process.

All bridges on NIST4 are designed with $W_m = 10$ μm and $L_m = 130$ μm. When the bridge is rotated 90 deg, another linewidth measurement is possible from this orientation. The e-beam machine used to print the masks divides the masks into sections and works on a section at a time. When working on a section, the e-beam travels in the x-direction after fine increments are made in the y-direction. Therefore, the linewidths on the masks may be different in the x- and y-directions, causing different linewidth results depending on the orientation.

b. Inverters (Column 4)

Inverters [4] with different channel lengths are included in this column. An example of one with channel lengths of 4 μm is given in figure 10. These inverters consist of an n-channel MOSFET and a p-channel MOSFET with twice the channel width but same channel length as the n-channel MOSFET. The design for these MOSFETs is similar to the ones in Columns 1 and 2.

Each MOSFET is on a separate island. The gates of the two MOSFETs are connected in polysilicon to form the input node, the drains are connected together to form the output node, the source of the n-channel MOSFET is connected to V_{SS}, and the source of the p-channel MOSFET is connected to V_{CC}. There is a substrate contact in the vicinity.

The only dimension that is changed in this structure throughout the column is the channel length.

c. Contact resistors (Columns 5 and 6)

Three types of contact resistors are included on NIST4. The first is the standard four-pad contact resistance structure (fig. 12) [5], the second is the Kelvin chain (fig. 13), and the third is a six-pad contact resistance structure (fig. 11).

For the four-pad contact resistance structure, the measured interfacial contact resistance is:

$$R_i = \frac{V_2 - V_1}{I}, \tag{4}$$

where the voltage taps are perpendicular to the direction of the current flow from one material, through the contact, to the next material. Interfacial contact resistance is an important parameter used in determining the performance of the fabrication process. The interfacial contact resistance is inversely proportional to the contact window area if the interfacial layer is uniform. Therefore, from plots of R_i versus contact area, one can ascertain approximate interfacial contact resistance values for all contact window sizes. These plots can be made from the measurements taken from strategically sized test structures in these columns.

For the Kelvin chain, the minimum design rules were used. From this chain, a measurement of the front contact resistance (not to be confused with the interfacial contact resistance) is possible using:

$$R_f = \frac{V_1 - V_2}{nI}, \tag{5}$$

where n = the number of contacts. Here, the voltage taps are at 90 deg to the direction of the current flow. This parameter is important for simulating circuit performance.

The six-pad contact resistance structure is similar to the four-pad contact resistance structure but is more versatile. In addition to measuring the interfacial contact resistance, the "end" contact resistance is obtained from which the "front" contact resistance is calculated. This structure and its measurement method were designed to minimize the effect of parasitic resistances and contact misalignments on the result.

d. Island-edge and other meanders (Column 7)

Polysilicon and metal are used as interconnects; therefore, they travel across the island lip. As a result, the polysilicon or metal may break at these locations. Several test structures were included to test the integrity of the polysilicon (fig. 14) and metal as they meander over island edges [6]. These are relatively small test structures. Metal atop polysilicon which meanders across the island edge are structures that are also included on NIST4 (fig. 15).

e. Capacitors (Columns 8 and 9)

The dimensions of the SIMOX structure preclude normal gate oxide capacitance measurements. The capacitance of the full gate-oxide-silicon-oxide-silicon structure has been simulated [7] under the assumption that the silicon film is completely isolated. Capacitors which meet these boundary conditions were included.

Figures 16, 17, and 18 show three capacitors which were designed for NIST4. Columns 8 and 9 include other capacitors [4], as well, from which to measure the capacitance between the various layers.

The capacitance is calculated using the formula:

$$C = \frac{\epsilon \times A}{d}, \tag{6}$$

where ϵ is the dielectric constant of the insulator, A is the area of the capacitor (i.e., the area of the smallest electrode), and d is the distance between the electrodes. The capacitors on NIST4 were designed to utilize as much area as possible inside a set of four probe pads.

6.2.5 The columns

NIST4 consists of four parts, the first part of which has twelve columns (2 pads wide) of four placements of 2 by 10 pads on 160-μm centers. These provide access to elemental active devices, inverters, and dc parametric test structures. An extra row of substrate contact test structures is included in the columns to assure contact to the substrate for each probe card placement.

The Part-I structures were 80% complete once there was one design for each column. It was relatively easy to fill in the columns. The first structure in Column 1 is an n-channel MOSFET (L=2 μm, W=6 μm) and the next structures use L=3, 4, 5 μm, etc. To complete this design task, the following steps were followed:

(a) Entered the first cell
(b) Changed the critical dimension
(c) Saved it under its new name
(d) Changed the critical dimension to make the third structure
(e) Saved it under its new name
(f) Continued until the column was complete
(g) Quit the file being edited so as not to modify the design of the first cell in the column
(h) Entered the main file (nist4.mag) and placed the structures (Now whenever an already designed cell is edited, the original placement will be preserved in the main file, as long as the main file is saved using "writeall.")

Using this procedure, it was not necessary to draw each structure individually, which saved a lot of time.

To make a p-channel MOSFET similar to an existing n-channel MOSFET, the following was done:

(a) Entered the pertinent n-channel MOSFET cell
(b) Selected the pwell
(c) Painted it nwell (This automatically changes all the appropriate layers such that the n-channel MOSFET becomes a p-channel MOSFET. The reverse can be done also.)

(d) Saved it, using an appropriate p-channel MOSFET cellname.

This was done for the first cell in the column of p-channel MOSFETs; however, it was faster once the initial one was designed to change its critical dimension to make the next cell, and so on. Entering and leaving Magic takes time, so this time was minimized by taking this approach.

Once the initial n-channel MOSFET design was complete, the remainder of Columns 1 and 2 was done in less than 15 minutes.

The other columns were designed using the above approach and similar short cuts. The appropriate person or persons approved each designed column.

6.3 The Part-II Structures

Once the Part-I structures were complete, the dynamic structures were designed in Part II. The following dynamic test structures were chosen:

(a) A 23-stage ring oscillator with NAND gate start-up circuitry
(b) A 4-stage output amplifier
(c) A NAND gate
(d) A 23-stage ring oscillator with output amplifier and NAND gate start-up circuitry
(e) A ring oscillator with a fanout of 2 and an output amplifier
(f) A 20-stage shift register
(g) A static RAM cell with the associated input and output circuitry
(h) Pieces of the larger dynamic structures (included in Column 13)
    (1) Inverters with the same dimensions as in the ring oscillators
    (2) N-channel MOSFETs of the same dimensions as in the dynamic integrated circuits
    (3) P-channel MOSFETs of the same dimensions as in the dynamic integrated circuits

These structures were designed in parts and then combined. For example, an inverter (with the minimum dimensions and using $W_p = 2 \times W_n$) was built, and this stage was repeatedly copied until the desired odd number of stages was obtained. The design rule for island isolation was followed when connecting the output of one inverter to the input of the next. This became the original ring oscillator. The components comprising the ring oscillator are pinned out separately in Column 13. These include the n-channel MOSFET, p-channel MOSFET, and inverter.

For the ring oscillators which included output amplifiers with four stages of inverters, the minimum dimensions were used in the first stage of the output buffer. Therefore, the inverter dimensions in the actual ring oscillator were made larger than the first stage of the output amplifier by a factor of 8 to minimize the loading of the output amplifier on the node of the ring oscillator. The channel widths in each successive stage in the output buffer were increased by a factor of 2 for design ease. This output amplifier was pinned

out separately and placed in Column 14.

For the ring oscillators with NAND gate start-up circuitry (as in fig. 21), the NAND gate was added in the place of an existing inverter and the dimensions $W_p = 2 \times W_n$ were used. This NAND gate is also pinned out separately and placed in Column 14.

A two-phase shift register was built (fig. 22). It consists of 20 inverters, each separated by a passgate whose gates are alternately connected to one of the two clocks. The last stage is connected to an output amplifier.

The dynamic integrated circuits on this chip were simulated on the CAD system using esim [2]. These simulations are fast, interactive, and ensure continuity of the circuit. These simulations also assure the designer that the circuit is hooked up properly (i.e., the correct number of stages) and that the device sizes are sufficient. For more accurate and detailed simulations, especially in the time domain, they can be simulated using SPICE3; however, for the dynamic circuits chosen for NIST4, the simulations using esim are sufficient.

All of the dynamic test structures above were successfully simulated using esim. A six-transistor static RAM cell (fig. 23) was also designed and simulated. However, the simulations showed that it could not overwrite the existing data. This demonstrated that several device sizes needed modification, and a new approach to rewriting the cell was initiated. A circuit diagram of the resulting cell is given in figure 24 along with the pertinent information to read and write the data in the cell.

All the above-mentioned dynamic test structures were designed using L=6 μm and placed in Column 14. Column 15 was made by modifying each structure in Column 14 to make L=4 μm and placing it in Column 15.

6.4 The Part-III Structures

Part III was started after the central area was complete. Part III includes the following transistors to be bonded:

(a) The standard n-channel (fig. 25) and p-channel MOSFETs
(b) Closed-geometry n-channel and p-channel MOSFETs (fig. 27) to determine the degree of gate peripheral leakage
(c) Many-fingered n-channel and p-channel MOSFETs (fig. 26) to determine the degree of gate peripheral leakage

Using the design rules for bond pads, two bond pads were created in a scratch cell. This cell was then duplicated and rotated around the periphery of the chip to help in cell placement and to determine the number of pads available for bonded MOSFETs. The bond pads along the top and left-hand edges of the chip are for n-channel MOSFETs, and the bond pads along the bottom and right-hand edges of the chip are for p-channel MOSFETs. A cell containing one bond pad connected to one substrate contact was created and placed appropriately around the edge of the chip such that each MOSFET would have

one substrate contact next to it.

Given the number of pads available for MOSFETs, their channel lengths and widths were chosen, as were their cell names.

An n-channel MOSFET was designed starting from the cell consisting of two bond pads which was then expanded to four pads. The other n-channel MOSFETs as well as p-channel MOSFETs were rapidly designed from this structure, keeping in mind the orientation of the pads.

These cells were then placed in the main file using the cell consisting of two bond pads as a placement guide. The unneeded cells were then deleted.

6.5 The Part-IV Structures

Space along the top of the chip and bottom of the chip (inside the bond pads) remains for the rf transistors, the Part-IV structures. The n-channel rf transistors (fig. 28) are located in the top section, and the p-channel rf transistors (fig. 29) are located in the bottom section.

The metal input terminals for these transistors were designed to provide an approximate 50-Ω input impedance to minimize reflections [8]. Computer simulations were performed on a VAX VMS 11/780 to select the optimum dimensions using the program in Appendix E. This program uses a simple model that does not account for a multilayer media such as is used here; therefore, variations in the results are expected. After several simulations, it was apparent that by designing three rf transistors, each with a different spacing (± 10 μm with respect to the spacing required to achieve a 50-Ω input impedance), the near-correct spacing could be determined by measuring the reflected rf signal. The tapering of this spacing toward the device was done in 1-μm steps at a 45-deg angle to minimize reflections.

There are three rows of n-channel MOSFETs in the top section and three rows of p-channel MOSFETs in the bottom section. The first row in both sections uses a "50-Ω" pad spacing of 50 μm, the second row uses 60 μm, and the third row uses 70 μm. The channel length varies as one traverses each row.

Six pads are used for each rf transistor; however, well and substrate connections are not available.

6.6 The Final Steps

Now that the test chip contained the test structures all placed in the main file, the following tasks remained:

(a) The placement of the alignment marks, chevrons, level identifiers, and NIST4 logo was checked. These structures were placed in the upper left-hand corner of the chip, space permitting.

(b) The cells were labeled with identifying marks.
(c) The placement pads were deleted.
(d) The final date was added in metal to the main file.
(e) A "writeall" was done.
(f) The final check was performed.
(g) The file was CIFed using the correct ostyle.
(h) The files were backed up on tape.

The test chips NIST3 and NIST4 will reside on the same wafer. One tape containing the CIF files of these two chips was sent to the mask vendor. This is discussed in a later section.

7. BUILDING NIST3

NIST3 consists of a small number of relatively large test structures. These structures are designed to be probed by a combination of electrical and physical techniques. Therefore, all these devices are connected to bondable pads. These structures along with their critical dimensions and cell names are given in table 4.

A MOSFET and capacitor were copied from NIST4 to be used as building blocks for NIST3 devices. These structures were then modified to reflect the specified measurements. The bonding pads were designed and placed around the periphery of the chip according to the bonding criteria. The cells were individually loaded into the main file using the Magic command ":getcell".

The interdigitated MOSFETs (L=10 μm, W=7 $\times$ 1500 μm) with seven fingers are for easy SEM cross section observation and direct CV measurement of gate-to-drain capacitance. They were designed using large rectangular contacts as opposed to the conventional square contacts. This is to ensure a view of the contacts when the devices are cross-sectioned.

Large square transistors are included on this test chip for charge pumping experiments as well as length/width studies.

Two different varieties of capacitors (500 μm $\times$ 500 μm) were designed. One is designed to measure the gate oxide capacitance, and the other, to measure the capacitance of the buried oxide.

A bipolar structure was read onto the Sun from a CIF tape and modified to be SIMOX compatible using the design rules. It is an experimental silicon magnetotransistor.

Once the chip was laid out, the alignment marks and the NIST3 logo were added.

8. THE DATA OUTPUT

8.1 The SIMOX CIF Layers

The mask fabricators require the CIF information associated with each mask. Thus there is a CIF name for each of these masks. These ten CIF names are given in Appendix C. They are similar to the CMOS CIF names except they begin with an 'S' as opposed to a 'C'. Magic, however, has twenty layer names; therefore, there will be more than one Magic name associated with a CIF name.

In the technology file, the name allNwell has been defined as including the Magic layers nwell and nwc (nwell contact), allPwell includes pwell and pwc (pwell contact), etc. All of the Magic layers associated with the CIF name are included in the CIF. However, there are several Magic layers which are not included in the CIF. One is the substrate layer. It was created because in Magic the substrate contact needs a layer on which to contact the metal. The subcon is needed for the CIF of the substrate contact; however, the substrate layer is not a mask level.

Some processes are not double metal; therefore, metal2 and m2c(metal2 contact) are the other Magic layers that are not included in the CIF.

8.2 A SIMOX Design Converted to a CMOS Design

Converting the SIMOX design to CMOS was easily done by specifying the cifoutput style as mosis(SCE) and submitting it to MOSIS [9] as an SCE technology. Since this is a "twin tub" design, MOSIS will delete the appropriate "well" and doping to correspond with the processing line to be used. For example, if a pwell process (SCP) is used, the nwell CIF is ignored as well as the n-implant CIF. However, the n-implant is created by them to be the inverse of the p-implant.

All of the MOSIS runs are double metal. Therefore, metal2 and m2c are needed in the pads. If they are not included, there will be no possible contact to the pads even if glass contacts are specified. Therefore, it is recommended to design all pads with double metal whether it will be processed using a double metal process or not. It is easier to delete its CIF than to redesign the pads which could create errors.

MOSIS does their own bloats and shrinks because they use different processing lines, and they ensure that what is designed is what is received regardless of the processing line they choose.

The choice of lambda is not critical. Lambda has nothing to do with what is designed, i.e., no multiplication of the CIF will occur. If you choose lambda equal to 1.5, that means it will be submitted on a 3-μm processing run. If lambda equals 1.0, it will be submitted on a 2-μm processing run, and so on. If transistors are being designed with a small designed channel length, choose a small lambda (half its value) in order to get working

parts. Currently, their minimum lambda is 0.6 μm which is available upon demand. This means designed channel lengths of 1.2 μm.

The SIMOX CIF was converted to CMOS CIF by simply modifying the cifoutput section of the technology file. The first letter of the CIF names now begins with 'C' and corresponds with MOSIS CIF names. Also an active area layer was created in the CIF. This was done in Appendix C.

When SIMOX is converted to CMOS, several things appear unusual. First, where the subcon existed for a substrate contact in the SIMOX process, this area in CMOS is metal with an area of pdiffusion which has no purpose. Also, the bloats of the diffusion areas may appear unusual, but this is not critical because the dimensions of the active area are the critical dimensions.

8.3 The Tape for the Mask Vendor

Once NIST3 and NIST4 were completed, the CIF files associated with these two chips were created. To do this, the CIF output style was set using the Magic command ":cif ostyle mosis(SCE)" for MOSIS to manufacture the wafers. The Magic command ":cif ostyle photronix" was used to send it to the mask vendor. The CIF files were then made by typing the Magic command ":cif". This command makes a CIF file using the same filename as the root file but with a .cif extension. Since this was done for both NIST3 and NIST4, the two CIF files nist3.cif and nist4.cif, respectively, resulted.

The mask vendor accepts or prefers one of the following tape formats:

(a) A tar tape (done on the Sun),
(b) A VMS copy tape (done on the VAX), or
(c) A VMS backup tape (done on the VAX).

Since the mask vendor preferred a VMS backup tape, the Sun CIF files were transferred to the VAX. To do this transfer, the file transfer protocol (ftp) was used in the ASCII mode (typically the default mode). To do this from a Sun terminal, "ftp VAX" was typed where VAX is the node name for the VAX. When the "ftp" prompt appeared, "put filename.cif filename.cif" was typed. This transferred the CIF file from the default Sun directory to the owner's top level VAX directory.

Since the mask vendor preferred a VAX backup tape, the following command sequence (which was put in a command file) was used to get the nist3.cif and nist4.cif files onto tape:

```
$ set verify
$ allocate mta0:
$ initialize mta0: nist
$ mount/for/dens=1600 mta0: nist
$ backup/ver/log/rewind/density=1600/ignore=label *.cif mta0:nist3a4.bck
```

```
$ backup/rewind/ignore=label/list=lpa0:nist3a4.lst mta0:nist3a4.bck
$ dismount/nounload mta0:
$ deallocate mta0:
$ set noverify
```

The resulting tape was sent to the mask vendor along with mask specifications, to be discussed next.

8.4 Mask Specifications

The mask set for NIST3 and NIST4 (labeled on the mask as NIST3A4) was e-beam printed with a 0.25-μm spot size and stripe height of 512 and was guaranteed to print 2-μm features. There is a price difference between masks with 2-μm features and above and those with less than 2-μm features. The less expensive route was chosen since the design rules were not stringent with this test chip set even though there are some noncritical features that are less than 2 μm to test the design rules. For this work, the characteristics of the resulting masks are:

(a) It is a 1X master.
(b) The thickness of the glass is 0.090 in.
(c) Antireflective coating of 9 to 15 % is used.
(d) There is a registration tolerance of 0.5 μm with respect to the island layer to ensure that all 10 masks align. This layer was chosen since it is the first mask used in the processing sequence and since the processing alignment marks on NIST3 and NIST4 use island as the reference layer. Therefore, the total misalignment (mask and processing) is minimized if the island layer is the reference layer for both.

Along with a tape of the two CIF files, nist3.cif and nist4.cif, the mask vendor was sent critical dimension drawings of the smallest feature desired to have printed on each mask with directions on where to find these dimensions on the mask layout. The critical dimensions for these layers are:

(a) 6.0 μm for NWELL, PWELL, ISL, and GLASS,
(b) 4.0 μm for M1, CNT and SUBCNT,
(c) 3.0 μm for NDIFF and PDIFF, and
(d) 2.0 μm for POLY.

The smallest actual dimensions are:

(a) 6.0 μm for GLASS,
(b) 4.0 μm for CNT and SUBCNT, and
(c) 1.0 μm for NWELL, PWELL, ISL, M1, POLY, NDIFF, and PDIFF.

For simplicity, the mask vendor was given the list of masks listed in the order they appear in the cifoutput section of the technology file. This is the same order they appear in the resulting CIF file, namely, NWELL, PWELL, ISL, M1, POLY, NDIFF, PDIFF, CNT,

SUBCNT, GLASS. The clear field masks (or dark digitized areas) and their CIF names are ISL(SIL), M1(SMF), and POLY(SPG), and the dark field masks (or clear digitized areas) and their CIF names are NWELL(SWN), PWELL(SWP), NDIFF(SND), PDIFF(SPD), CNT(SCT), SUBCNT(SCS), and GLASS(SOG).

Clear scribe lines were chosen for all the clear field masks. These masks define features which have processing height. The metal in particular can damage the diamond-edged saw; therefore, these layers are not included in the scribe lines. Clear scribe lines are also used on the dark field masks. These masks are either implants or contact cuts which would facilitate the dicing of the wafer into die. Also, the clear scribe lines on the dark field masks facilitate the alignment process. The distance between test chips is 400 μm which is available for the "scribe lines." This is enough area to dice the wafer with a diamond-edged saw and guarantee working die.

Because both test chips, NIST3 and NIST4, were incorporated on the same mask set, a wafer layout map was sent along with a step-and-repeat dimension in the x- and y-directions (which includes a space of 400 μm between all test chips) and other key coordinates for them to duplicate the map. They also needed the lower left coordinates and upper right coordinates referred to in the CIF of NIST3 and NIST4. The top portion of the wafer consists of only NIST4. There are seven die in the x-direction and three die in the y-direction. NIST3 resides on the bottom portion of the wafer with 11 die in the x-direction and seven die in the y-direction. This arrangement of test chips helps conserve area.

As a final check, large plots of the digitized areas for NIST3 and NIST4, as the mask maker intended to print them, were received. These proved helpful and informative, both for the design team to check the levels and for the process team to determine critical areas for alignment purposes.

The goal is to receive masks which would help manufacture wafers with structures that look similar to what is seen on the Sun (with no inversions). Since chrome masks are printed with chrome side down, when viewed chrome side down, it is desired to see structures as designed on the Sun. To preserve the masks, they must be viewed through a microscope chrome side up so the structures would appear inverted. The masks are generally visually inspected (while in hand) chrome side up; therefore, it is good practice to specify to the mask vendor to insert the mask title on the mask to be read in this manner.

9. CONCLUSIONS

This manual contains the design guidelines for test chips NIST3 and NIST4. The thoughts behind the designed SIMOX test structures are included as well as the specifics of building these chips in a timely manner and submitting them to the mask vendor.

The technology file supplied with Magic was modified for the SIMOX process. With one design, the technology file can create a CIF or Calma file for a SIMOX process or a bulk CMOS (MOSIS) process. This technology file is in Appendix C.

For testing specifics, the testing guide [1] for NIST3 and NIST4 should be consulted.

10. ACKNOWLEDGMENTS

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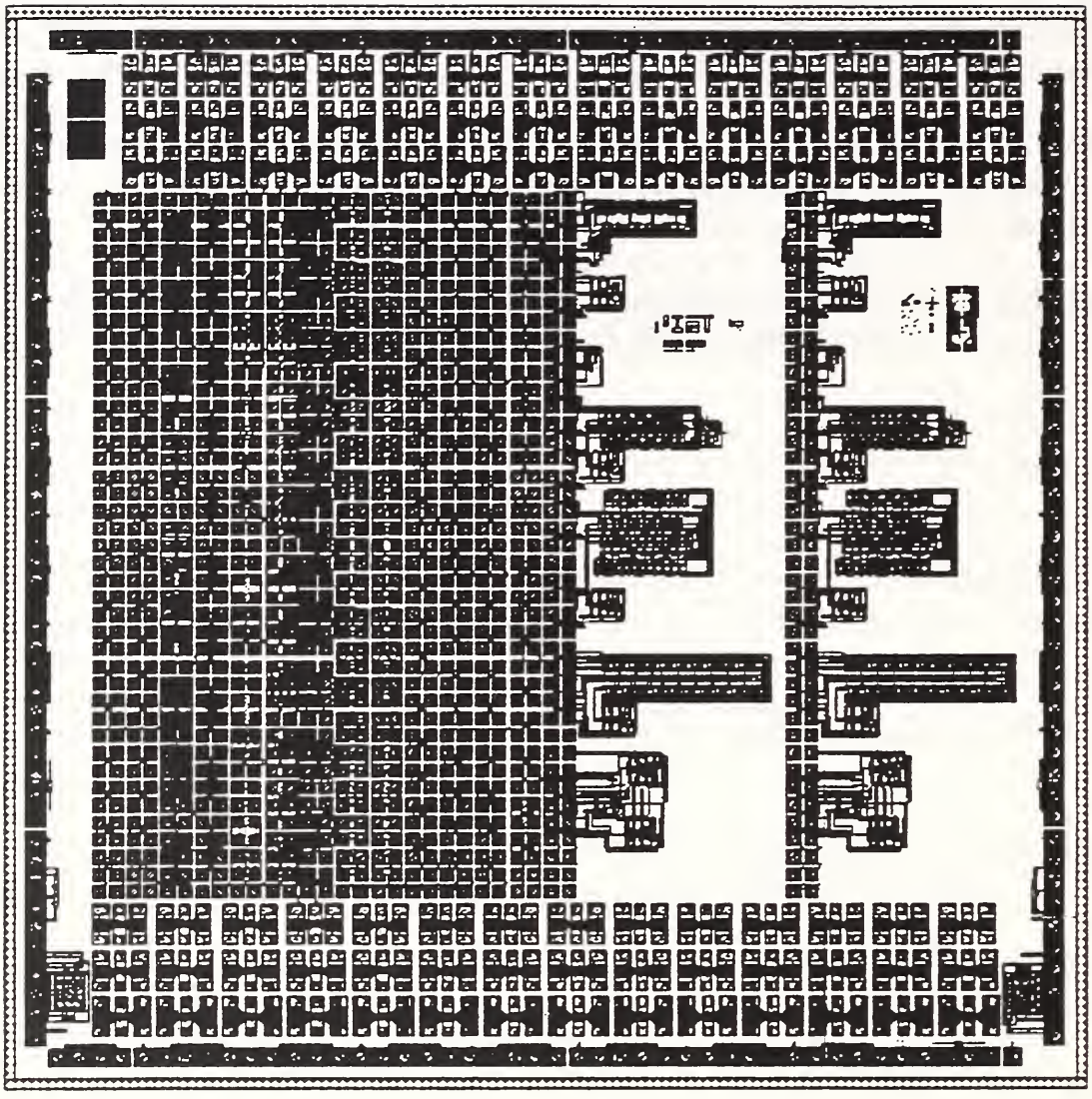


Figure 1. SIMOX Test Chip NIST4.

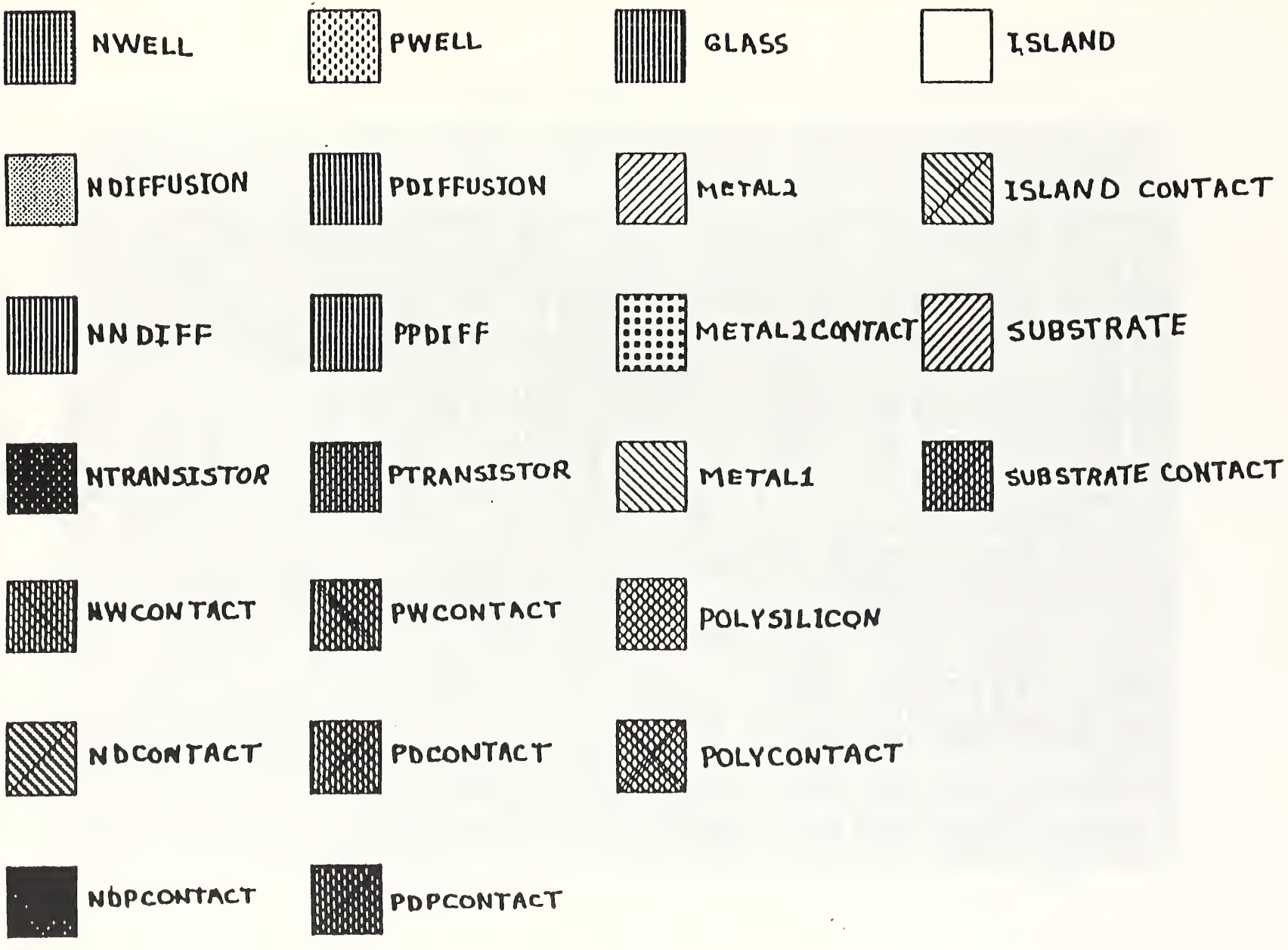


Figure 2. Key to the shading in the figures.

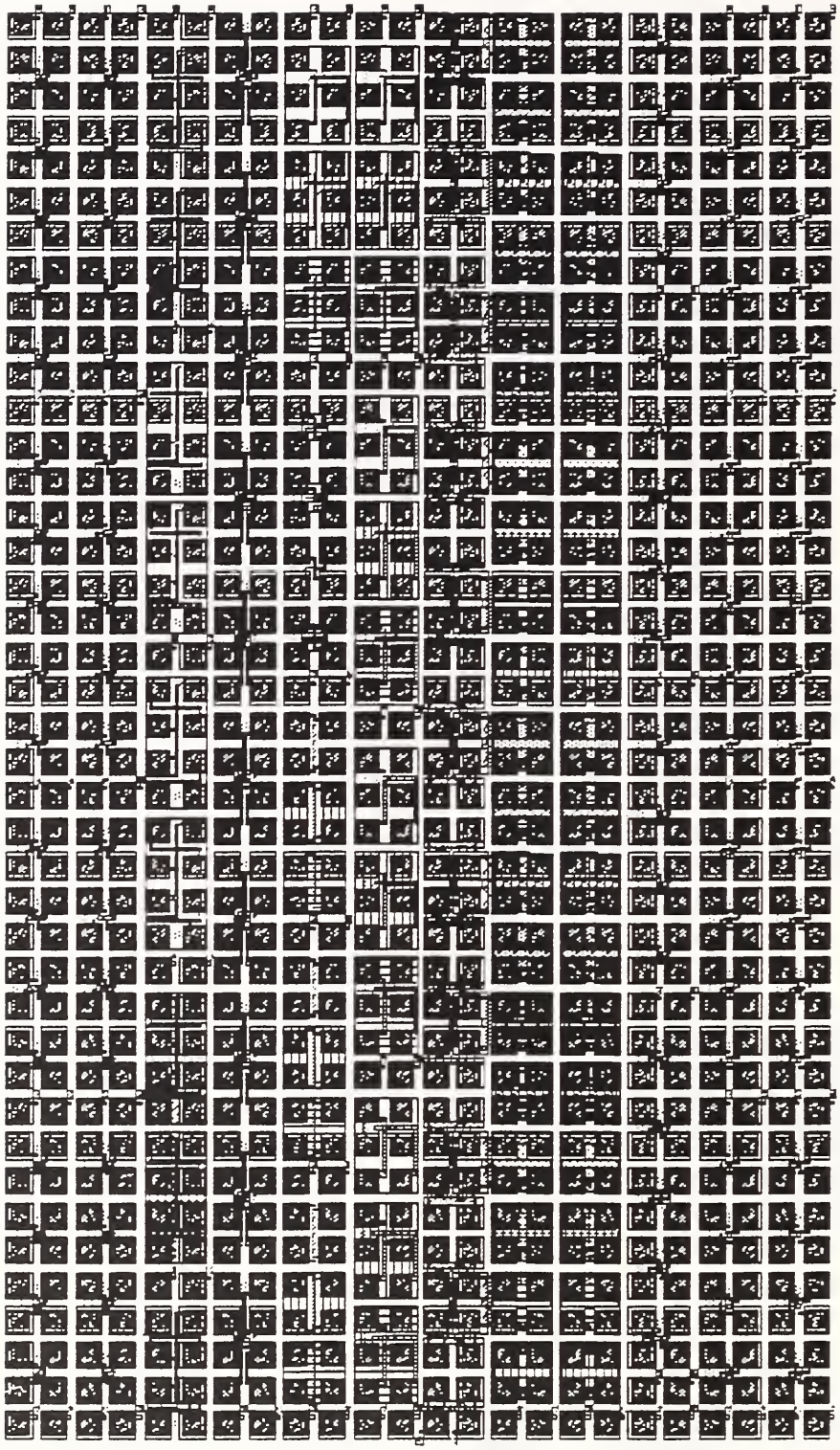


Figure 3. Part-I structures in columns 1 to 12 consist of elemental active devices, inverters, and dc parametric test structures to be probed with a 2 by 10 probe card.

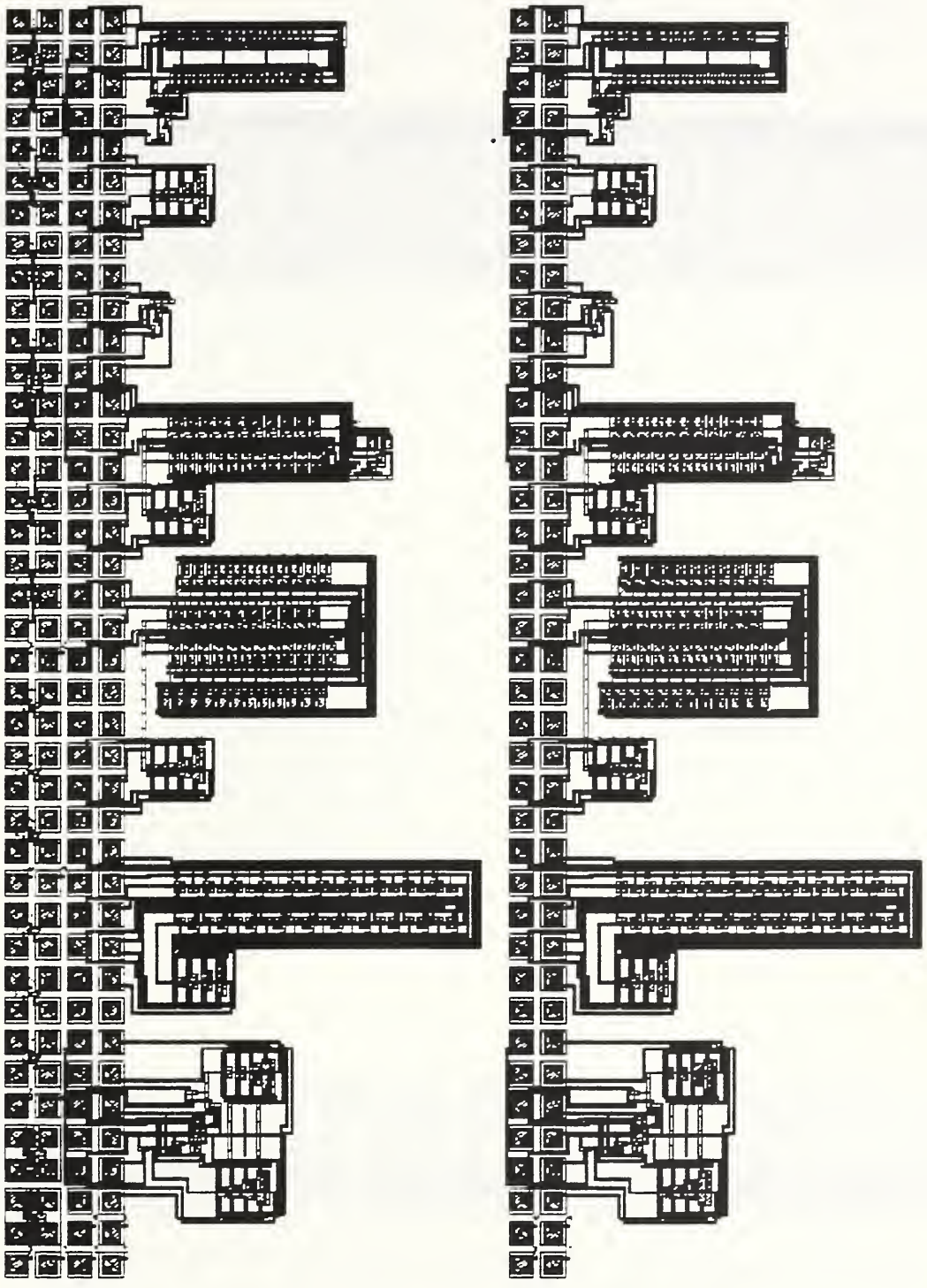


Figure 4. Part-II structures in columns 13 to 15 consist of circuits and their elemental parts.

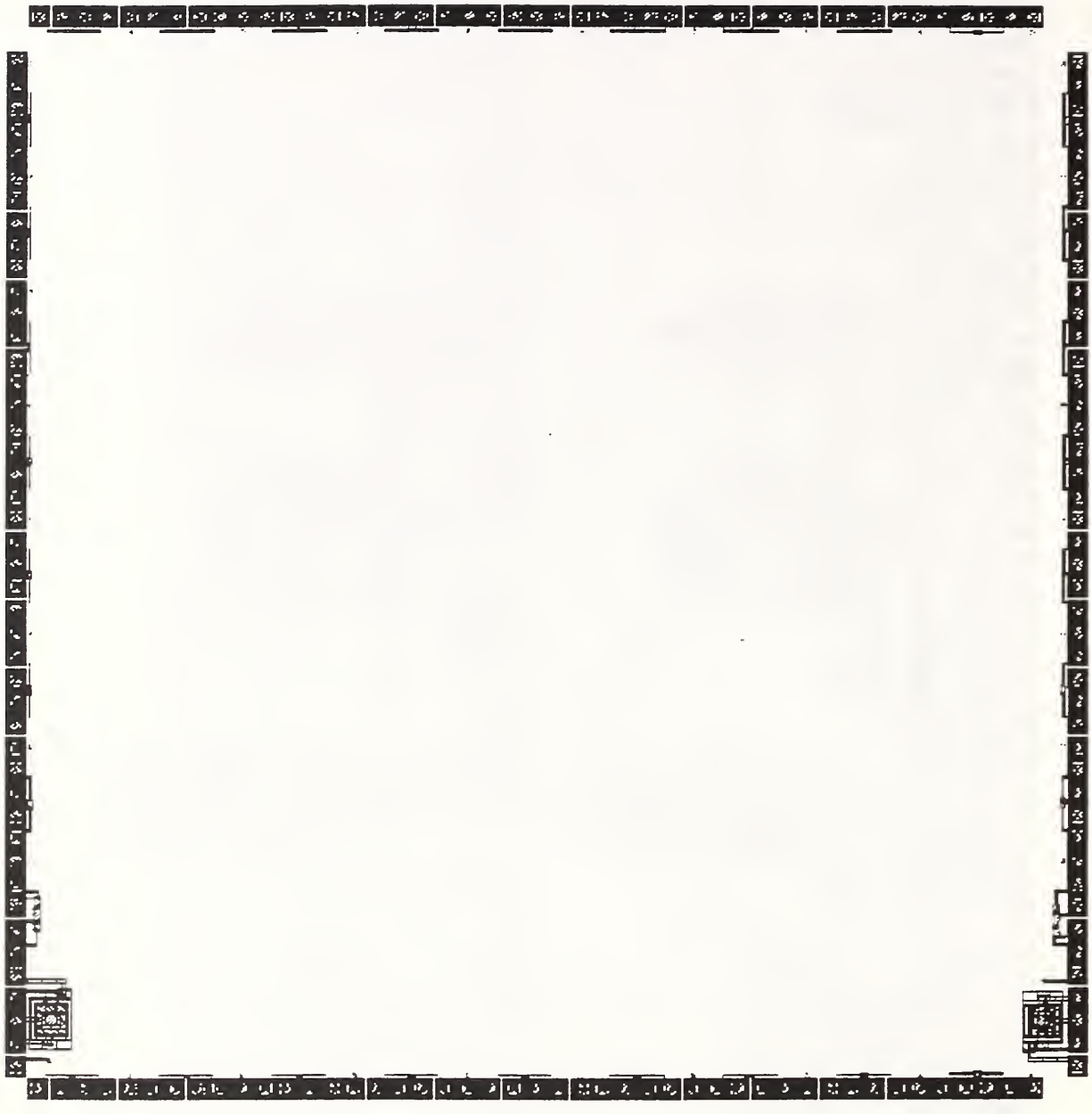
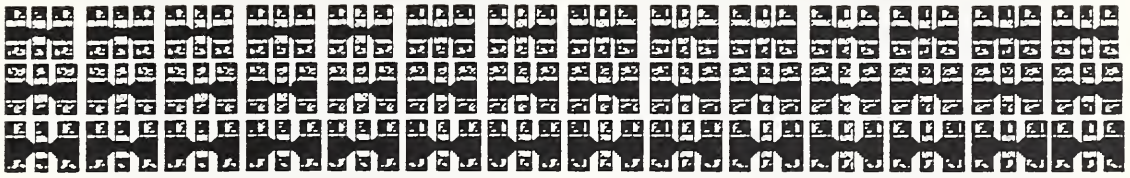


Figure 5. Part-III structures include transistors connected to bondable pads for radiation studies.



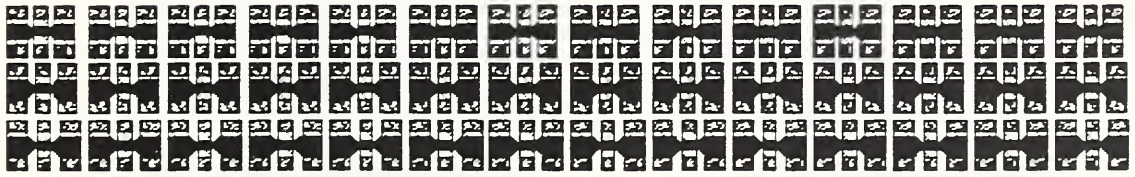


Figure 6. Part-IV structures include transistors padded out to be compatible with rf probe cards for on-wafer rf testing.

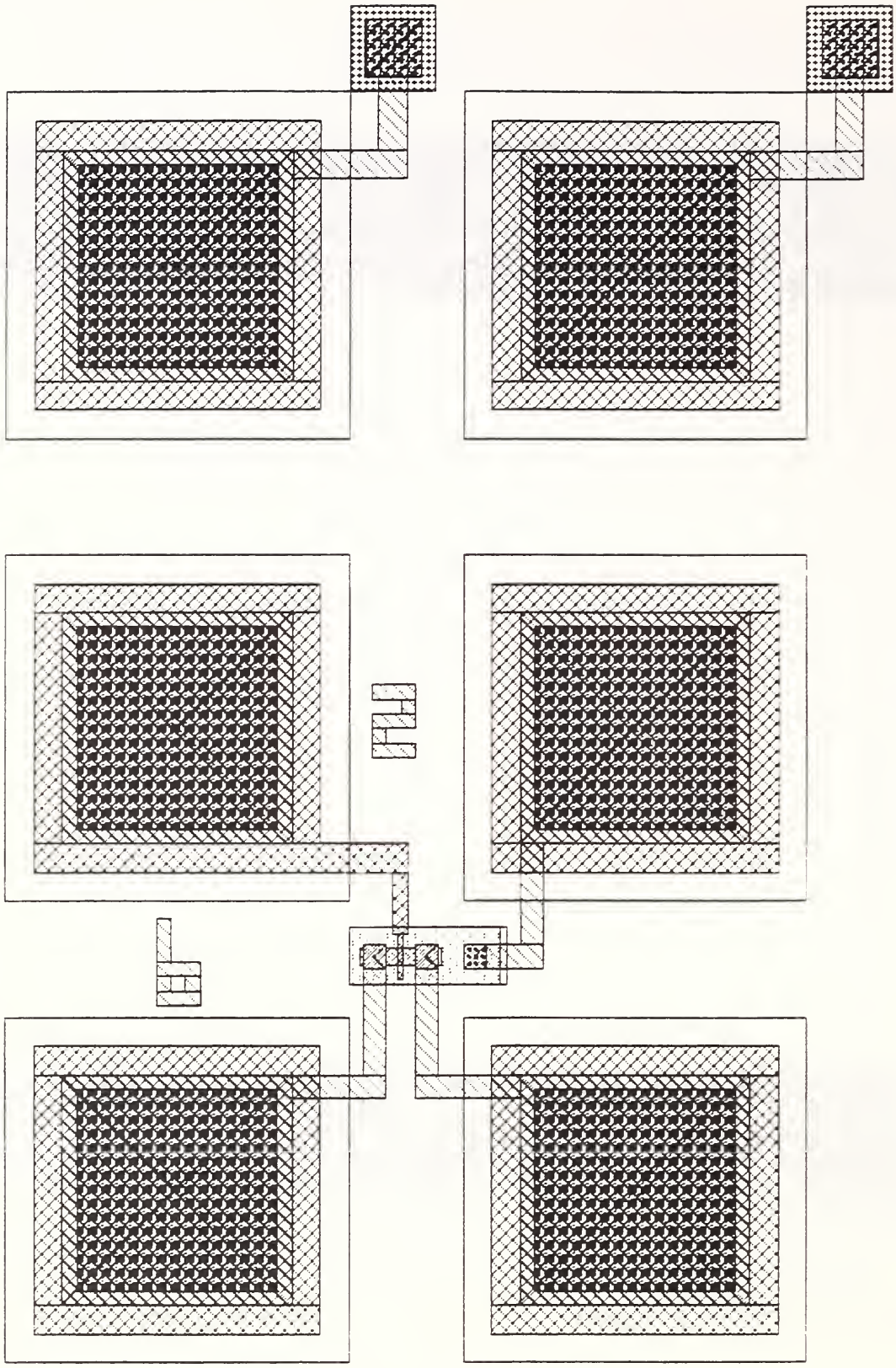


Figure 7. *N*-channel polysilicon gate MOSFET with channel contact beside the drain.

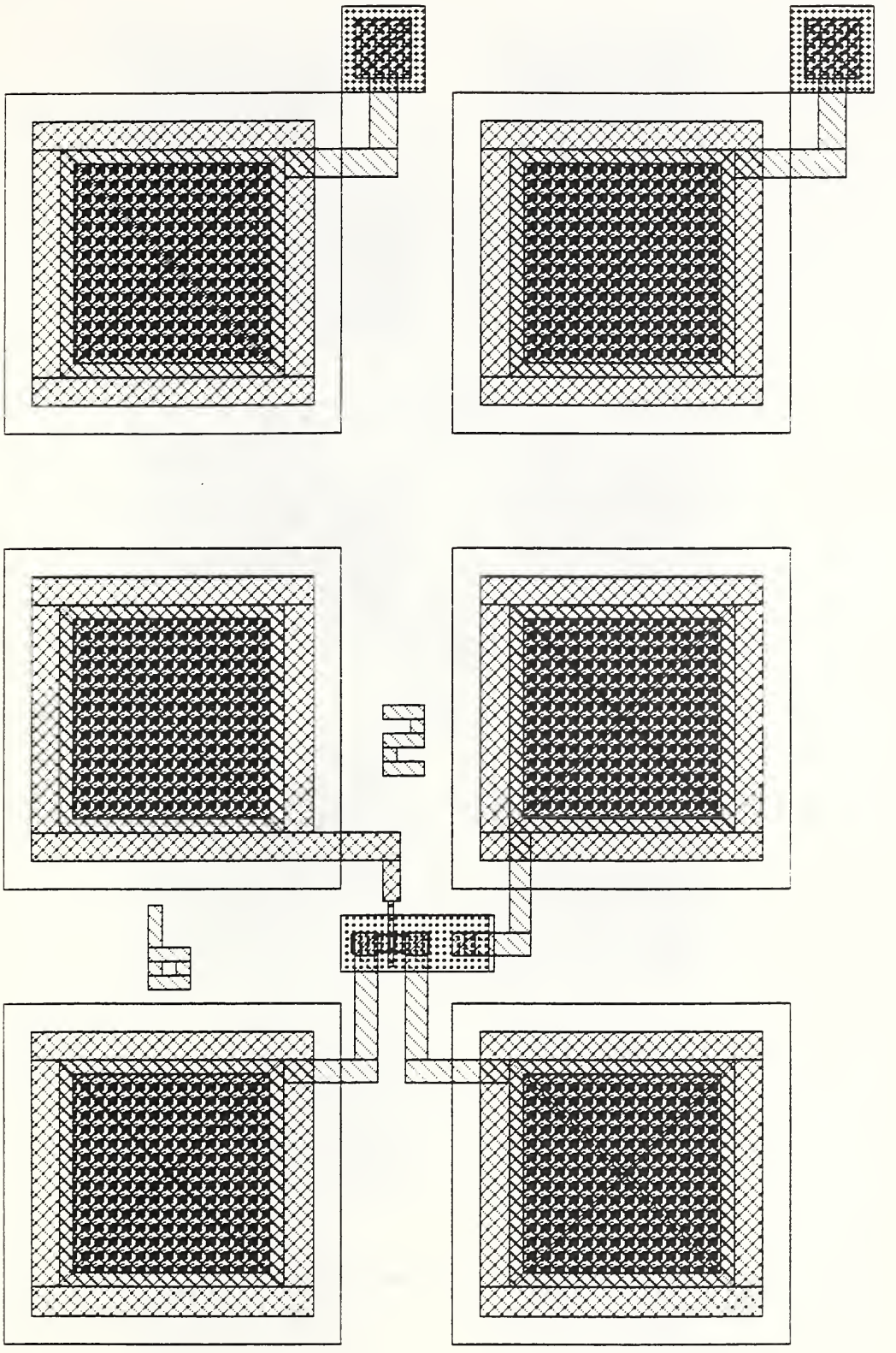


Figure 8. *P*-channel polysilicon gate MOSFET with channel contact beside the drain.

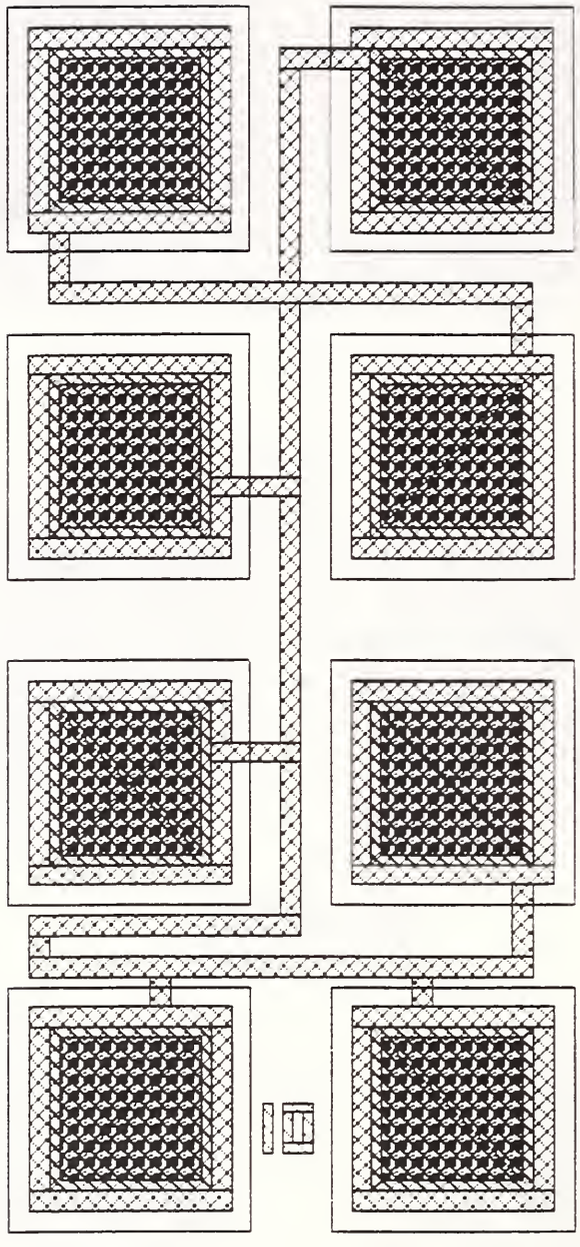


Figure 9. Polysilicon cross-bridge resistor.

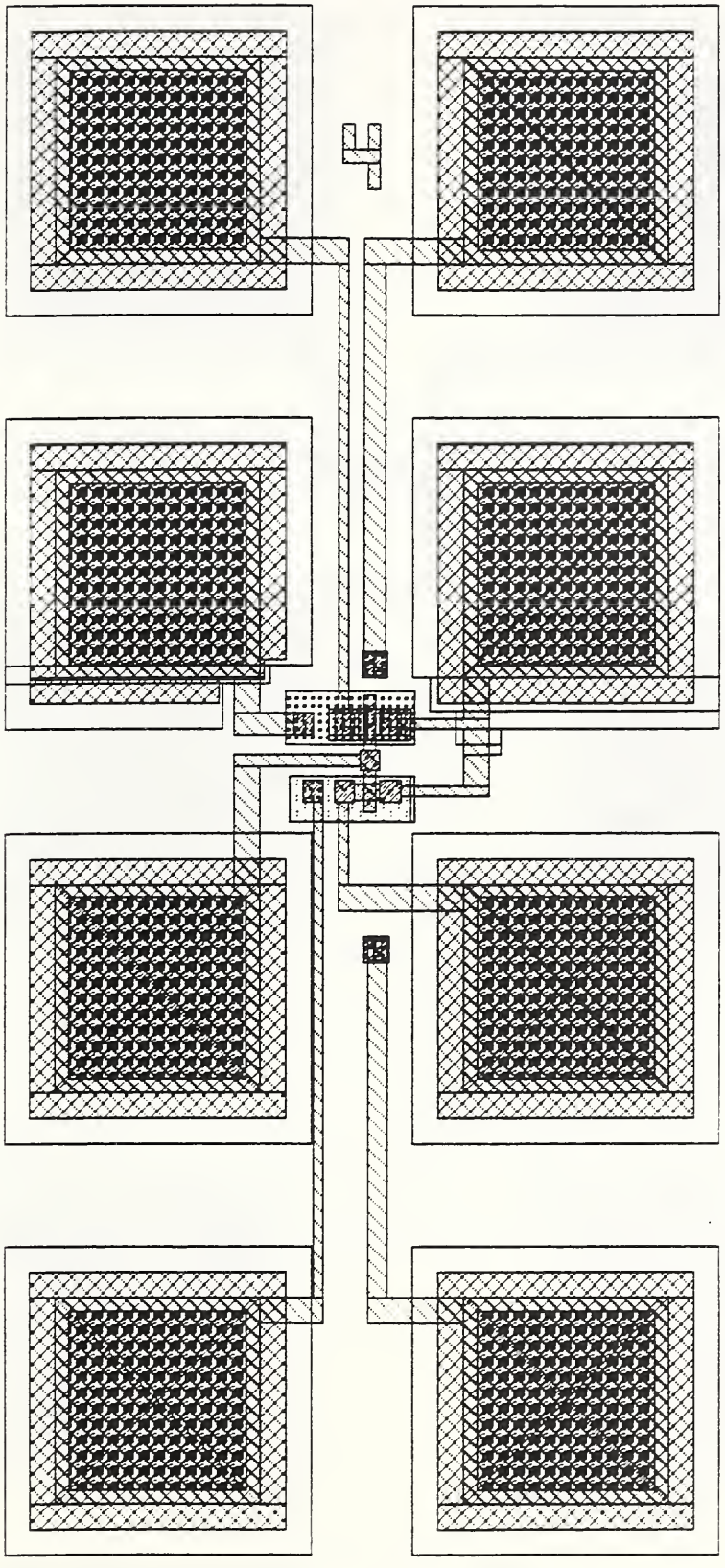


Figure 10. Inverter using L=4 μm.

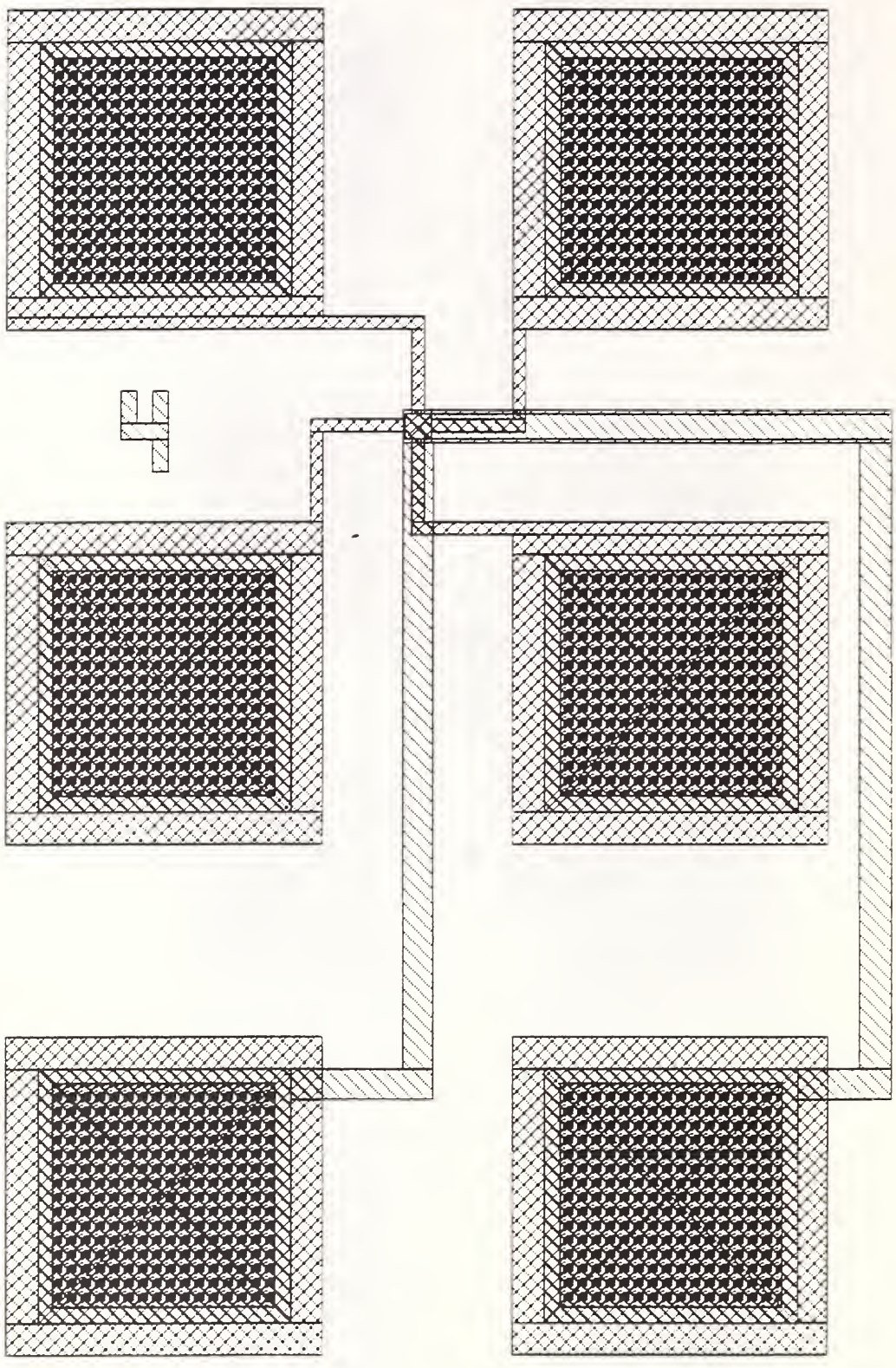


Figure 11. Six-pad contact resistance test structure.

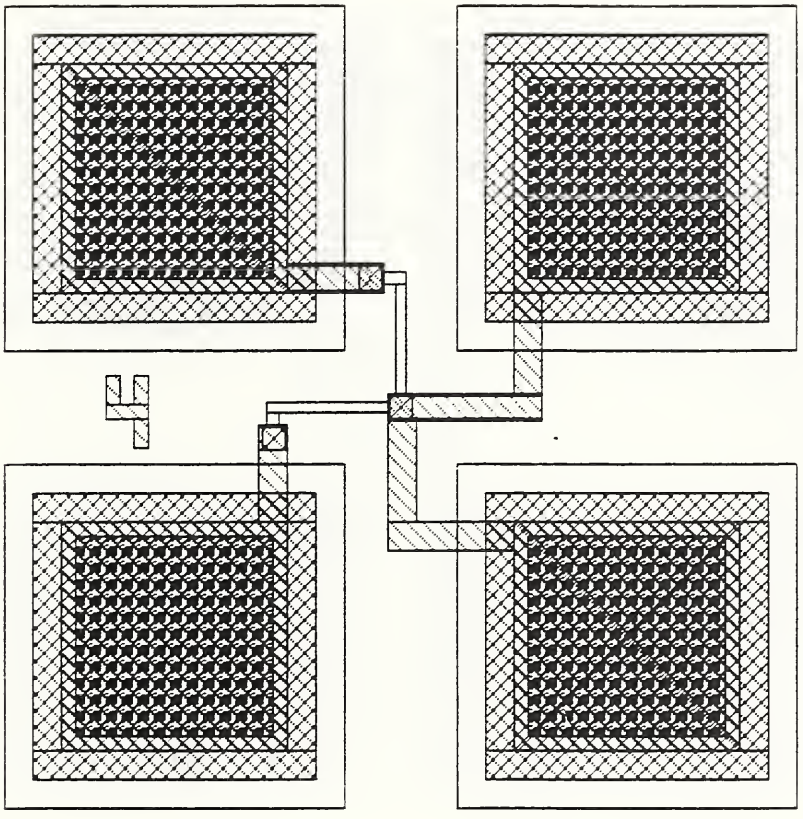


Figure 12. Four-pad contact resistance test structure.

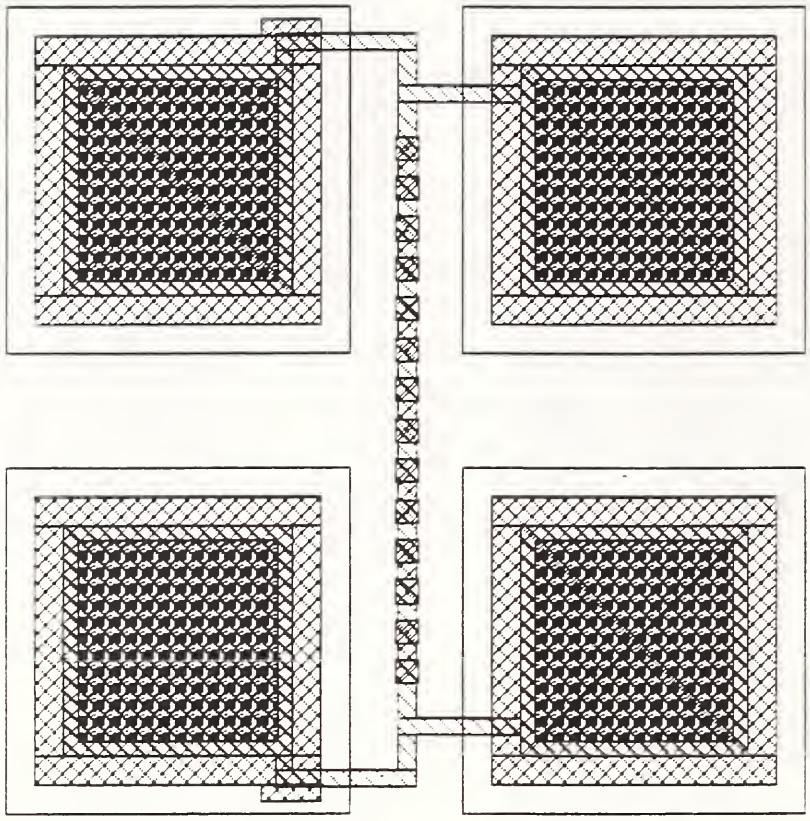


Figure 13. Kelvin chain of 14 contacts.

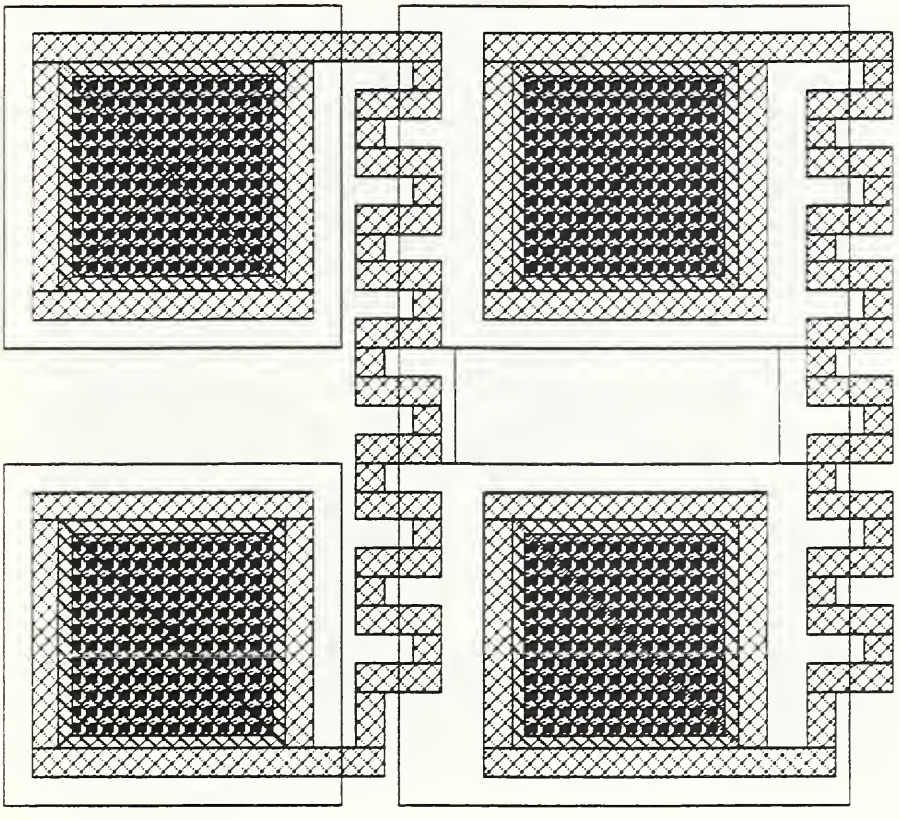


Figure 14. Polysilicon-over-island meander structure.

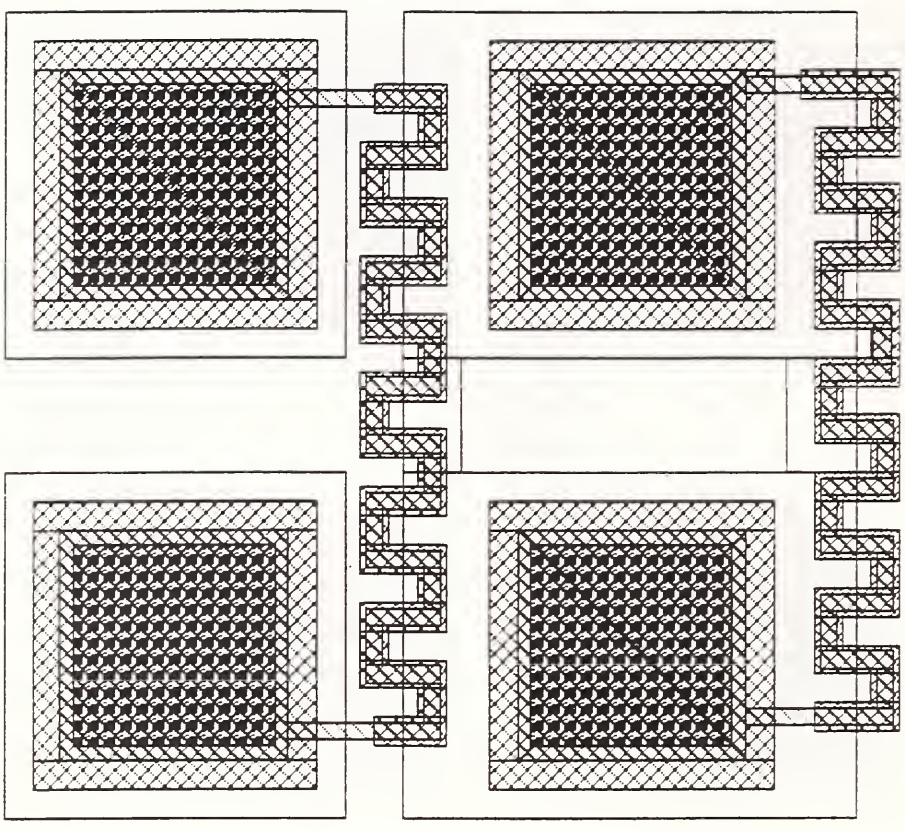


Figure 15. Metal-atop-polysilicon-over-island meander structure.

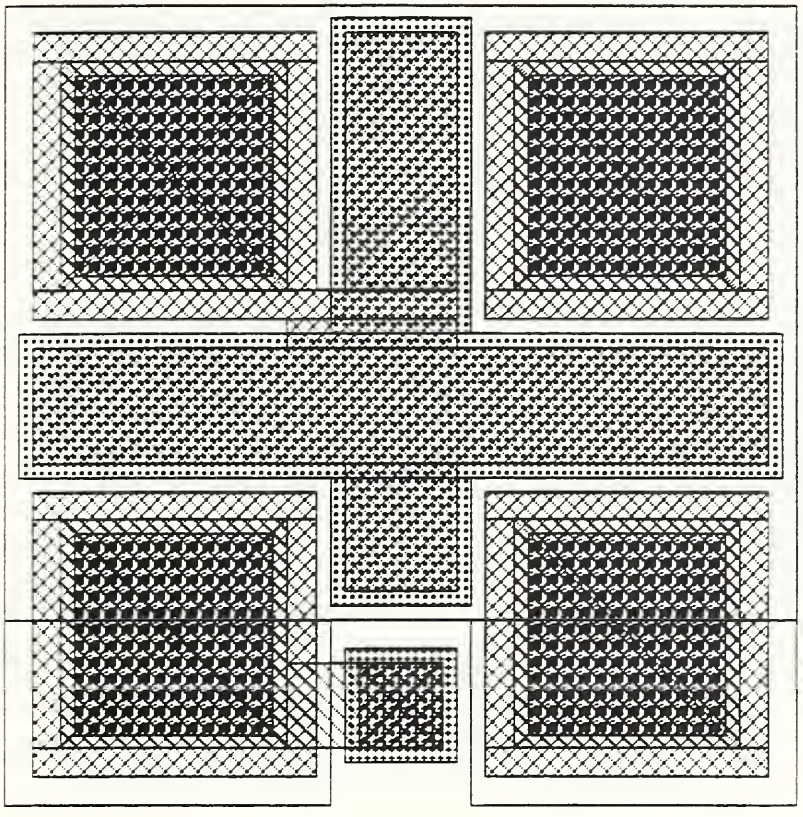


Figure 16. Polysilicon-over-nwell-to-substrate capacitor.

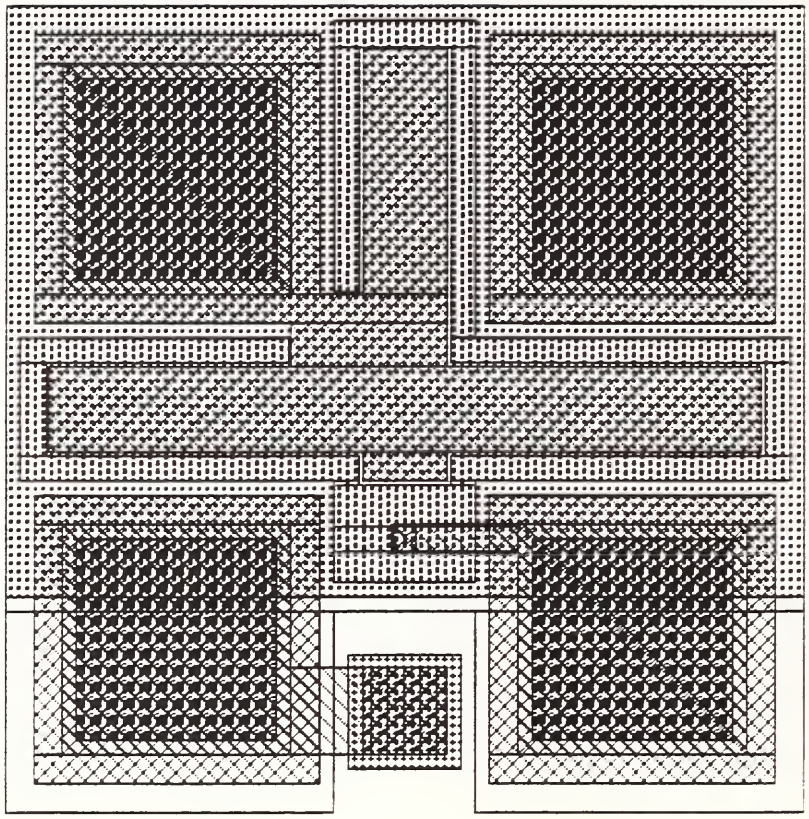


Figure 17. Polysilicon-over-nwell to nearby nndiff in same nwell-to-substrate capacitor.

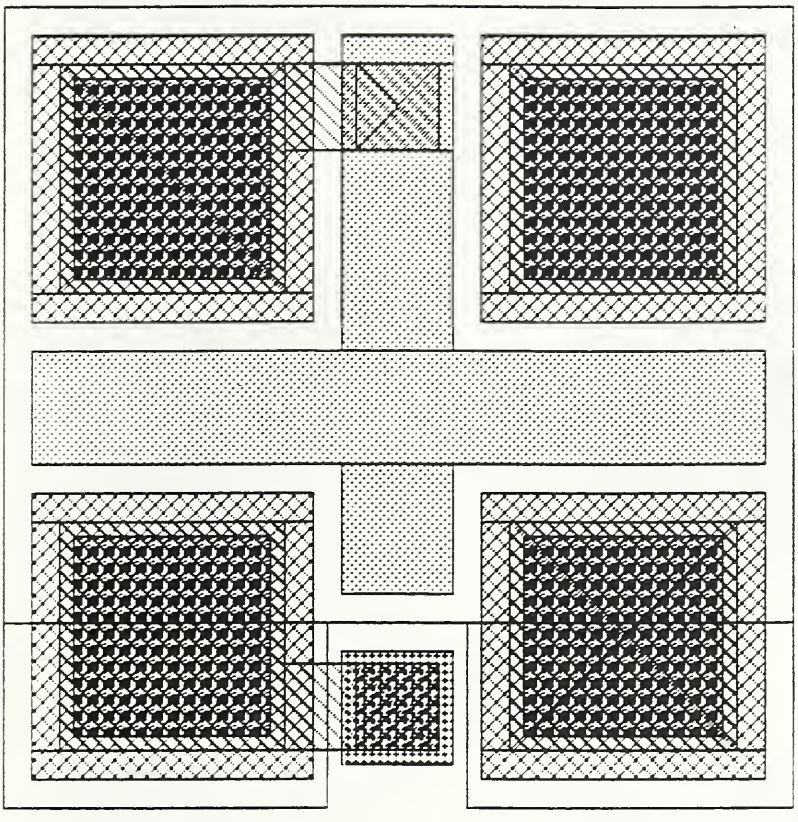


Figure 18. Ndiffusion-to-substrate capacitor.

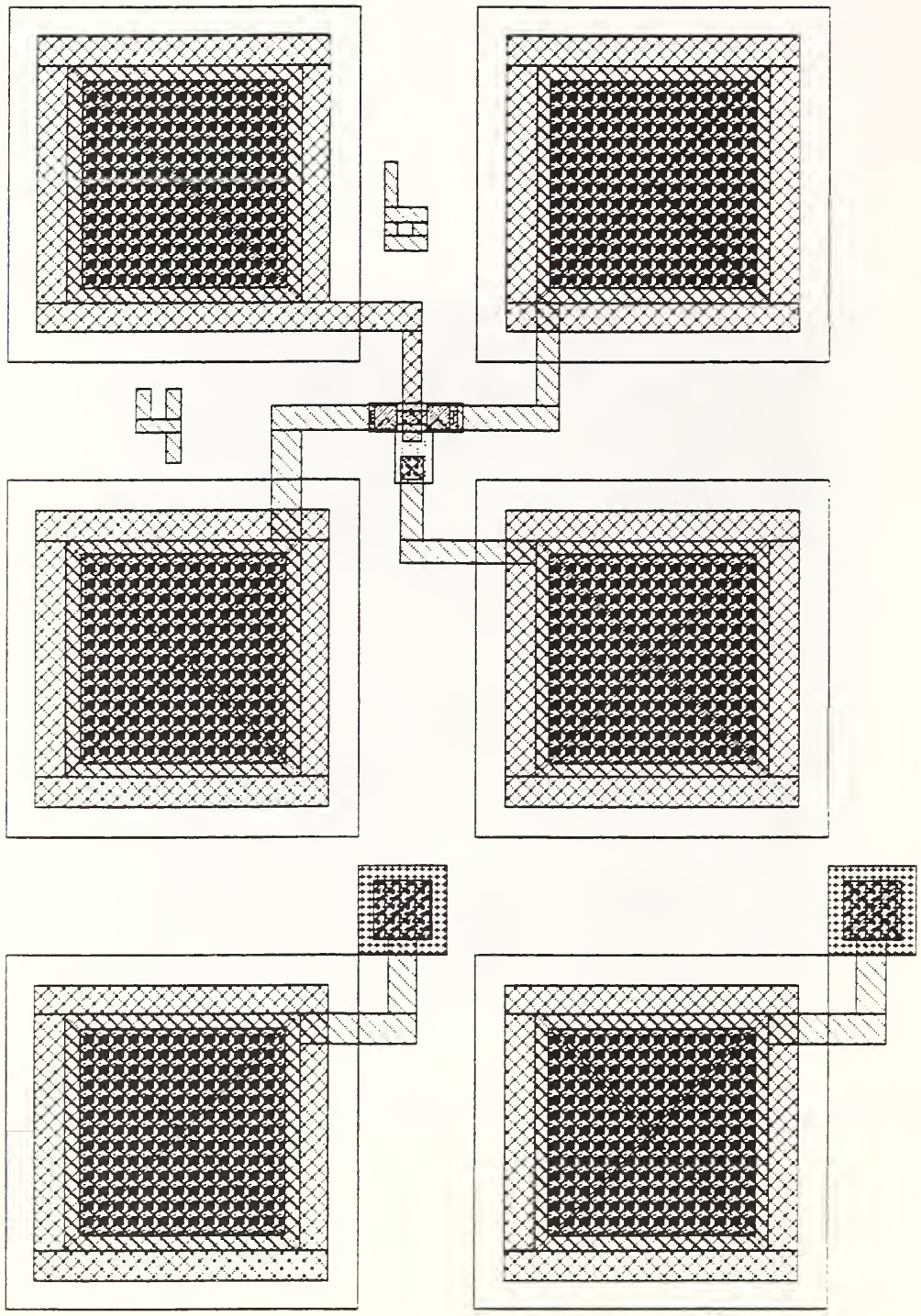


Figure 19. *N*-channel polysilicon gate MOSFET with channel contact near the channel.

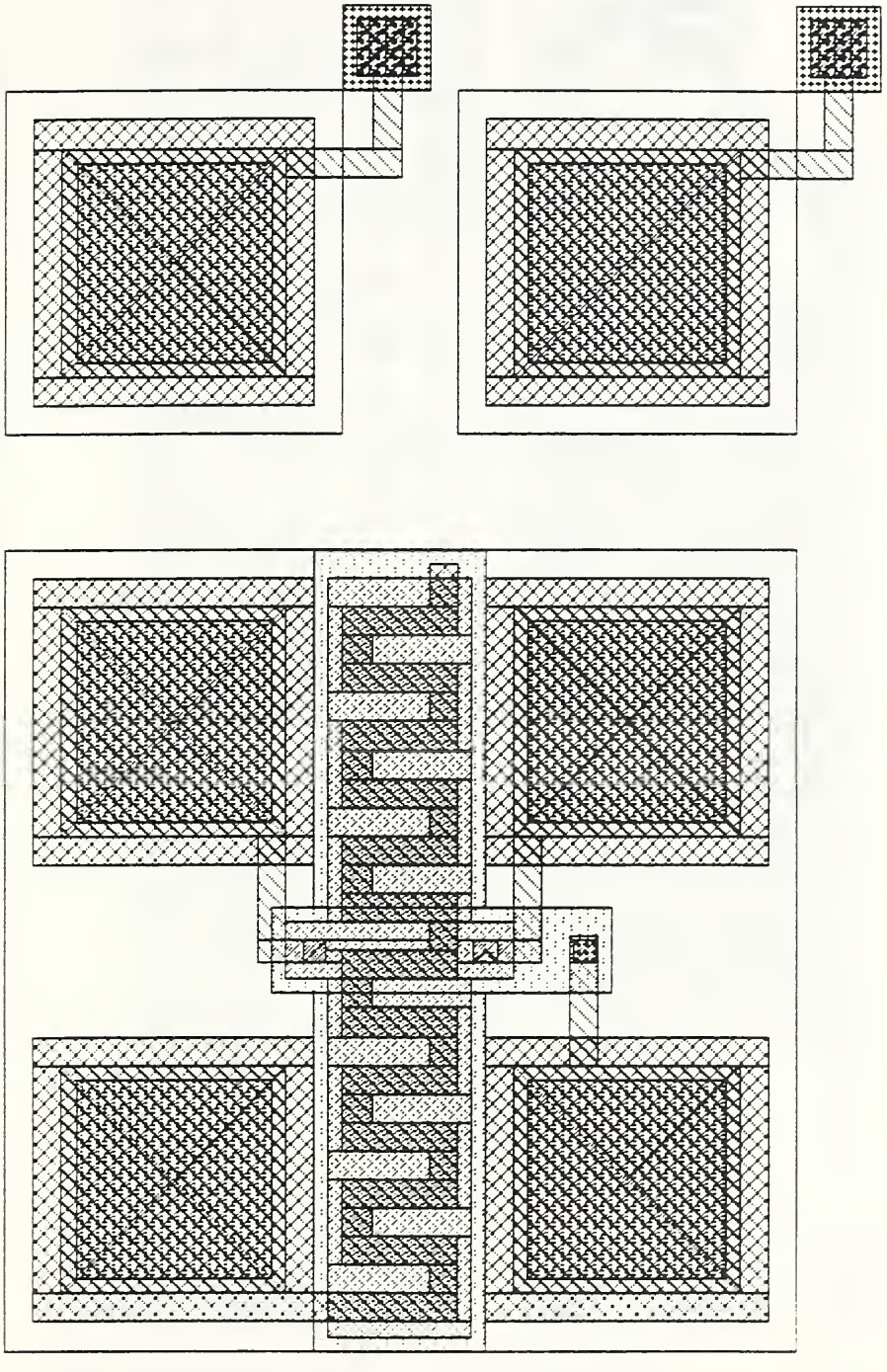


Figure 20. *N*-channel MOSFET with snake-like gate with 25 corners.

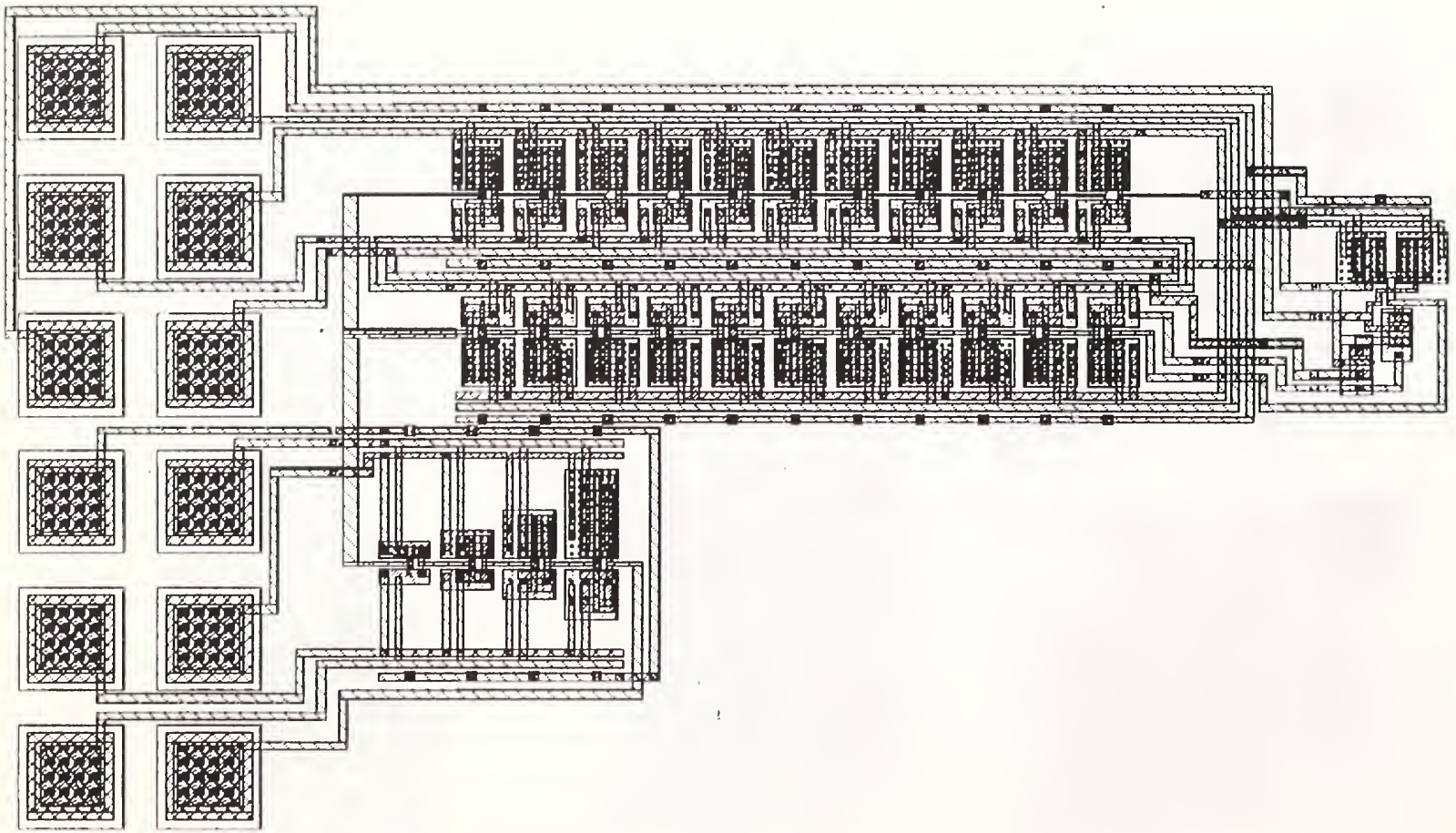


Figure 21. Twenty-three-stage ring oscillator with NAND gate startup and four-stage output amplifier.

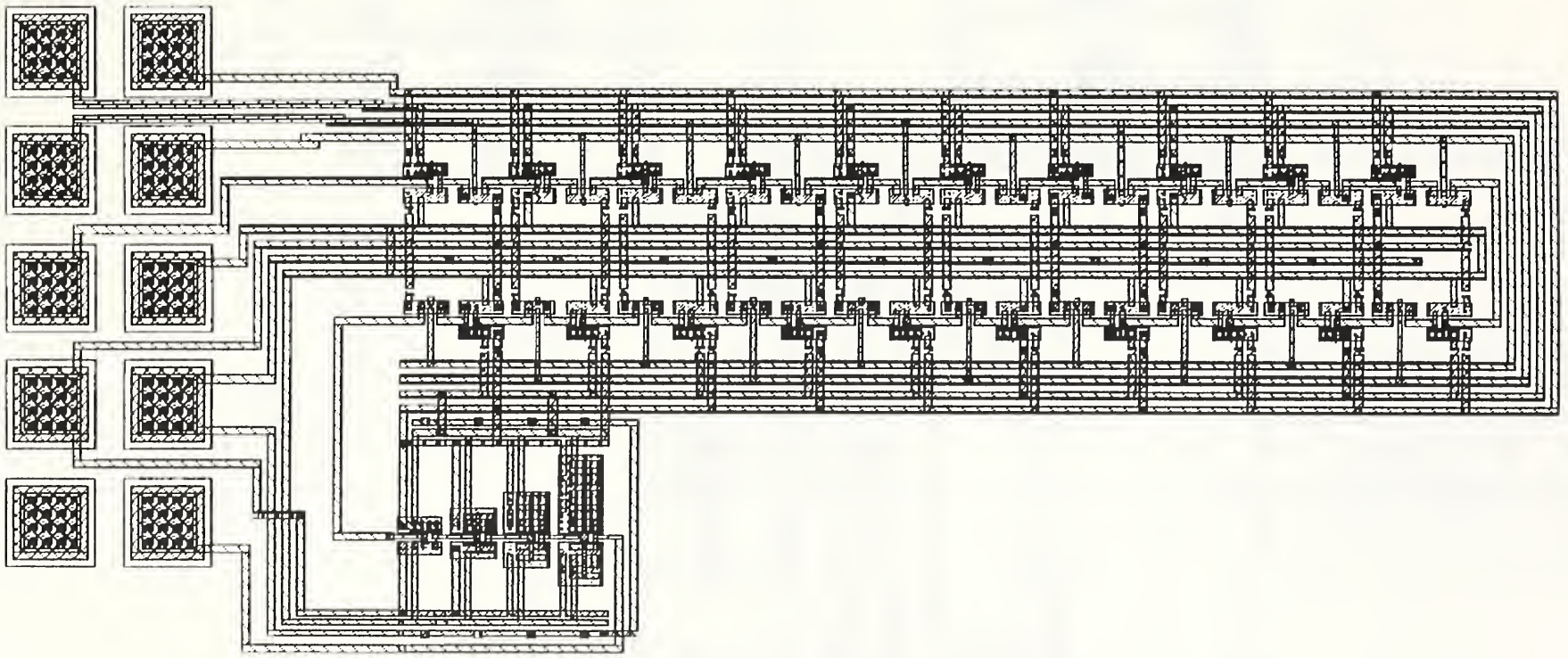


Figure 22. Twenty-stage shift register with two clocks and an output amplifier.

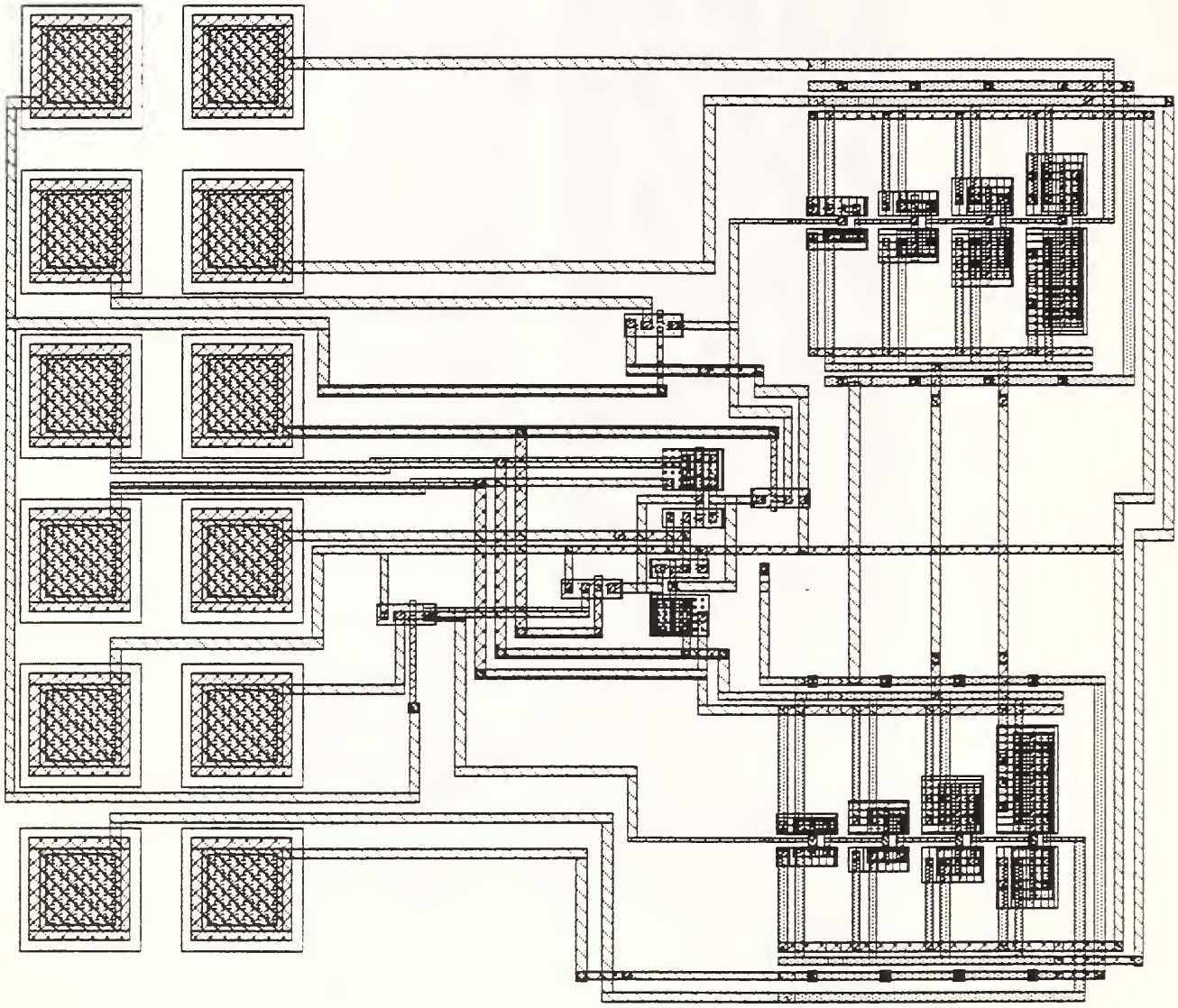


Figure 23. Six-transistor static RAM cell with two four-stage output amplifiers.

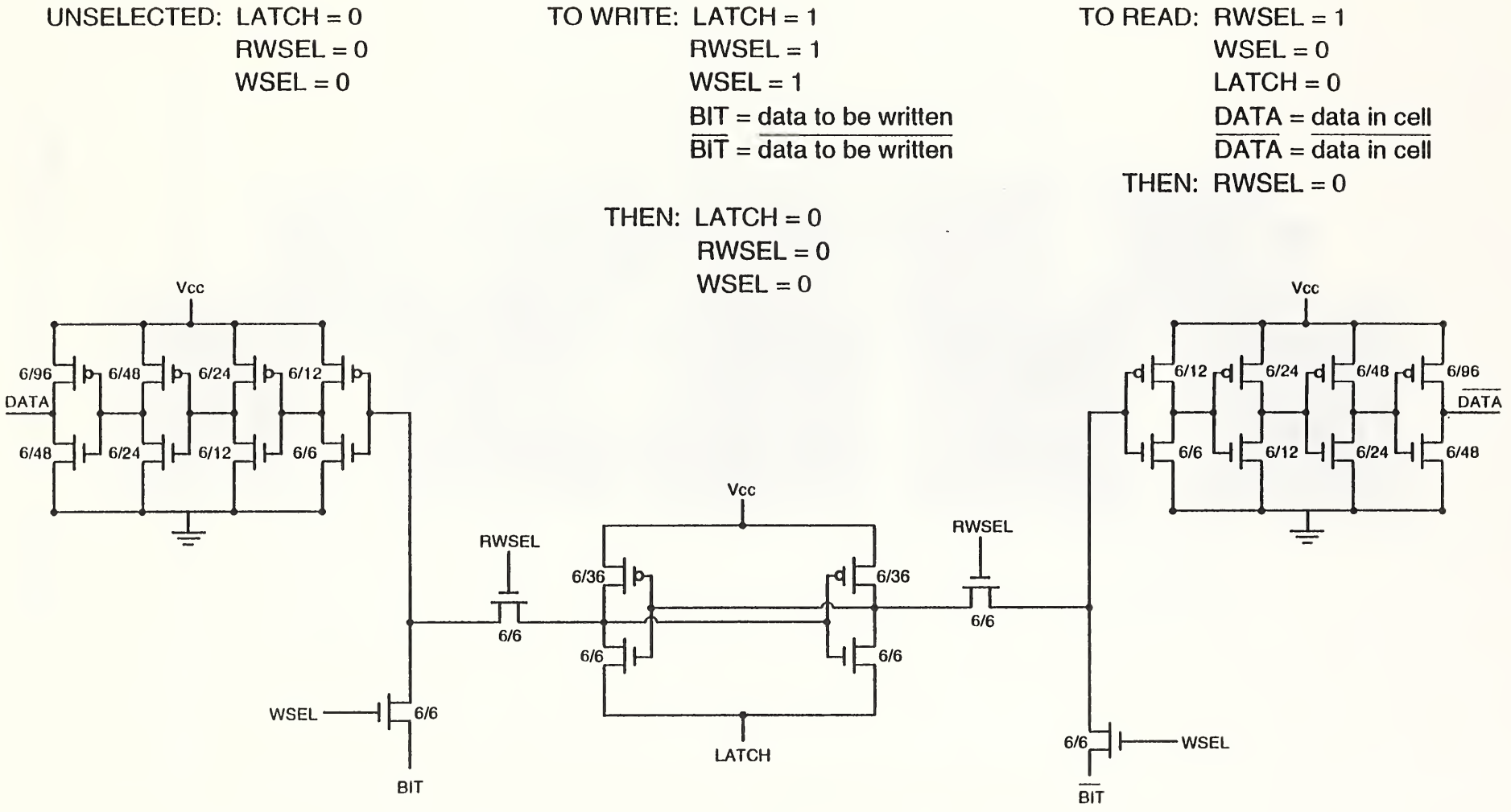


Figure 24. Circuit diagram of the static RAM cell (and how to test it).

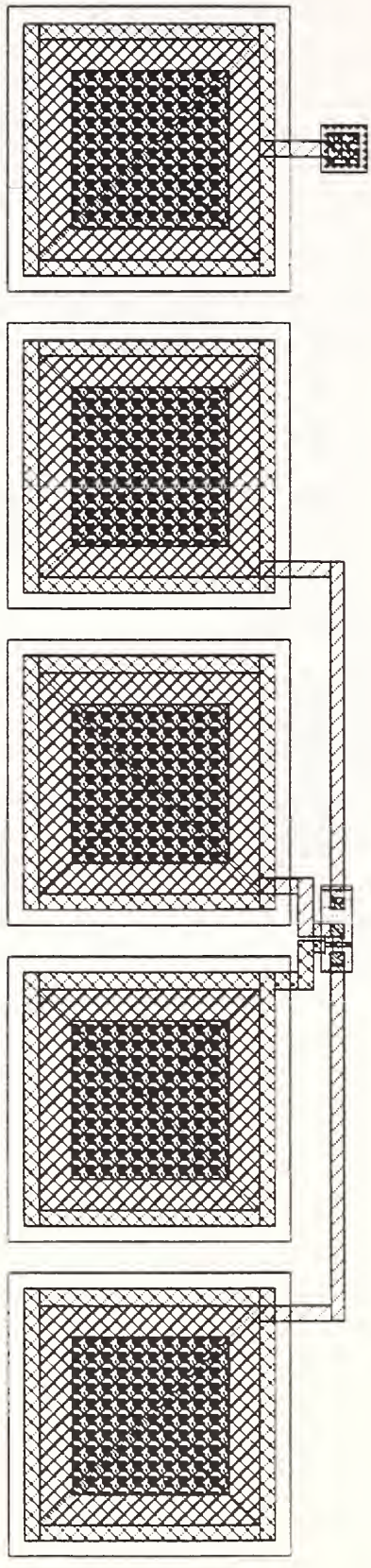


Figure 25. Bonded n-channel MOSFET.

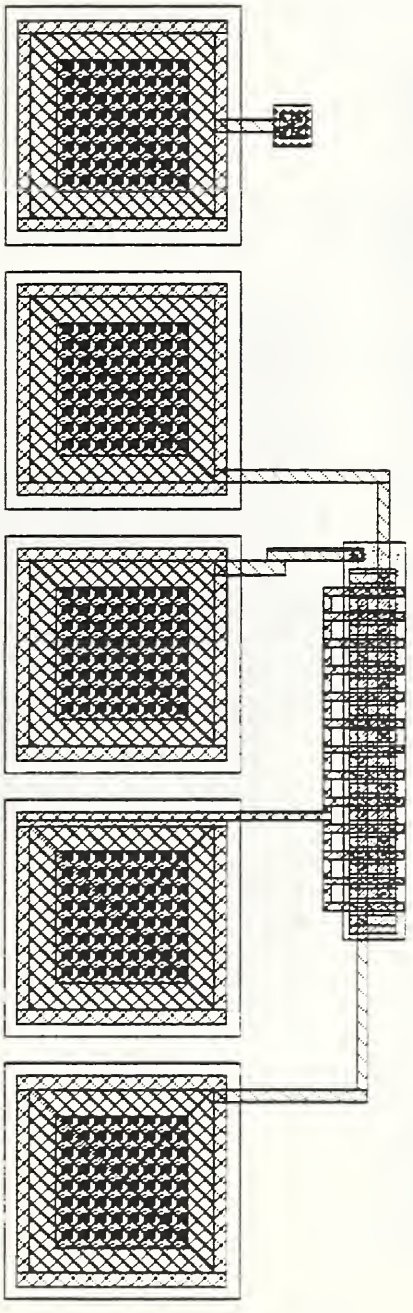


Figure 26. Bonded MOSFET with a comb-shaped gate with 13 teeth.

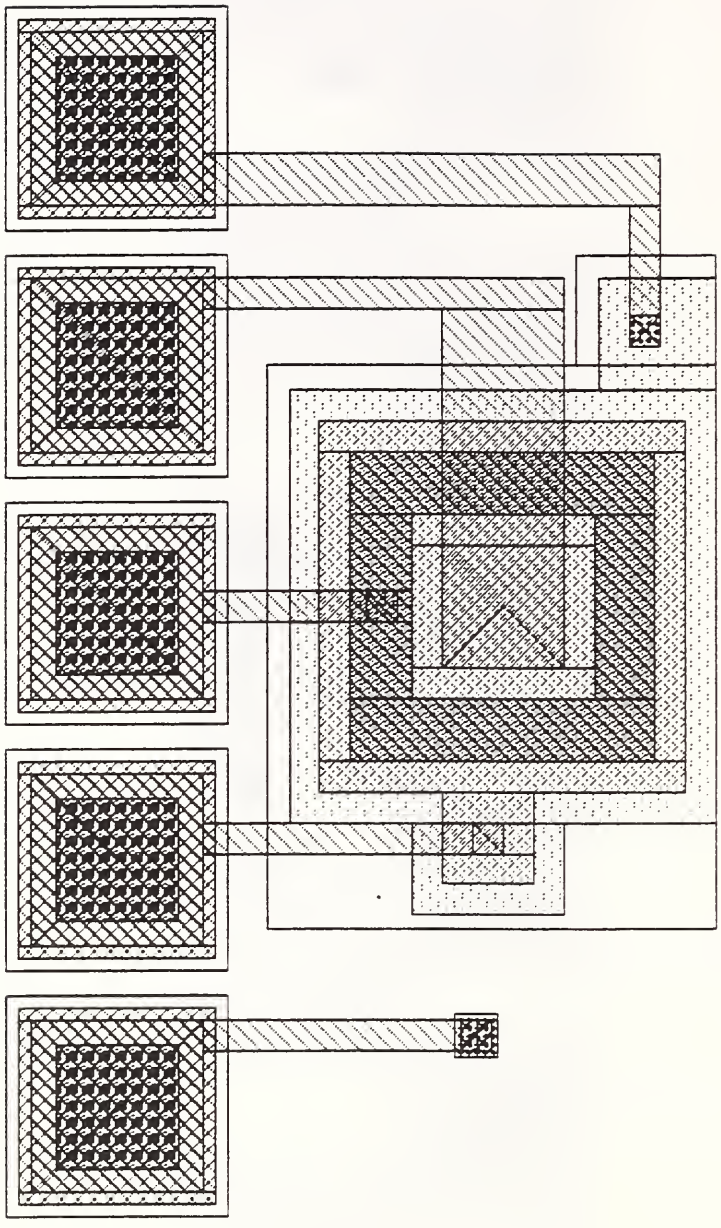


Figure 27. Bonded closed-geometry MOSFET.

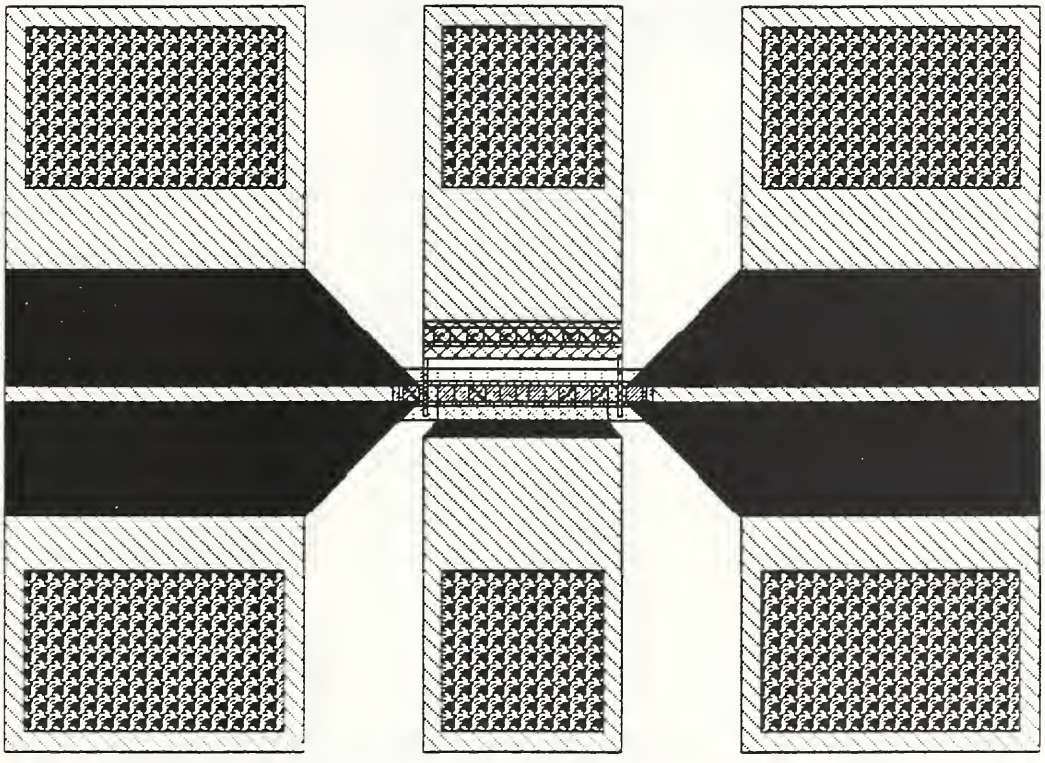


Figure 28. *N*-channel rf transistor.

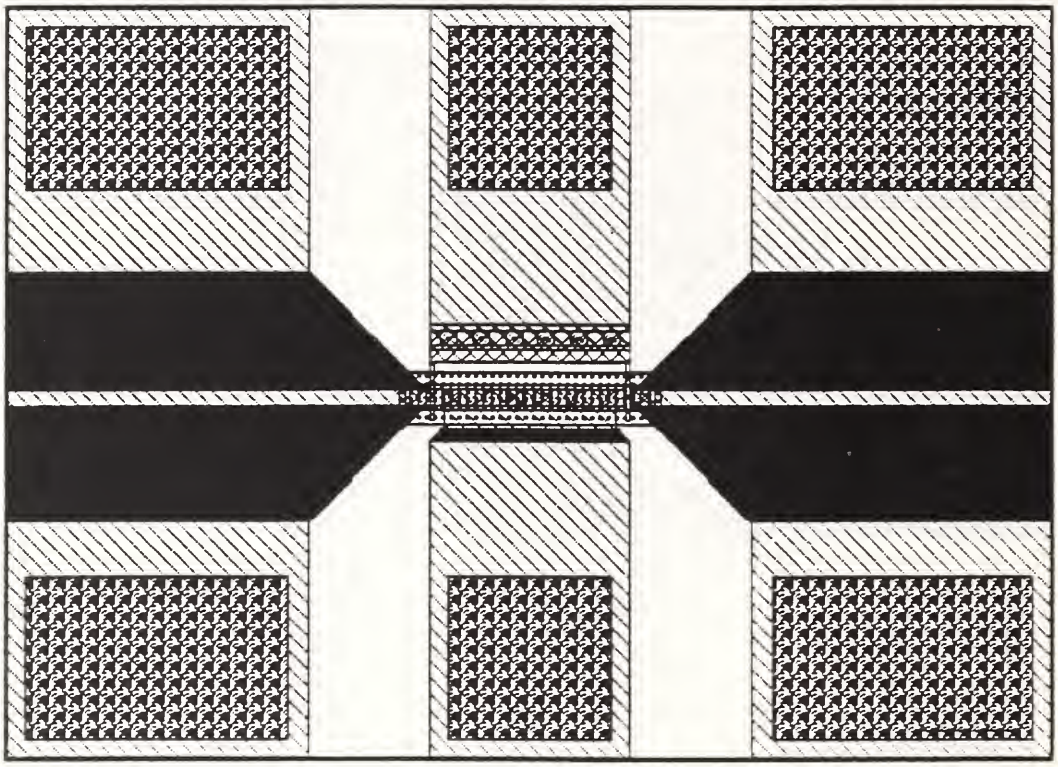


Figure 29. *P*-channel rf transistor.

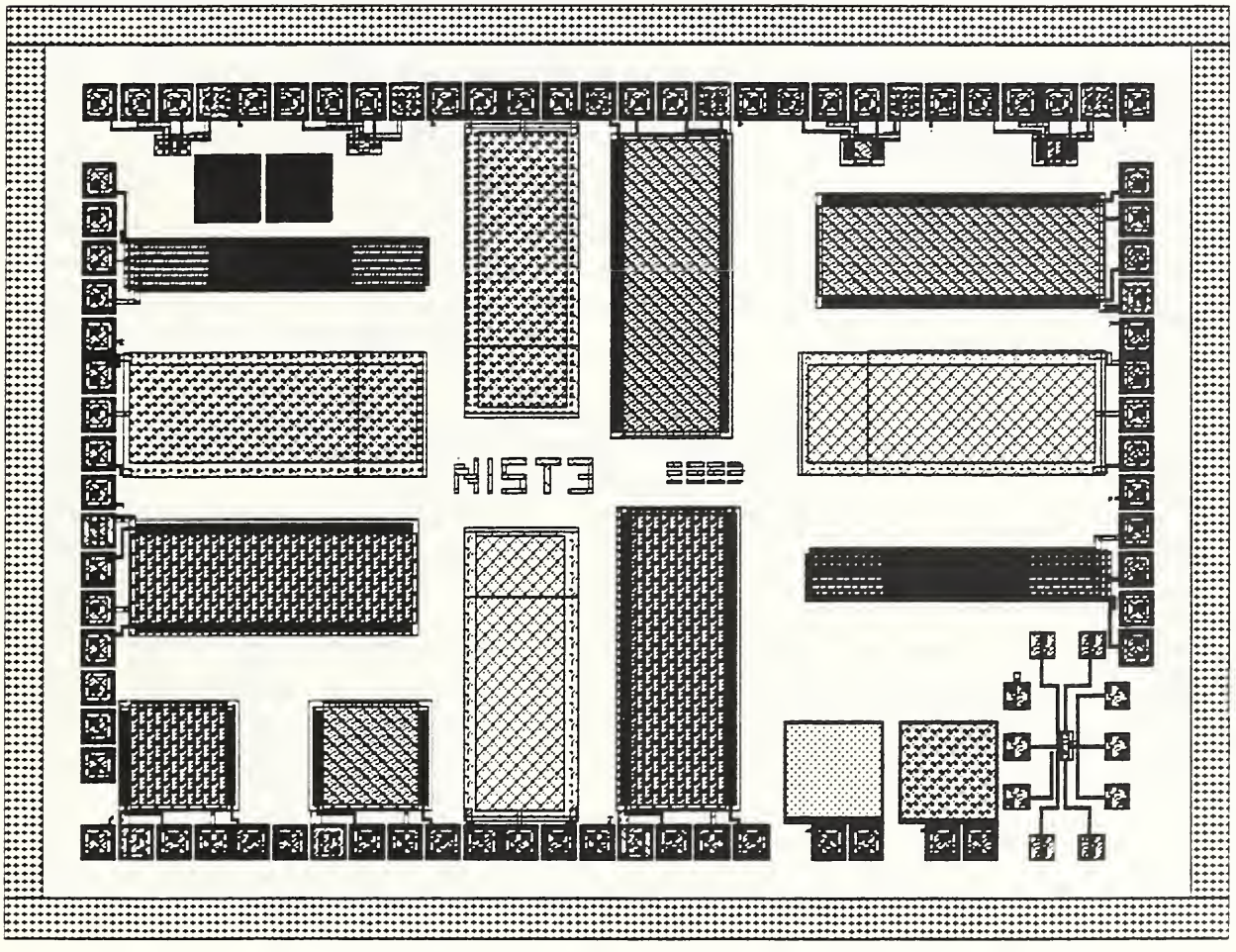


Figure 30. SIMOX Test Chip NIST3.

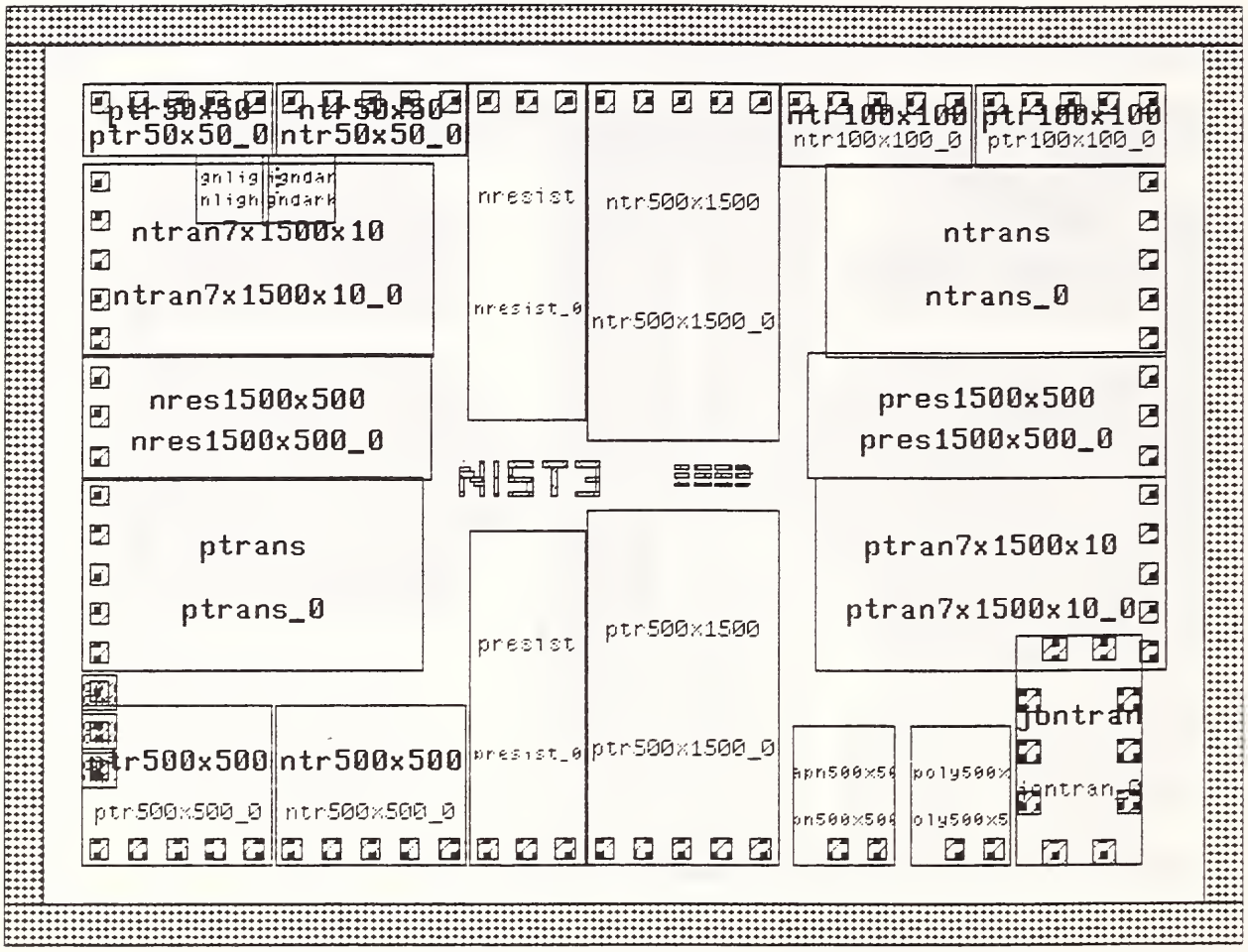


Figure 31. Cell structure of NIST3.

Table 1. General Location of the Test Structures found on NIST4

Part #	Location	Structures
Part I.		
	Column 1	N-channel MOSFETs with the channel contact beside the drain
	Column 2	P-channel MOSFETs with the channel contact beside the drain
	Column 3	Cross-bridge sheet resistors
	Column 4	Inverters
	Column 5	Contact resistors
	Column 6	Contact resistors
	Column 7	Meanders
	Column 8	Capacitors
	Column 9	Capacitors
	Column 10	Specially-sized MOSFETs
	Column 11	N-channel MOSFETs with the channel contact near the channel
	Column 12	P-channel MOSFETs with the channel contact near the channel
Part II.		
	Column 13	Component parts of the dynamic test structures and miscellaneous structures
	Column 14	Dynamic test structures (L=6μm)
	Column 15	Dynamic test structures (L=4μm)
Part III.		
	Bond Pads on Top of the chip	N-channel MOSFETs
	Bond Pads on Left of the chip	N-channel MOSFETs
	Bond Pads on Bottom of the chip	P-channel MOSFETs
	Bond Pads on Right of the chip	P-channel MOSFETs
Part IV.		
	Row 1	N-channel RF transistors (spacing between the electrodes=50μm)
	Row 2	N-channel RF transistors (spacing between the electrodes=60μm)
	Row 3	N-channel RF transistors (spacing between the electrodes=70μm)
	Row 4	P-channel RF transistors (spacing between the electrodes=50μm)
	Row 5	P-channel RF transistors (spacing between the electrodes=60μm)
	Row 6	P-channel RF transistors (spacing between the electrodes=70μm)
Miscellaneous locations		miscellaneous structures

Table 2. Basic Test Structures found on NIST4 (and the parameters measured)

Structure	Parameter(s) Measured	Where on NIST4	Sample Figure(s)	Ref.
Contact resistors	Contact resistance	Part I C 5 & 6	11,12, 13	[5]
Cross-bridge sheet resistors	Sheet resistance Bridge width	Part I C 3	9	[3]
MOSFETs	Transistor characteristics, Gate oxide parameters, Electrical channel length, Interface trapped charge density	Part I C 1 & 2 C 11 & 12 C 13 Part III Top, Left Bottom, Right	7,8 19 20 25 26 27	[10] [11,12]
RF transistors	Switching speed	Part IV R 1-6	28,29	[8]
Inverters	Inverter characteristics	Part I C 4 C 13	10	[4]
Capacitors	Capacitance	Part I C 8 & 9	16,17, 18	[4]
Meanders	Connectivity	Part I C 7	14,15	[6]
Ring oscillators	Frequency Inverter delay	Part II C 14 & 15	21	[4,13]
Shift register	Data retention vs. clocking speed	Part II C 14 & 15	22	[4]
Static RAM cell	Data retention	Part II C 14 & 15	23	[14]

Table 3. Miscellaneous Structures and Pertinent Information

Designed Cell Name	Remarks
1. alignlight	Alignment marks to be used with a clear field mask Located in the upper left portion of the chip.
2. aligndark	Alignment marks to be used with a dark field mask Located in the upper left portion of the chip.
3. ident	An identification of the levels located Located in the middle left portion of the chip.
4. chevron	Chevrons to check the minimum feature sizes and spaces organized as follows: ndiffusion pdiffusion nwell pwell island polysilicon metal
5. none	The NIST4 identifier

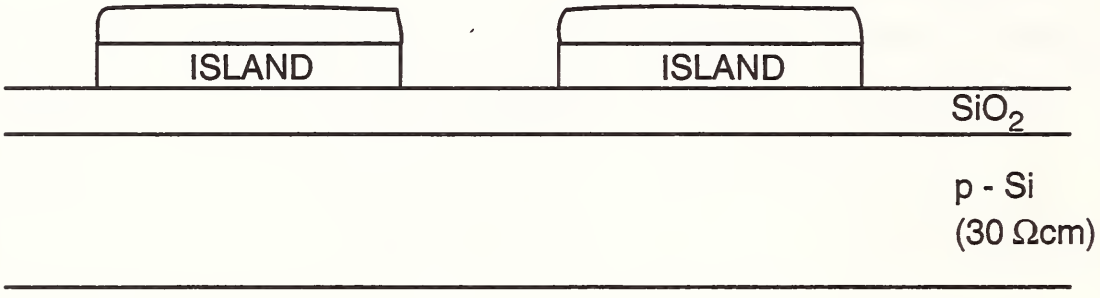
Table 4. Test Structure List with Critical Dimensions for the SIMOX Test Chip, NIST3

Designed Cell Name	Structure	Critical Dimensions(μm)
1. ptr50x50	p-channel MOSFET	(L=50,W=50)
2. ntr50x50	n-channel MOSFET	(L=50,W=50)
3. nresist	nwell resistor	(Lpoly=460, Wpoly=1410)
4. ntr500x1500	n-channel MOSFET	(L=500,W=1500)
5. ntr100x100	n-channel MOSFET	(L=100,W=100)
6. ptr100x100	p-channel MOSFET	(L=100,W=100)
7. ntrans	n-channel MOSFET	(L=460,W=1440)
8. pres1500x500	pwell resistor	(Lpoly=500, Wpoly=1500)
9. ptran7x1500x10	p-channel MOSFET	(L=10,W=7x1500)
10. jontran	a bipolar structure	
11. cappoly500x500	polysilicon over nwell - substrate capacitor	(Area=500μmx500μm)
12. capn500x500	ndiffusion - substrate capacitor	(Area=500μmx500μm)
13. ptr500x1500	p-channel MOSFET	(L=500,W=1500)
14. presist	pwell resistor	(Lpoly=460, Wpoly=1410)
15. ntr500x500	n-channel MOSFET	(L=500,W=500)
16. ptr500x500	p-channel MOSFET	(L=500,W=500)
17. ptrans	p-channel MOSFET	(L=460,W=1440)
18. nres1500x500	nwell resistor	(Lpoly=500, Wpoly=1500)
19. ntran7x1500x10	n-channel MOSFET	(L=10,W=7x1500)

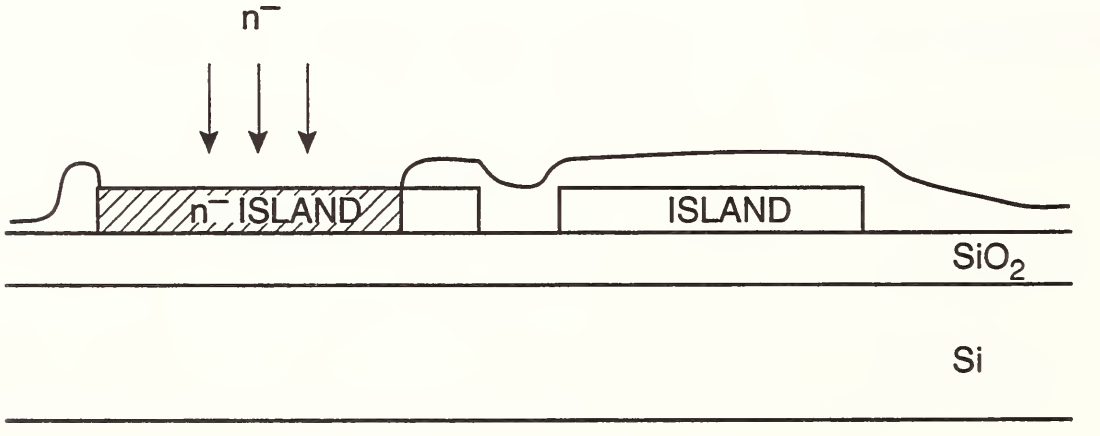
20.	alignlight3	alignment marks to be used with a clear field mask
21.	aligndark3	alignment marks to be used with a dark field mask
22.	none	NIST3 identifier

APPENDIX A - The Ten SIMOX Processing Steps

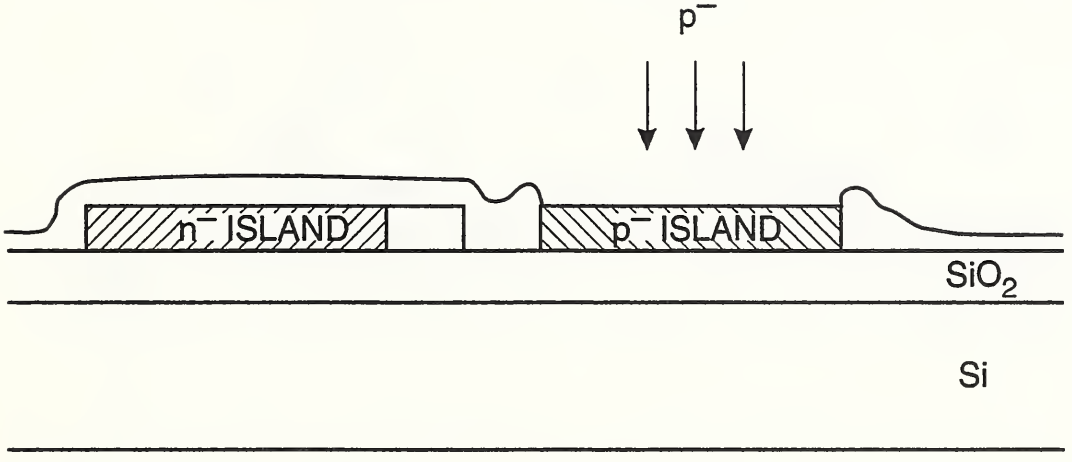
STEP 1 - ISLAND (a clear field mask)



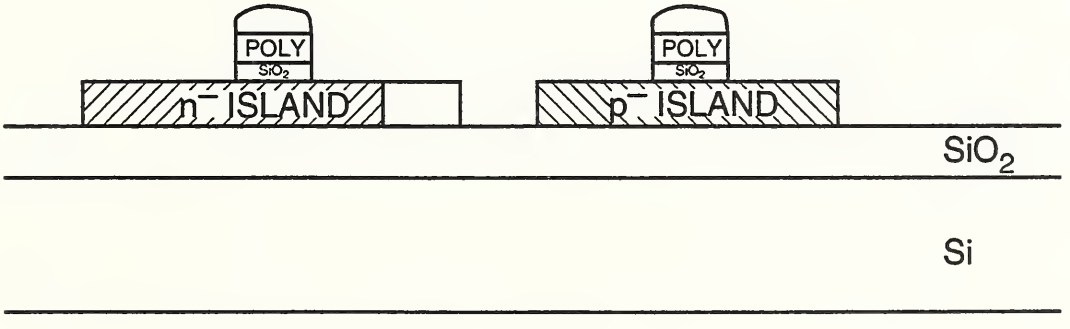
STEP 2 - NWELL (a dark field mask)



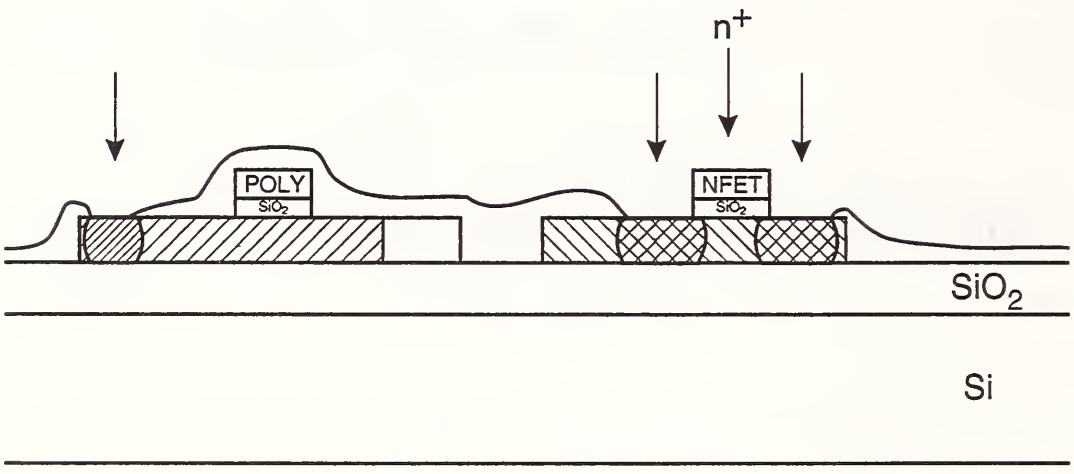
STEP 3 - PWELL (a dark field mask)



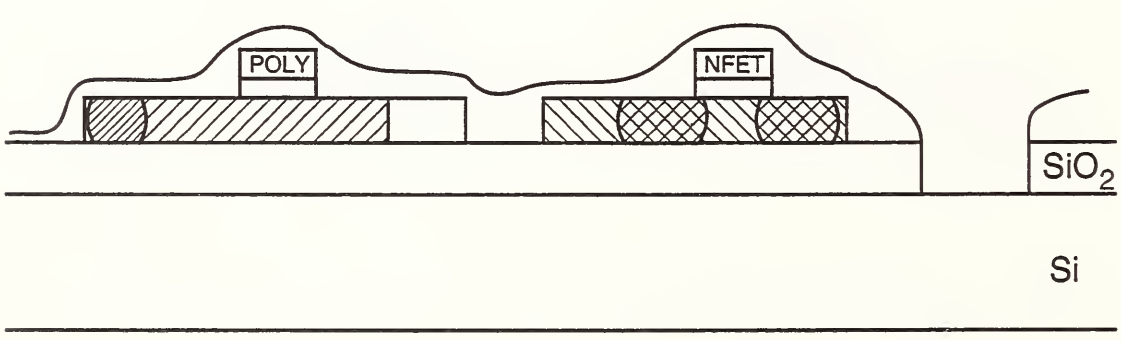
STEP 4 - POLYSILICON (a clear field mask)



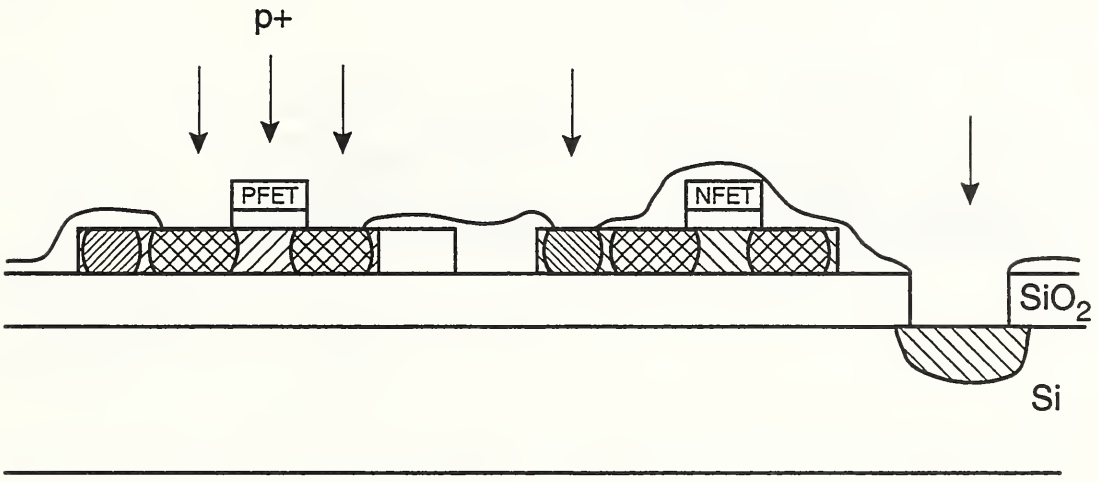
STEP 5 - NDIFFUSION (a dark field mask)



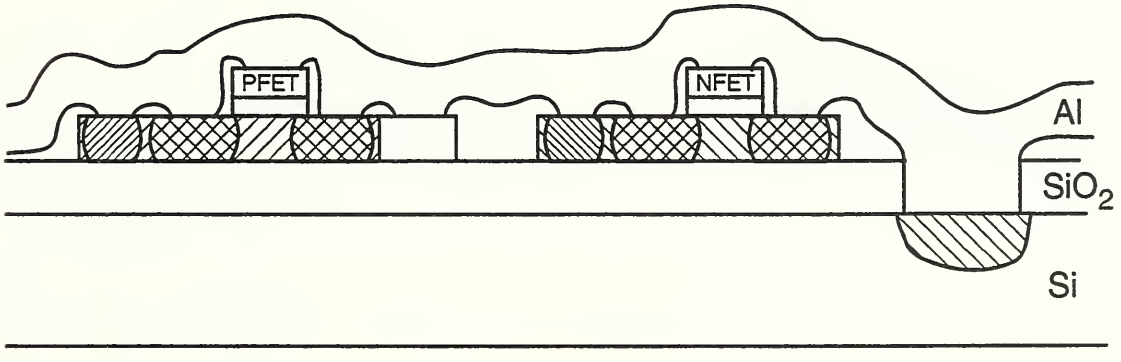
STEP 6 - SUBSTRATE CONTACT (a dark field mask)



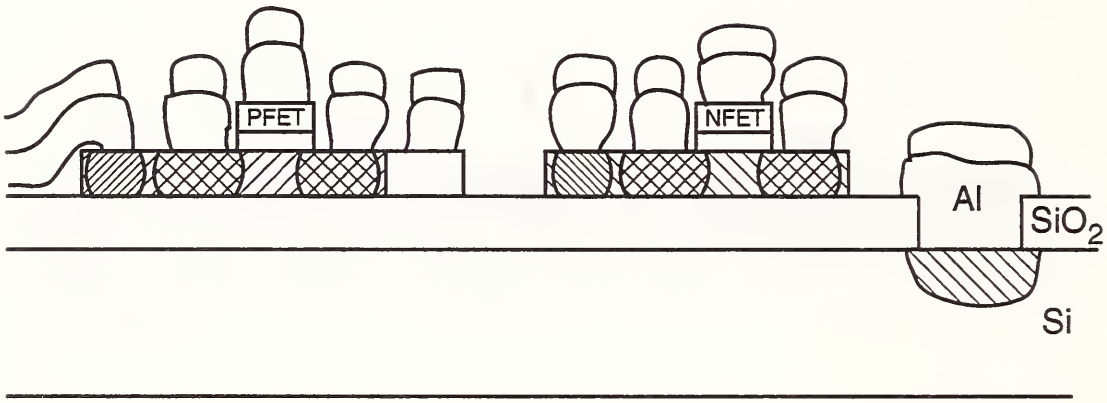
STEP 7 - PDIFFUSION (a dark field mask)



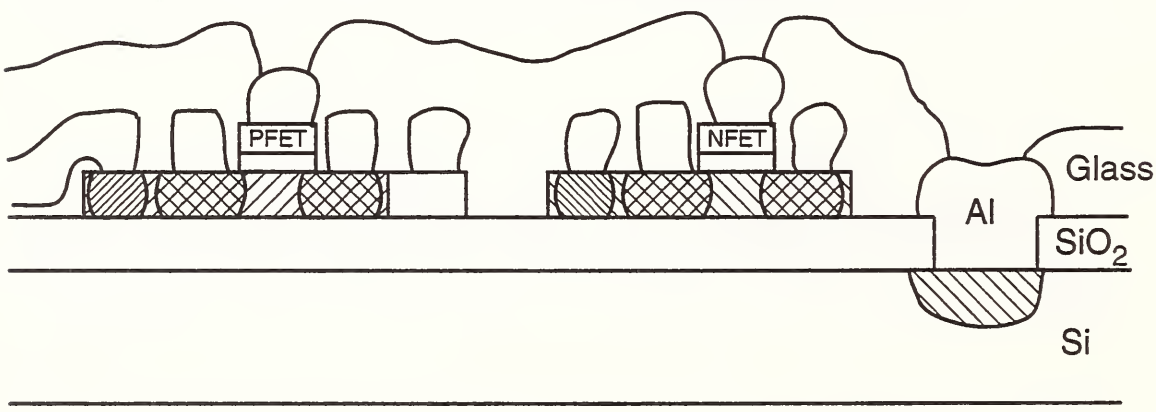
STEP 8 - SUBSTRATE CONTACT & OTHER CONTACTS
(dark field masks)



STEP 9 - METAL (a clear field mask)



STEP 10 - GLASS (a dark field mask)



Appendix B - The SIMOX Design Rules

	Rule	Width (μm)	Spacing (μm)	Misc. (μm)
1.1	nwell	6		
1.2	nwell		4*	
1.3	pwell	6		
1.4	pwell		4*	
2.1	allDiff**	6		
	allDiffO**	6		
2.2	allDiff		3*	
2.3	ndiff,ndc,nfet to pdiff,pdc,pfet		8	
	ndiff,nfet,ndc to nwell		8	
	pdiff,pfet,pdc to pwell		8	
2.4	ndiff,ndc,nfet to nwc,nndiff		8	
	pdiff,pdc,pfet to pwc,ppdiff		8	
	nwc,nndiff to pwc,ppdiff		8	
	nwc,nndiff to pwell		8	
	pwc,ppdiff to nwell		8	
3.1	allPoly**	6		
3.2	allPoly		2	
3.3	gate overlap			5
3.4	transistor diffusion overhang			3
3.5	poly,pc to ndiff,pdiff,ndc,pdc, nndiff,ppdiff,nwc,pwc		1	
4.1	nfet to pwc,ppdiff		3	
	pfet to nwc,nndiff		3	
4.2	ndiff,ndc,nfet to pwc,ppdiff		4	
	pdiff,pdc,pfet to nwc,nndiff		4	
5.1,2,3	pc	4		
5.4,5	pc to allPoly		3	
5.6	pc to allDiff		1	
6.1,2,3	ndc	4		

	pdc	4	
	nwc	4	
	pwc	4	
	ndpc	4	
	pdpc	4	
	ilc	4	
	m2c	4	
	subcon	4	
6.4,5	ndc,pdc,nwc,pwc to allDiff		4
6.6	ndc,pdc,nwc,pwc to nfet,pfet		2
6.7	ndc,pdc,nwc,pwc to poly,pc		1
6.8	island contacts must be on a flat surface (no poly or diffusion edges inside contact)		
6.9	pc to ndc,pdc,nwc,pwc		2
7.1	allMetal1**	6	
7.2	allMetal1		6
8.1	m2	6	
8.2	m2		6
8.3	glass	6	
8.4	glass		6
9.1	allIsland**	6	
9.2	allIsland		8
10	pc,ndpc,pdpc,ndc,pdc,nwc,pwc, ilc, and subcon must be rectangular		

All contacts	8x8μm (before CIF)	4x4μm (after CIF)
Metal pad	8x8μm (before CIF)	8x8μm (after CIF)
Other pad	8x8μm (before CIF)	8x8μm (after CIF)

Avoid coincident edges amongst island, polysilicon, and metal
Polysilicon to island (when the polysilicon is used as a runner) 2μm
Metal to island (when the metal is used as a runner) 2μm
Make polysilicon contacts on the substrate (not an island), if possible

```
* Not applicable because we designed one MOSFET per island.

** allDiff = ndiff,pdiff,ndc,pdc,nndiff,ppdiff,nwc,pwc,nfet,pfet
   allDiff0 = nwc,pwc,nndiff,ppdiff
   allPoly = poly,pc,nfet,pfet,ndpc,pdpc
   allMetal1 = m1,pc,ndpc,pdpc,ndc,pdc,nwc,pwc,ilc,subcon
   allIsland = il,ilc
```

```
/* ------------------------------------------------------------ *
 * simox.tech -- The SIMOX Technology File for lambda=1.0       *
 * ------------------------------------------------------------*/

tech
    simox
end

planes
    substrate,subst
    active,diffusion,polysilicon,act
    metal1,m1
    metal2,m2
    metal3,m2c
    island,il
    well,w
end

types

    /* primary layers */

    substrate  glass
    metal3     metal2c,metal3,m2c,via
    metal2     metal2,m2,purple
    metal1     metal1,m1,blue
    active     polysilicon,red,poly,p
    active     ndiffusion,green,ndiff
    active     pdiffusion,brown,pdiff
    active     nndiff
    active     ppdiff
    well       nwell,nw
    well       pwell,pw
    island     island,il,yellow
    substrate  substrate,subst

    /* Contacts */

    active     polycontact,pcontact,pc
    active     ndpcontact,ndpc
    active     pdpcontact,pdpc
    active     ndcontact,ndc
    active     pdcontact,pdc
    active     nwcontact,nwc
    active     pwcontact,pwc
    metal1     ilcontact,ilc
    metal1     subcon

    /* Transistors */

    active     ntransistor,nfet
```

```
    active      ptransistor,pfet

end

contact
    pc          poly        metal1
    ndpc        nfet        metal1
    pdpc        pfet        metal1
    ndc         ndiff       metal1
    pdc         pdiff       metal1
    nwc         nndiff      metal1
    pwc         ppdiff      metal1
    ilc         island      metal1
    subcon      substrate   metal1
end

styles
    styletype mos

    glass       34
    m2          21
    m1          20
    poly         1
    nfet         6
    nfet         7
    pfet         8
    pfet         9
    ndiff        2
    pdiff        4
    nndiff       3
    ppdiff       5
    nwell       12
    pwell       13
    il          11
    substrate   10

    m2c         33
    pc           1
    pc          20
    pc          32
    ndpc         6
    ndpc         7
    ndpc        20
    ndpc        32
    pdpc         8
    pdpc         9
    pdpc        20
    pdpc        32
    ndc          2
    ndc         20
    ndc         32
    pdc          4
    pdc         20
    pdc         32
```

```
    nwc          3
    nwc         20
    nwc         32
    pwc          5
    pwc         20
    pwc         32
    ilc         20
    ilc         11
    ilc         32
    subcon      20
    subcon      10
    subcon      32
    subcon      34

    error_p     42
    error_s     42
    error_ps    42
end

compose
    compose     nfet poly ndiff
    compose     pfet poly pdiff

    /* The rules below allow nwell to be painted over an area to
     * flip all p-well structures to n-well structures and vice versa.
     */

    paint       nwell           pwell     pwell
    paint       pdc/active      pwell     ndc/active
    paint       pdc/m1          pwell     ndc/m1
    paint       pfet            pwell     nfet
    paint       pdiff           pwell     ndiff
    paint       nndiff          pwell     ppdiff
    paint       nwc/active      pwell     pwc/active
    paint       nwc/m1          pwell     pwc/m1

    paint       pwell           nwell     nwell
    paint       ndc/active      nwell     pdc/active
    paint       ndc/m1          nwell     pdc/m1
    paint       nfet            nwell     pfet
    paint       ndiff           nwell     pdiff
    paint       ppdiff          nwell     nndiff
    paint       pwc/active      nwell     nwc/active
    paint       pwc/m1          nwell     nwc/m1
end

#define allSomeM1 m1,pc/m1,ndpc/m1,pdpc/m1,ndc/m1,pdc/m1
#define allMetal1 allSomeM1,nwc/m1,pwc/m1,ilc/m1,subcon/m1
#define allPoly poly,pc/active,nfet,pfet,ndpc/active,pdpc/active
#define allNdiff ndiff,ndc/active,nndiff,nwc/active,nfet,ndpc/active
#define allPdiff pdiff,pdc/active,ppdiff,pwc/active,pfet,pdpc/active
#define allSomeD ndiff,pdiff,ndc/active,pdc/active,nndiff,ppdiff
#define allDiff allSomeD,nwc/active,pwc/active,nfet,pfet
#define allDiff0 nndiff,ppdiff,nwc/active,pwc/active
```

```
#define allNwell nw,nwc/active
#define allPwell pw,pwc/active
#define allIsland il,ilc/il
#define allSub subst,subcon/subst

connect
    allMetal1           allMetal1
    allPoly             allPoly
    ndiff               ndc
    ndiff               ndpc
    pdiff               pdc
    pdiff               pdpc
    nwell,nwc,nndiff    nwell,nwc,tndiff
    pwell,pwc,ppdiff    pwell,pwc,ppdiff
    allIsland           allIsland
    allSub              allSub
end

/* WARNING ::::: automatic generation of wells does not guarantee   */
/* rules on width and spacing of wells are followed !!              */
/* It is strongly recommanded that designers layout their own wells */

cifoutput
style mosis(SCE)
    scalefactor 100
    layer CWN allNwell
          calma 1 1
    layer CWP allPwell
          calma 2 1
    layer CMS m2
          grow 300
          calma 3 1
    layer CMF allMetal1
          calma 4 1
    layer CPG allPoly
          calma 5 1
    layer CAA allNdiff,allPdiff
          calma 6 1
    layer CVA m2c
          grow 100
          calma 7 1
    layer CSN ndiff,nfet
          grow 200
          calma 8 1
          or allNdiff
    layer CSP pdiff,pfet
          grow 200
          or allPdiff
          calma 9 1
    layer CCA ndc,pdc,pwc,nwc
          shrink 200
          calma 10 1
    layer CCP pc,ndpc,pdpc
          shrink 200
```

```
            calma 11 1
        layer COG glass
            calma 12 1

    style photronix
        scalefactor 100
        layer SWN allNwell
            calma 40 1
        layer SWP allPwell
            calma 41 1
        layer SIL allIsland
            calma 42 1
        layer SMF allMetal1
            calma 43 1
        layer SPG allPoly
            calma 44 1
        layer SND allNdiff
            calma 45 1
        layer SPD allPdiff
            calma 46 1
        layer SCT ndc,pdc,nwc,pwc,pc,ilc,ndpc,pdpc
            shrink 200
            calma 47 1
        layer SCS subcon
            shrink 200
            calma 48 1
        layer SOG glass
            calma 49 1

    end

    /* ------------------------------------------------------------------ *
     * In the CIFinput section, the order of layer specifications is very  *
     * important.  Each layer overrides any of the previous layers.  There *
     * are places where one layer is generated over an area that is too    *
     * large, but with the knowledge that later layers will "take over"    *
     * the extraneous area, leaving the first layer only where it belongs. *
     * This happens for various flavors of diffusion, for example.         *
     * Note: when reading in CMOS, wells are created in the Magic files.   *
     * They can be eliminated manually if desired.                         *
     * ------------------------------------------------------------------*/

    cifinput
    style mosis(SCE)
        scalefactor 100
        layer nw CWN
        layer pw CWP
        layer m2c CVA
        layer m2 CMS
        layer m1 CMF
        layer poly CPG
        layer il CAA
        layer nndiff CSN
            and CWN
```

```
layer ppdiff CSP
      and CWP
layer ndiff CSN
      and-not CWN
layer pdiff CSP
      and-not CWP
layer nfet CPG
      and CAA
      and CSN
layer pfet CPG
      and CAA
      and CSP
layer pdc CCA
      and CAA
      and CSP
      and CMF
layer ndc CCA
      and CAA
      and CSN
      and CMF
layer pwc CCA
      and CAA
      and CSP
      and CMF
      and CWP
layer nwc CCA
      and CAA
      and CSN
      and CMF
      and CWN
layer pc CCP
      and CPG
      and CMF
      and-not CSN
      and-not CSP
layer ndpc CCP
      and CPG
      and CMF
      and CSN
layer pdpc CCP
      and CPG
      and CMF
      and CSP
layer glass COG

calma CWN 1 *
calma CWP 2 *
calma CMS 3 *
calma CMF 4 *
calma CPG 5 *
calma CAA 6 *
calma CVA 7 *
calma CSN 8 *
calma CSP 9 *
```

```
    calma CCA 10 *
    calma CCP 11 *
    calma COG 12 *

style photronix
    scalefactor 100
    layer nw SWN
    layer pw SWP
    layer il SIL
    layer ml SMF
    layer poly SPG
    layer ndiff SND
    layer pdiff SPD
    layer nndiff SND
          and SWN
    layer ppdiff SPD
          and SWP
    layer ndiff SND
          and-not SWN
    layer pdiff SPD
          and-not SWP
    layer nfet SPG
          and SND
    layer pfet SPG
          and SPD
    layer ilc SCT
          and SIL
          and SMF
    layer ndc SCT
          and SND
          and SMF
          and SIL
    layer pdc SCT
          and SPD
          and SMF
          and SIL
    layer nwc SCT
          and SND
          and SWN
          and SMF
          and SIL
    layer pwc SCT
          and SPD
          and SWP
          and SMF
          and SIL
    layer pc SCT
          and SPG
          and SMF
          and-not SND
          and-not SPD
    layer ndpc SCT
          and SPG
          and SMF
```

```
        and SND
    layer pdpc SCT
        and SPG
        and SMF
        and SPD
    layer substrate SCS
        grow 200
    layer subcon SCS
        and SMF
    layer glass SOG

    calma SWN 40 *
    calma SWP 41 *
    calma SIL 42 *
    calma SMF 43 *
    calma SPG 44 *
    calma SND 45 *
    calma SPD 46 *
    calma SCT 47 *
    calma SCS 48 *
    calma SOG 49 *

end

/* ================================*/
/* the SIMOX DESIGN RULES   */
/* ================================*/
drc
/* ------------------------------------------------------------- */
/* 1.1 & 1.2 */
    width nwell 6 \
        "N-Well width must be at least 6 (rule #1.1)"

    spacing nwell nwell 4 touching_ok \
        "N-Well spacing must be at least 4 (rule #1.2)"

/* 1.3 & 1.4 */
    width pwell 6 \
        "P-Well width must be at least 6 (rule #1.3)"

    spacing pwell pwell 4 touching_ok \
        "P-Well spacing must be at least 4 (rule #1.4)"

/* ------------------------------------------------------------- */
/* 2.1 & 2.2 */
    width allDiff 6 \
        "Diffusion width must be at least 6 (rule #2.1)"

    width allDiff0 6 \
        "Ohmic Diffusion width must be at least 6 to assure the well width
            (rule #1.1)"

    spacing allDiff allDiff 3 touching_ok \
        "Diffusion spacing must be at least 3 (rule #2.2)"
```

```
/* 2.3 */
    spacing ndiff,ndc/active,nfet pdiff,pdc/active,pfet 8 touching_illegal \
          "P-type diffusion must be 8 away from N-type diffusion (rule
                #2.3)"

    spacing ndiff,nfet,ndc/active nwell 8    touching_illegal \
          "N-diffusion and N-well must be separated by 8 (rule #2.3)"

    spacing pdiff,pfet,pdc    pwell     8    touching_illegal \
          "P-diffusion and P-well must be separated by 8 (rule #2.3)"

/* 2.4 */
    spacing ndiff,ndc,nfet nwc/active,nndiff 8 touching_illegal \
          "N-type diffusion must be 8 away from Nwell contact (rule #2.4)"

    spacing pdiff,pdc,pfet pwc/active,ppdiff 8 touching_illegal \
          "P-type diffusion must be 8 away from Pwell contact (rule #2.4)"

    spacing nwc/active,nndiff pwc/active,ppdiff  8  touching_illegal \
          "Opposite well contacts must be separated by 8 (rule #2.4)"

    spacing nwc/active,nndiff pwell     8    touching_illegal \
          "Nwell diffusion and P-well must be separated by 8 (rule #2.4)"

    spacing pwc/active,ppdiff nwell     8    touching_illegal \
          "Pwell diffusion and N-well must be separated by 8 (rule #2.4)"

/* ------------------------------------------------------------ */
/* 3.1 */
    width allPoly 6 \
          "Polysilicon width must be at least 6 (rule #3.1)"

    edge4way   poly,pc/active pfet 3    pfet 0    0 \
          "Transistors must be at least 3 units wide (rule #3.1)"

    edge4way   poly,pc/active nfet 3    nfet 0    0 \
          "Transistors must be at least 3 units wide (rule #3.1)"

/* 3.2 */
    spacing allPoly allPoly 2 touching_ok \
          "Polysilicon spacing must be at least 2 (rule #3.2)"

/* 3.3 */
    edge4way nfet,pfet poly,pc/active  5  poly,pc/active poly,pc/active 2 \
          "Poly must overhang transistor by at least 5 (rule #3.3)"

/* 3.4 */
    edge4way nfet ndiff,ndc/active 3 ndiff,ndc/active,nfet ndiff,ndc/active
                  2 \
          "Diffusion must overhang transistor by at least 3 (rule #3.4)"

    edge4way pfet pdiff,pdc/active 3 pdiff,pdc/active,pfet pdiff,pdc/active
          2 \
```

```
        "Diffusion must overhang transistor by at least 3 (rule #3.4)"

    edge4way   nfet,pfet space     1    poly 0    0 \
        "Transistor overhang is missing (rule #3.4)"

/* 3.5 */
    edge4way ndiff,pdiff,ndc,pdc,nndiff,ppdiff,nwc/act,pwc/act poly,pc 1
                space 0 1 \
        "Poly and diffusion must be separated by at least 1 (rule #3.5)"

    edge4way poly,pc ndiff,pdiff,ndc,pdc,nndiff,ppdiff,nwc/act,pwc/act 1
                space 0 1 \
        "Poly and diffusion must be separated by at least 1 (rule #3.5)"

    edge  poly,pc  space  1  space  space  1 \
        "Poly and diffusion must be separated by at least 1 (rule #3.5)"

    edge  ndiff,pdiff,ndc,pdc,nndiff,ppdiff,nwc/act,pwc/act space 1 space
                space 1 \
        "Poly and diffusion must be separated by at least 1 (rule #3.5)"

/* ------------------------------------------------------------ */
/* 4.1 */
    spacing nfet    pwc/active,ppdiff   3    touching_illegal \
        "Transistors must be separated from well contacts by 3 (rule
                #4.1.a)"

    spacing pfet    nwc/active,nndiff   3    touching_illegal \
        "Transistors must be separated from well contacts by 3 (rule
                #4.1.b)"

/* the following rules are over-estimated check for some unlikely situations
*/

    edge4way nwc/act,nndiff ~(nwc,nndiff,pdiff,pdc)/active 5 ~(pfet)/active
                nwc/act,nndiff,pdc,pdiff 3 \
        "Transistors must be separated from selects(generated by well
                cont) by 3 (rule #4.1.c)"

    edge4way pwc/act,ppdiff ~(pwc,ppdiff,ndiff,ndc)/active 5 ~(nfet)/active
                pwc/act,ppdiff,ndc,ndiff 3 \
        "Transistors must be separated from selects(generated by well
                cont) by 3 (rule #4.1.d)"

    edge4way  nwc,nndiff ~(pdiff,pdc,nwc,nndiff)/active 5 ~(pfet)/active
                ~(pdiff,pdc,nwc,nndiff)/active 5 \
        "Transistors must be separated from selects(generated by well cont)
                by \3 (rule #4.1.e)"

    edge4way  pwc,ppdiff ~(ndiff,ndc,pwc,ppdiff)/active 5 ~(nfet)/active
                ~(ndiff,ndc,pwc,ppdiff)/active 5 \
        "Transistors must be separated from selects(generated by well cont)
                by 3 (rule #4.1.f)"
```

```
/* 4.2 */
    edge4way ~(ndiff,ndc,nfet)/active ndiff,ndc,nfet 4 ~(pwc,ppdiff)/active
                    \     ndiff,ndc,nfet 2 \
          "Backedge of diffusion must be 4 from well diff (rule #4.2)"

    edge4way ~(pdiff,pdc,pfet)/active pdiff,pdc,pfet 4 ~(nwc,nndiff)/active
                    \     pdiff,pdc,pfet 2 \
          "Backedge of diffusion must be 4 from well diff (rule #4.2)"

    edge4way nwc/act,nndiff pdiff,pdc,pfet 3 pdiff,pdc,pfet pdiff,pdc,pfet 3
                    \
          "Pdiff must be 3 wide if it abuts nwc or nndiff (rule #2.1+4.2)"

    edge4way pwc/active,ppdiff ndiff,ndc,nfet 3 ndiff,ndc,nfet
                    ndiff,ndc,nfet 3 \
          "Ndiff must be 3 wide if it abuts pwc or ppdiff (rule #2.1+4.2)"

/* ------------------------------------------------------------ */
/* 5.1 & 5.2 & 5.3*/
    width pc 4 \
          "Contact width must be at least 4 (rule #5B.1,2,3)"

/* 5.4 & 5.5 --
 * Watch out here:  a spacing "touching_ok" rule CANNOT be used here:
 * it will miss certain checks.
 */
    edge4way  allPoly  ~(allPoly)/active  3  ~pc/active  ~(allPoly)/active
                    3 \
          "Poly contact must be at least 3 from other poly (rule #5B.4,5)"

/* 5.6 --
 * This is mostly handled by 3.5 already, but need rule here to handle
 * case of pc abutting transistor.
 */
    spacing pc allDiff 1 touching_illegal \
          "Poly contact must be 1 unit from diffusion (rule #5B.6)"

/* ------------------------------------------------------------ */
/* 6.1 & 6.2 & 6.3*/
    width ndc 4 \
          "N-Diffusion contact width must be at least 4 (rule #6.1,2,3)"

    width pdc 4 \
          "P-Diffusion contact width must be at least 4 (rule #6.1,2,3)"

    width nwc 4 \
          "Nwell contact width must be at least 4 (rule #6.1,2,3)"

    width pwc 4 \
          "Pwell contact width must be at least 4 (rule #6.1,2,3)"

    width ndpc 4 \
          "ndpc width must be at least 4 (rule #6.1,2,3)"
```

```
    width pdpc 4 \
          "pdpc width must be at least 4 (rule #6.1,2,3)"

    width ilc 4 \
          "Island contact width must be at least 4 (rule #6.1,2,3)"

    width m2c 4 \
          "M2c width must be at least 4 (rule #6.1,2,3)"

    width subcon 4 \
          "Substrate contact width must be at least 4 (rule #6.1,2,3)"

/* 6.4 & 6.5 --
 * Watch out here:  a spacing "touching_ok" rule CANNOT be used here:
 * it will miss certain checks.
 */
    edge4way  allDiff  ~(allDiff)/active  4  ~(ndc,pdc,nwc,pwc)/active \
                  ~(allDiff)/active  4 \
           "Diffusion contacts must be 4 from other diffusions (rule
                  #6.4,5)"

/* 6.6 -- already handled by rule 3.5 */
    spacing ndc/act,pdc/act,nwc/act,pwc/act nfet,pfet 1 touching_illegal \
          "Diffusion contacts must be 2 away from transistors (rule #6.6)"

/* 6.7 */
    spacing ndc/act,pdc/act,nwc/act,pwc/act poly,pc/act 1 touching_illegal \
          "Diffusion contact to field poly must be at least 1 (rule #6.7)"

/* 6.8 */
    /* Don't allow poly or diffusion edges underneath island contacts: */

    edge4way  allPoly  ~(allPoly)/active  1  ~ilc/island \
                  ~(allPoly)/active  1 \
          "Island contacts must be on a flat surface (rule #6.8)" island

    edge4way  allDiff  ~(allDiff)/active  1  ~ilc/island \
                  ~(allDiff)/active  1 \
          "Island contacts must be on a flat surface (rule #6.8)" island

    edge4way  ~(allPoly)/active allPoly  1  ~ilc/island allPoly  1 \
          "Island contacts must be on a flat surface (rule #6.8)" island

    edge4way  ~(allDiff)/active  allDiff  1  ~ilc/island allDiff  1 \
          "Island contacts must be on a flat surface (rule #6.8)" island

/* 6.9*/
    spacing pc/act ndc/act,pdc/act,nwc/act,pwc/act 2 touching_illegal \
          "Poly contacts must be 2 away from diffusion contacts (rule #6.9)"

/* ------------------------------------------------------------ */
/* 7.1 & 7.2 */
    width allMetal1 6 \
          "Metal1 width must be at least 6 (rule #7.1)"
```

```
    spacing allMetal1 allMetal1 6 touching_ok \
          "Metal1 spacing must be at least 6 (rule #7.2)"

/* ------------------------------------------------------------ */
/* 8.1 & 8.2 */
    width m2 6 \
          "Metal2 width must be at least 6 (rule #8.1)"

    spacing m2 m2 6 touching_ok \
          "Metal2 spacing must be at least 6 (rule #8.2)"

/* 8.3 & 8.4 */
    width glass 6 \
          "Glass width must be at least 6 (rule #8.3)"

    spacing glass glass 6 touching_ok \
          "Glass spacing must be at least 6 (rule #8.4)"

/* ------------------------------------------------------------ */
/* 9.1 & 9.2 */
    width allIsland 6 \
          "Island width must be at least 6 (rule #9.1)"

    spacing allIsland allIsland 8 touching_ok \
          "Island spacing must be at least 8 (rule #9.2)"

/* ------------------------------------------------------------ */
/* 10 */
    /* Contacts must all be rectangular (no adjacent contacts
     * of same type).  This is handled using the corner checks
     * in the rules below.  Overlaps between contacts must be exact
     * overlaps.  The only exception is oversubcon, which doesn't
     * matter.
     */
    edge4way   pc/m1     ~pc/m1    1    ~pc/m1        (~pc,pc)/m1    1 \
          "Polysilicon contacts must be rectangular (rule #10)"

    edge4way   ndpc/m1   ~ndpc/m1  1    ~ndpc/m1   (~ndpc,ndpc)/m1  1 \
          "ndpc contacts must be rectangular (rule #10)"

    edge4way   pdpc/m1   ~pdpc/m1  1    ~pdpc/m1   (~pdpc,pdpc)/m1  1 \
          "pdpc contacts must be rectangular (rule #10)"

    edge4way   ndc/m1    ~ndc/m1   1    ~ndc/m1       (~ndc,ndc)/m1  1 \
          "N-diffusion contacts must be rectangular (rule #10)"

    edge4way   pdc/m1    ~pdc/m1   1    ~pdc/m1       (~pdc,pdc)/m1  1 \
          "P-diffusion contacts must be rectangular (rule #10)"

    edge4way   nwc/m1    ~nwc/m1   1    ~nwc/m1       (~nwc,nwc)/m1  1 \
          "Nwell contacts must be rectangular (rule #10)"

    edge4way   pwc/m1 ~pwc/m1 1 ~pwc/m1      (~pwc,pwc)/m1  1 \
```

```
        "Pwell contacts must be rectangular (rule #10)"

    edge4way   ilc/il    ~ilc/il   1    ~ilc/il   (~ilc,ilc)/il  1 \
        "Island contacts must be rectangular (rule #10)"

    edge4way   subcon/m1  ~subcon/m1    1  ~subcon/m1    (~subcon,subcon)/m1
                  1 \
        "Subcon contacts must be rectangular (rule #10)"

/* overlapping rules */
    exact_overlap ilc,ndc,pdc,pc,pwc/m1,nwc/m1
    no_overlap pfet,nfet pfet,nfet
/* ------------------------------------------------------------------------ */
end

extract

style lambda=1.0

    lambda     100
    step  100

/*--------------------------------------------------------------------------*/
/* sheet resistivity                      milli-ohms per square */

    resist     m2                                          33
    resist     metal1,m2c,ilc,subcon                       49
    resist     poly,pc/active,nfet,pfet,ndpc,pdpc       30000
    resist     ndiff,nmdiff                             40000
    resist     pdiff,ppdiff                            110000
    resist     ndc/active,nwc/active                    50000
    resist     pdc/active,pwc/active                   100000
    resist     nwell,il                               3500000
    resist     pwell                                  3500000

/*--------------------------------------------------------------------------*/
/* area capacitance to well (GND)       atto-farads/lambda**2 */

    areacap    m2                                  16
    areacap    metal1,m2c                          26
    areacap    poly,pc/active                      57
    areacap    ndiff,ndc/active                   220
    areacap    pdiff,pdc/active                   270

/*  areacap    nfet,pfet                          930            *
 * not needed because in the MODEL card for SPICE this value is included */

/*--------------------------------------------------------------------------*/
/* sidewall capacitance to well (GND)              atto-farads/lambda */

    perimc     poly,pc/active      space,nwell,pwell    80
    perimc     ndiff,ndc/active    space,pwell         550
    perimc     pdiff,pdc/active    space,nwell         350
```

```
/*-------------------------------------------------------------------*/
/* overlap coupling capacitance                    aF/lambda**2   shield*/

    overlap    m2         metal1                        44
    overlap    m2         poly                          22        metal1
    overlap    m2         ndiff,pdiff,nndiff,ppdiff     22        metal1
    overlap    metal1     poly                          47
    overlap    metal1     ndiff,pdiff,nndiff,ppdiff     47

/*-------------------------------------------------------------------*/
/* transistors */

    fet   nfet ndiff,ndc        2  nfet  GND!      0   0
    fet   pfet pdiff,pdc        2  pfet  Vdd!      0   0

end

/*-------------------------------------*/
wiring
    contact pc  8 metal1 0 poly   0
    contact ndpc 8 metal1 0 nfet 0
    contact pdpc 8 metal1 0 pfet 0
    contact ndc 8 metal1 0 ndiff  0
    contact pdc 8 metal1 0 pdiff  0
    contact nwc 8 metal1 0 nndiff  0
    contact pwc 8 metal1 0 ppdiff  0
    contact ilc 8 metal1 0 island 0
    contact subcon 8 metal1 0 substrate 0
end

/*-------------------------------------*/
router

    layer1 metal1 6 allMetal1,glass 6
    layer2 poly 6 allPoly 6 allDiff,nw,pw,ilc,subcon 4
    contacts pc 8
    gridspacing 14
end

/*-------------------------------------*/
plowing
    fixed nfet,pfet,glass
    covered nfet,pfet
    drag nfet,pfet
end

/*-------------------------------------*/
plot
end
```

Appendix D - The Magic layers, CIF names, and Calma numbers (as found in the cifoutput section of the technology file) Associated with the Ten SIMOX masks.

MASK	MAGIC LAYERS INCLUDED	SIMOX CIF NAME	CALMA NUMBER
1. allNwell	nwell nwc	SWN	40
2. allPwell	pwell pwc	SWP	41
3. allIsland	island ilc	SIL	42
4. allMetal1	metal1 pc ndc pdc nwc pwc ilc subcon ndpc pdpc	SMF	43
5. allPoly	poly pc nfet pfet ndpc pdpc	SPG	44
6. allNdiff	ndiff ndc nwc nfet nndiff ndpc	SND	45
7. allPdiff	pdiff pdc pwc pfet ppdiff pdpc	SPD	46
8. contacts atop the island	ndc pdc nwc pwc	SCT	47

	pc ilc ndpc pdpc		
9. substrate contacts	subcon	SCS	48
10. glass	glass	SOG	49
A TOTAL OF 10 MASKS			

Appendix E - A Computer Program to Determine the Appropriate Dimensions for the RF Transistors

```
C
C     FILENAME:  RFP.FOR
C
C     PURPOSE:  THIS PROGRAM OBTAINS THE DIMENSIONS FOR AN RF TRANSISTOR.

C               A 50 OHM INPUT IMPEDANCE NEEDS TO BE MATCHED.
C               NOTE: USE MICRONS !
C
      DIMENSION NUMFILE(50), FILN1(50), FILN2(50)
C
      open(unit=10, file='in.dat', status='old')
      open(unit=20, file='out.dat', status='old')
C
      c=3.06e8*1.e6                    ! speed of light
      e0=8.85e-14*100e-6               ! in F/micron
      ersio2=3.9                       ! for SiO2
      esi=11.8                         ! for Si
C     ersio2=11.6                      ! for GaAs
C
C     read the data in.....
C
      read (10,*) s                    ! electrode width
      read (10,*) w0                   ! electrode spacing
      w=w0
C
C     perform the following calculations
C
500   er=esi
      ak=s/(s+2*w)
      akp=sqrt(1.-ak**2.)
C
      if ((ak .ge. 0.) .and. (ak .le. (sqrt(2.))/2.)) go to 10
      if ((ak .ge. (sqrt(2.))/2.) .and. (ak .le. 1.)) go to 11
C
      write (20,702)
702   format(1x,'ak in the wrong ballpark')
      go to 900
C
10    akratio=1./((1./3.1416)*alog(2.*(1.+sqrt(akp))/(1.-sqrt(akp))))
      go to 16
11    akratio=(1./3.1416)*alog(2.*(1.+sqrt(ak))/(1.-sqrt(ak)))
C
16    z0=1./(2.*sqrt(2.)*e0*c*sqrt(er+1.)*akratio)
C
C     write the value of z0 in out.dat
C
      write (6,700) s,w,z0
70    format(1x,'s=',F8.2,15x,'w=',F8.2,15x,'z0=',F8.2)
C
```

```
      if (z0 .lt. 50.) w=w+10.
      if (z0 .lt. 50.) go to 500
      write (20,700) s,w,z0
C
      s=s+10.
      w=w0
      if (s .gt. 200.) go to 900
      go to 500
C
900   CONTINUE
      END
```

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The design guidelines for test chips NIST3 and NIST4 are specified in this manual. These chips were designed for process monitoring and device parameter extraction for a CMOS (Complementary Metal-Oxide-Semiconductor)-on-SOI (Silicon-On-Insulator) process. The chips contain structures which are common to a standard CMOS process as well as structures specifically designed for a SIMOX (Separation by the IMplantation of OXygen) process. In order to facilitate the CAD process, a unique "technology file" was created for the Magic VLSI layout editor used on a Sun-3/280 system running Sun Version 3.5. This SIMOX technology file is very general and can be used to build CMOS as well as SIMOX chips.

NIST3 is 6380 μm × 4780 μm and contains several large-geometry MOSFETs, resistors, and capacitors. NIST4 is 1 cm × 1 cm and contains approximately 300 small-geometry test structures. The SIMOX specific structures found on these chips include MOSFETs, capacitors, interconnects, and pads to be discussed in more detail.

The test guide for the test structures on NIST3 and NIST4 is included in a separate manual.

12. KEY WORDS (6 TO 12 ENTRIES; ALPHABETICAL ORDER; CAPITALIZE ONLY PROPER NAMES; AND SEPARATE KEY WORDS BY SEMICOLONS)

CAD; Magic; MOSFET; NIST3; NIST4; SIMOX; SOI; test chip; test structure

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