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Double-Level Metallization: Annual Report for October 1, 1985 to September 30, 1986

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U.S. DEPARTMENT OF COMMERCE
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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

TABLE OF CONTENTS

LIST OF TABLES

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ABSTRACT

An outline for a double-level metal process for the fabrication of circuits having a minimum linewidth of 3 μm is described. The process is designed to be implemented in the Microelectronics Processing Facility at Fort Meade, Maryland, where single-level metallization circuits are already in production. A summary is included of the research performed in the Semiconductor Processing Research Laboratory at the National Bureau of Standards.

Key words: double-level metallization; integrated circuit processing; interlevel dielectric; microelectronic processing; polyimide; semiconductor processing; test structures.

DISCLAIMER

Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

I. INTRODUCTION

The double-level metal research and development project of the National Security Agency (NSA) and the National Bureau of Standards (NBS) was conducted during the period September 1985 to August 1986. The project was a collaborative effort to investigate certain double-level metallization materials and processes using improved test structures and processing techniques.

A. Objective

The major objective was to provide information for the development of a double-level metallization capability for NSA's 3-μm CMOS process and for other applications to be implemented in NSA's Microelectronics Processing Facility.

B. Benefits and Results

Research and development conducted in NBS's Semiconductor Processing Research Laboratory provided the knowledge and skills necessary to propose a practical

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double-level metallization process. This report contains details of the proposed process, background information to support the chosen process techniques, and a summary of the work performed. This report is presented to assure that the benefits and results of our work are immediately available for actual implementation in the NSA facility. Recommendations for test structures to characterize and monitor the process are presented in an Appendix.

During the study, as we gained understanding and learning from the laboratory work, we were able to make decisions to improve upon the initially envisioned work plan. This enabled us to make the best of our limited time and resources. The result of this flexible approach, based upon a growing understanding, is what we consider to be an optimal process to meet the needs of NSA and to best utilize NSA's existing and expected processing equipment.

C. Considerations

To achieve the work objectives in the best way, certain practical considerations were taken into account as they became apparent. Some of these considerations were:

Not all materials met performance expectations. Some of the interlevel dielectrics were eliminated from further study because they had inferior properties, such as unstable electrical characteristics and poor thermal stability.

Test structure work requires the process to be determined. The originally planned work on test structures could not be fulfilled because the design of production test structures depends strongly on the process and materials; production test structures are designed to address yield-limiting factors in a specified process. A specific process was not identified at the outset. Existing NBS research test structures were used for the laboratory development.

Only the process development work could be done. The planned work was divided between the NBS and NSA facilities to assure that the processing and characterization techniques developed are appropriate to the production equipment at NSA. Research was carried out in NBS's Semiconductor Processing Research Laboratory. However, due to critical production demands on the NSA production facility, portions of the work related to implementation could not be carried out at NSA.

Increased knowledge yielded a better prospective. During this project, we learned a great deal and developed a large amount of expertise. This knowledge has given us the insight to evaluate recent trends occurring in industry and new advances reported in the literature.

II. A PROPOSED PROCESS

The process outlined here is compatible with existing or expected equipment at NSA. The materials and procedures have been shown to perform to the requirements.

A. Description

First-Level Metal Material: Aluminum with 1% silicon

Thickness: 1.0 μm

Deposition method: Sputtering

Deposition equipment: Varian Model 3118 or Perkin Elmer Model 4450

Etching method: Either wet chemical, plasma, or reactive ion

Etching equipment: Tegal Model 702 Dry Etching System or scheduled LAM 690 reactive ion etching system

Interlevel Dielectric Material: Silicon dioxide (undoped)

Thickness: 1.5 μm

Deposition method: Low temperature chemical vapor deposition (CVD)

Deposition equipment: Very low pressure CVD furnace

Etching method: Wet chemical

Second-Level Metal Material: Aluminum (or aluminum with 1% silicon)

Thickness: 1.0 μm

Deposition method: Sputtering

Deposition equipment: Varian Model 3118 or Perkin Elmer Model 4450

Etching method: Either wet chemical, plasma, or reactive ion

Etching equipment: Tegal 702 Dry Etching System or scheduled LAM 690 reactive ion etching system

B. Suitability

First-Level Metal

The first-level metal (Metal 1) suggested for the double-level metallization process for 3-μm design rules is an aluminum with 1% silicon alloy. This metallization is currently used in NSA's existing 3-μm single-level process. Metal 1 can be sputtered in NSA's existing Perkin Elmer Model 4450. Metal 1 can either be wet or dry etched. A wet etch process exists for etching aluminum with 1% silicon with the required geometries. The alloy can also be etched in NSA's Tegal 702 Dry Etching System. A dry etching process has already been developed for etching this alloy.

A barrier refractory metal (Ti:W, 10% weight Ti) has been shown to reduce hillock growth [1]. In a typical application, aluminum is deposited on a Ti:W film which acts as a barrier layer between the underlying silicon and the aluminum.

However, it has been shown that hillock growth and electromigration-related problems are not concerns in a 3-μm process [2]. Further development work may be required to confirm that these phenomena are not a problem.

The addition of titanium and copper to the aluminum has been used to improve interconnect reliability and may be of use in this process. An aluminum with 1% silicon alloy with 0.4% titanium added has been shown to reduce electromigration effects [1]. Copper (1-4%) added to the alloy has been used traditionally also to reduce electromigration effects. The copper-containing alloy may be more difficult to etch without leaving a residue. The barrier alloy (Ti:W) and the titanium-containing aluminum alloy can be deposited in the Perkin Elmer Sputtering System.

Interlevel Dielectric

For a process with 3-μm design rules, a 1.5-μm thick layer of nonplanarized, undoped CVD material is suggested as the interlevel dielectric. The following considerations lead to the choice of this thickness:

1. The dielectric-to-Metal 1 thickness ratio must be greater than 1.5 to avoid problems with re-entrant angles.

2. When the dielectric film thickness is greater than half the minimum spacing between Metal 1 features, bridging can occur across trenches, resulting in the formation of voids in the dielectric.

Since the Metal 1 thickness in the 3-μm single-level metal process at NSA is 1 μm, and the metal-to-metal minimum spacing is 3 μm, the interlayer dielectric is restricted to a thickness of 1.5 μm, assuming the metal thickness is kept the same in the double-level metal process.

Undoped, rather than phosphorus-doped, CVD oxide is the dielectric of choice since the phosphorus is necessary only to reflow the oxide. The temperature required to reflow the oxide is approximately 900°C, which is above the melting point of aluminum. Also, if phosphorus-doped oxide were used as the intermetal dielectric, then a layered combination of undoped-doped-undoped oxide must be fabricated. Phosphorus-doped oxide, in the presence of moisture, can form phosphoric acid, which can etch aluminum. The "sandwich" structure is necessary to separate the aluminum and phosphorus-doped oxide. However, such a sandwich of oxides presents a problem in the etching of the vias because undoped and doped oxides etch at different rates. For these reasons, it is recommended that undoped rather than doped CVD oxide be used as the inter-metal dielectric.

Implementing low-temperature CVD oxide as the inter-metal dielectric requires no additional equipment at NSA. A low-temperature oxide furnace tube is already used in production for depositing CVD oxide as the pre-Metal 1 dielectric. This same tube could be used to deposit the inter-metal dielectric.

Metal 2

The material for the second level metal (Metal 2) is an aluminum-1% silicon

alloy. The NSA design rules dictate a thickness of 1.0 μm and linewidth of 5.0 μm. A process for depositing and wet etching aluminum already exists at NSA. Aluminum with 1% silicon can be sputtered in the Varian S-Gun System or in the Perkin Elmer 4450. The Al-Si alloy can be easily wet etched or dry etched in the Tegal 702 Dry Etching System, or dry etched in the expected LAM 690 reactive ion etching system.

C. Implementation

It has been shown that planarization of the interlevel dielectric may not be necessary for a 3-μm process [2]. Test chip results will provide the information necessary to determine whether step coverage is a yield-limiting factor that could be remedied by planarization of the interlevel dielectric or by sloping the walls of the vias. If a planarization technique is needed, it could be performed in NSA's Drytec RIE 100S System. In this system, vias are cut through the interlevel oxide by a resist-erosion process to achieve sloped walls for good Metal 2 step coverage into the vias.

Another consideration is the deposition of undoped CVD oxide by plasma-enhanced CVD (PECVD). PECVD oxide is deposited at a lower temperature than conventional CVD oxide. Test chip results and junction depth measurements, along with computer modeling, could be performed to determine whether the temperature at which CVD oxide is deposited is low enough to avoid design-rule violations or any detrimental material effects.

III. SUMMARY OF COMPLETED RESEARCH

Most of the work performed was on the characterization of inter-metal dielectric materials, particularly polyimides, spin-on-glasses, and CVD oxides. Deposition and etching processes were developed and evaluated for each of these dielectrics. The thickness uniformity of the dielectric across the wafer, planarization properties over steep topographies, breakdown voltages, leakage currents, dielectric constants, chemical and/or physical interactions with metal layers, and etching properties were measured.

A. Polyimides

Five polyimides were investigated: Ciba-Geigy XU 284, Ciba-Geigy XU 285, Dupont Pyralin 2555, Hitachi P1QB, and General Electric SPI 2000.

Processing of polyimides is complex. It involves a "curing" procedure in which the polyimide is heated first at relatively low temperatures (80°C to 150°C) to remove solvents and then at higher temperatures (240°C to 450°C) to harden the polyimide.

1. Process Development and Characterization

<u>XU 284 and XU 285</u>

Bare silicon wafers were coated with XU 284 and with XU 285. XU 284 is the more viscous polyimide and results in a thicker layer.

The preparation procedure was as follows:

a. Apply diluted adhesion promoter (1 part XU 289 concentrate with 9 parts XU 290 dilutent) with a pipet. (Shelf life of this mixture is 48 h.)

b. Spin on adhesion promoter: 5000 rpm, 20 s. (A dehydration bake is suggested by the manufacturer to promote adhesion. This bake was not performed.)

c. Spin on polyimide at 3000 rpm for 45 s. A dropper was used to dispense XU 284 as the high viscosity made use of a pipet impractical.

d. Cure: 85°C for 30 min on a hot plate;
150°C for 15 min on a hot plate; and
240°C for 15 min in an oven.

One wafer had an additional cure at 400°C for 15 min. A commercial thin film thickness measurement system was used to measure the film thicknesses. This instrument works by measuring the reflected light intensity at normal incidence as a function of the incident light wavelength for wavelengths in the visible range. The index of refraction is needed to deduce the film thicknesses using this instrument. Some of the polyimide manufacturers specify the refractive indexes of their materials. The thin film measurement system uses a default value for the refractive index of polyimides of 2.0. The resulting thickness measurement is inversely proportional to the refractive index entered in the system.

The manufacturer's value for the index of refraction of pre- and post-cured XU 284 and 285 is 1.61. The index of refraction measured on five wafers using a research ellipsometer at a wavelength of 632.8 nm is as follows:

TABLE 1. WAFERS PROCESSED WITH XU 284 and XU 285.

Wafer Number	Polyimide	Index of Refraction
1	XU 285, uncured	Inconclusive
2	XU 285, cured	1.51
3	XU 284, uncured	1.49
4	XU 284, cured	1.89
5	XU 284, cured	1.46

We were often not able to determine the refractive index of polyimides by ellipsometry because of high optical absorption of the films. We do not know how the manufacturers measured the published indexes.

The film thickness measurements in the following table were obtained using the thin film measurement system. The manufacturer's data sheets specify expected film thicknesses of 2.4 and 1.0 μm for XU 284 and XU 285, respectively, after curing according to the spinning and curing cycles we used.

TABLE 2. THICKNESS MEASUREMENTS ON XU 284 AND XU 285 FILMS.

Wafer Number	Cured	Uniformity Across the Wafer	Ellipsometrically Measured Index of Refraction	Measured Film Thickness (μm)
2 XU 285	yes	±7.0%	1.51	0.62
4 XU 284	yes	±6.7%	1.89	1.45
3 XU 284	no	±14.0%	1.49	2.11

The film thickness values are the average at five points on each wafer: in the center, about an inch above and below center, and about 2.5 cm to each side of center (with the major flat at bottom). There is a considerable loss of film thickness during the curing cycle. The film thickness measurements do not agree well with the manufacturer's thickness curves.

Once the polyimide is spun onto the wafer, it must be cured within a few hours. Otherwise, the polyimide condenses into large puddles on the wafer. Even after the curing process, these polyimides appear to be "soft" and are easily scratched with metal tweezers during routine wafer handling.

Pyralin 2555

The processing schedule for Pyralin 2555 was as follows:

a. Apply 3 cc to bare silicon wafers with a pipet.

b. Spin wafers #1 and #2 at 3500 rpm for 60 s.
Spin wafers #3 and #4 at 3000 rpm for 60 s.

c. Soft bake on a hot plate: 30 min at 140°C.

d. Cure: 300°C for 30 min in an oven;
400°C for 30 min in a furnace; and
450°C for 10 min in a furnace.

e. Rinse with a 1% solution of acetic acid.

f. Rinse in deionized water.

The published index of refraction of pre- and post-cured Pyralin 2555 is 1.7. The thickness measurement results are given below:

TABLE 3. THICKNESS MEASUREMENTS ON PYRALIN FILMS.

Wafer Number	Cured	Average Film Thickness (μm)	Uniformity Across the Wafer	Index of Refraction Used to Measure Film Thickness
1	yes	2.14	±7%	1.7 (manufacturer)
2	no		Inconclusive	
3	yes	2.39	±2%	1.7 (manufacturer)
1	yes	2.52	±0.3%	1.46 (ellipsometry)

We were not able to determine the index of refraction of the uncured film due to high absorption and nonuniform thickness.

During handling, Pyralin 2555 seemed to be more resistant to scratches than other polyimides. Also, cleaning of residue from containers and utensils is easier than cleaning residues of other polymides; when rinsed with water, 2555 forms a white, milky, plastic substance which is easily peeled off surfaces.

Hitachi P1QB

P1QB polyimide was processed as follows:

a. Spin at 3000 rpm for 30 s.

b. Cure: 95°C for 1 h on a hot plate;
220°C for 1 h in an oven; and
350°C for 1 h in a furnace.

The manufacturer's data sheets do not provide an index of refraction; but they indicate that this processing schedule should yield a thickness of approximately 2.5 μm.

We were not able to obtain an index of refraction or thickness using ellipsometry because the absorption of the material was too high. A thickness of 2.46 μm was obtained using the thin film measurement system and inserting a value of 2.0 for the index of refraction.

General Electric SPI 2000

The processing schedule used for SPI 2000 was as follows:

a. Dispense 2.5 cc of polyimide.

b. Spin at 400 rpm for 55 s, then spin at 2000 rpm for 30 s.

c. Cure: 60°C for 15 min on a hot plate;
120°C for 30 min on a hot plate;
200°C for 30 min on a hot plate; and
410°C for 30 min in a furnace.

The cured SPI 2000 polyimide film was dark brown and relatively soft compared to other polyimides; normal wafer handling with metal tweezers made imprints on the surface. Measurements with the thin film measurement system and the ellipsometer yielded inconclusive thickness and index of refraction results.

2. Capacitance and Breakdown Voltage Measurements

Capacitance-voltage (C-V) measurements were performed on two types of structures: metal/polyimide/silicon and metal/polyimide/metal. The first structure is not normally found in a double-layer metallization process, but it is useful for determining certain electrical characteristics of a dielectric.

From the high frequency (1-MHz) C-V curves, the flat-band voltage and the thickness of each of the polyimide films were determined. No evidence of excessive amounts of trapped charge, interface charge, or pinholes was detected.

The electrical thickness of the polyimide films were calculated from the C-V curve by the following formula:

$$t = \varepsilon_{ox} A/C,$$

where ε_{ox} is the dielectric constant of the dielectric, A is the area of the metal gate, and C is the accumulation capacitance of the dielectric. In the absence of other data, we took the dielectric constant to be the square of the real part of the index of refraction.

The "electrical" thickness was compared to the "optical" thickness. In most cases, the agreement was poor, often different by as much as a factor of two, due to the uncertainty in the value and frequency dependence of the index of refraction.

Current leakage measurements were also made on the polyimide films at a positive 5-V bias. As a reference, a capacitor with 100-nm thick thermal oxide as the dielectric was measured to have a leakage current of 5×10^{-12} A/cm^2. The leakage currents of the 1- to 2-μm thick polyimides were in the range of 2 to 4 $\times 10^{-12}$ A/cm^2.

3. Etching Properties

In a practical process, windows are etched in the intermetal dielectric to form "vias" to connect the second level metallization to the first. The slope of the edges of the vias must be relatively smooth and not too steep so that the second metal layer can maintain good continuity as it goes into the via.

A barrel-type plasma etcher was used to etch vias for our studies. Patterned CVD oxide was used to mask the polyimide. The etched wafers were dipped in a 2% solution of hydrofluoric acid for 6 s prior to Metal 2 deposition to clear the Metal 1 surface in the via.

Van der Pauw resistor test structures [3,4] on Test Chip NBS-30 were used to evaluate the metal-to-metal contact resistance. Specific contact resistivity results obtained with XU 284 and Pyralin 2555 were in the range expected for good metal-to-metal contact.

Poor results were achieved with the SPI 2000 and P1QB polyimides. The SPI-2000 polyimide decomposed during the deposition of the CVD oxide.

4. Step Coverage Measurements

Evaluation of step coverage was performed using Test Chip NBS-28 [5]. The test chip contains structures having serpentine metal lines running perpendicularly over polysilicon lines with the dielectric in between. In our tests, Metal 1 was substituted for polysilicon.

Preliminary results demonstrated good step coverage properties for Pyralin and SPI 2000 polyimides, but not for the XU and P1QB Polyimides. Poor adhesion of Metal 2 to the XU and P1QB polyimides resulted in entire Metal 2 structures lifting off. This adhesion problem was corrected on P1QB by first depositing CVD oxide over the polyimide, stripping it off, and then immediately depositing the Metal 2 layer.

When adhesion was good, the maximum number of steps in the test chip (62,400) was often reached successfully for each of the polyimides. In the small number of structures where open circuits were found, the arrays were examined optically and the open circuit was revealed to be caused by a processing defect.

B. CVD Oxide

Characterization of low temperature chemical vapor deposited oxide (LTO) for use as an inter-metal dielectric was performed in a manner similar to the polyimides.

1. Process Characterization

A process was developed in NBS's LTO furnace for depositing undoped oxide. The deposition parameters closely match the process currently in use at NSA for depositing LTO. Thickness uniformity of the oxide in the range of 1.5 μm to 4.0 μm was better than ±5.0% as measured on the thin film measurement system using the 5-point measurement array described earlier.

2. Capacitance and Breakdown Voltage Measurements

The metal/LTO/silicon structures produced nonideal C-V curves. The thickness calculated from the accumulation capacitance varied over the range 320 to 980 nm for different devices on the same wafer. The optically measured thickness was 400 nm. The C-V curves showed a negative shift in flatband voltage after the application of a negative bias. A positive bias shifts the flatband voltage even more negatively. This effect is thought to be due to a slow trapping instability. This instability is due to the injection of charges from silicon into traps in the oxide. Slow trapping instabilities have been observed by others in deposited oxides, and less often in thermally grown oxides [6]. Such instabilities are not a concern when the oxide is used as an interlevel dielectric because the oxide does not come into contact with the silicon. Measurements using the metal/LTO/metal structure produced well-behaved capacitors.

Leakage tests were performed on the LTO for a 5-V bias. The leakage was approximately 5×10^{-12} A/cm^2 for 100-nm thick films. Tests using thermal oxide produced approximately the same results, verifying the high quality of the LTO.

3. Etching Properties

Evaluation of etching properties was performed using contact resistor test structures [3,4] in Test Chip NBS-30. Vias were etched using buffered hydrofluoric acid. Photoresist was used as the masking material. Metal 2 was deposited immediately after a 2% HF dip, thus preventing any oxidiation

to build up in the vias. An LTO thickness of 1.5 μm was used. No evidence of excess metal-to-metal contact resistance was found.

4. Step Coverage Measurements

Using Test Chip NBS-28 and thicknesses of 400 to 900 nm, LTO was shown to provide good step coverage for 2-μm (approx.) wide lines.

C. Spin-on-Glass

Three spin-on glass (SOG) products from Allied Chemical Corporation were evaluated. SOG yields a silicon dioxide-like film upon spin-on application and subsequent curing. The three SOGs are reported to be electrically similar and to vary only in the viscosity of the uncured product.

1. Process Development and Characterization

The SOG was deposited on bare silicon wafers and on oxide-coated wafers. The first configuration was for optical and electrical measurements; the second was to evaluate a practical configuration for an interlevel dielectric. The manufacturer suggested that the SOG be used as a smoothing layer, and that it be applied before or after the deposition of an LTO insulating dielectric layer.

The processing scheduled used is as follows:

a. Dispense 2.0 mL of SOG on a bare silicon wafer or on a wafer with a 400-nm thick film of LTO. The spin speeds used are shown in table 4.

TABLE 4. SPIN SPEEDS FOR SPIN-ON-GLASS.

SOG Type	Spin Speed (rpm)	Manufacturer's Published Thicknesses after Curing (nm)
204	3000	220
305	4000	330
407	5000	330

b. Cure: 100°C for 10 min on a hot plate; and
400°C for 1 h in a furnace.

The index of refraction was measured on the SOG-coated bare silicon wafers using ellipsometry; results are shown in table 5.

TABLE 5. INDICES OF REFRACTION OF SPIN-ON-GLASS FILMS.

SOG Type	Measured Index of Refraction	Manufacturer's Stated Index of Refraction
204	1.23	1.47
305	1.24	1.47
407	1.20	1.47

The discrepancy between our measured values and the manufacturer's claimed values may indicate that the manufacturer measured films which are chemically different than ours, possibly due to a different curing cycle.

2. Capacitance and Breakdown Voltage Measurements

Capacitance-voltage measurements were made on metal/SOG/silicon and metal/SOG/LTO/silicon MOS structures. The SOG/LTO combination produced nearly ideal C-V curves. The SOG without the LTO appeared to bubble and decompose and shorted electrically when a small voltage (5 V) was applied to the metal gate. The problem may be due to leakage current causing excessive heating and chemical breakdown of the SOG. The C-V curves also showed hysteresis. These results demonstrate that, when processed as was done for this work, the SOG cannot be used alone as an inter-metal dielectric.

One advantage of using an SOG/LTO combination as the dielectric is planarization; CVD oxide is conformal to the underlying topography while the SOG smooths the surface topologically. However, since it has been shown that planarization of the interlevel dielectric is not necessary for 3-μm geometries, no further investigation of the SOG/LTO oxide combination was undertaken.

IV. SUMMARY

Based upon the research results on spin-on-glass, polyimides, and low-temperature CVD oxide described in this report, it was concluded that an aluminum-1% silicon alloy should be used for the metallization, and updoped low-temperature silicon dioxide should be used for the interlevel dielectric for the required process. An outline for the suggested double-level metallization process is provided. Also provided (in the Appendix) is a description of improved test structures for use with a double-level metallization process.

APPENDIX

CHARACTERIZING ELECTRICALLY THE PERFORMANCE OF THE INTERCONNECT PROCESS

The implementation of a new process necessarily includes the implementation of a measurement program to evaluate and characterize the performance of the process. A successful measurement program is based on knowledge of the specifications of the process, understanding of the materials and procedures, and well-designed test vehicles and methods for testing them.

A. Test Methodology

Comprehensive test methods for monitoring a fabrication process include electrical, optical, and other physical measurements at appropriate times during the fabrication procedure. They may require planned-for regions or structures on the product wafer or on separate test wafers. In some cases, commercial equipment is used routinely and easily to monitor process steps that are common to most processes. Diagnostic measurements requiring a great deal of effort or time are reserved for process development or trouble-shooting.

Test methods performed after a particular process step or after all processing is completed, using test vehicles that are primarily electrically addressed devices, can be most valuable because they can be automated. The test devices, or test structures, should be composite structures whose design requires careful consideration and integration with the process [7]. Ideally, well-designed test structures can be used to provide accurate, sensitive, unambiguous measurements of selected parameters with simple models and with automated data acquisition and analysis.

Test structures are commonly incorporated into a chip composed only of test structures. Test chips are often inserted among product chips in several locations on the wafers, or they may be fabricated on separate wafers comprised only of test chips. The choice has implications for the testing program and the application of the measurement results.

Test structures may be intended to interrogate or extract materials, process, device, and circuit parameters, to check layout rules, and to analyze random faults and reliability. Much of the information test structures can be used to obtain may be difficult or impossible to obtain by any other means.

The implementation of a test chip and a test chip measurement program depends on a variety of factors that may change with time as the process evolves and as test results are accumulated and evaluated [8]. For a newly developed process, it is necessary to identify those parameters associated with materials and circuit characteristics that are sensitive to process control, to establish their variability, to quantify excursions from expected results, and to identify sources of process variations.

The initial test results can be used to correct or improve the process and also to identify tests that provide the information most needed to monitor the process performance, to characterize the materials, and to evaluate the critical performance parameters. When the process is determined to be stable, the initial test program, or the test chip itself, may be modified to

provide the most useful information at a reduced expenditure of time and effort.

Test data must be interpreted in association with a mathematical model. When choosing a model for the interpretation of test data, the accuracy with which the model represents the test device becomes an issue. Too simple a model or measurement can provide incorrect results or can fail to detect unacceptable device behavior. A complex model may better describe device behavior over a specified range using less accurate or more general parameters. However, a complex model requiring large amounts of data acquisition and analysis may mean in actuality that no data will be acquired or analyzed because the investment is too great.

There are no simple guidelines to choose the optimal degree of complexity or the optimal amount of data needed to characterize and monitor a particular process. In a successful test program, reliable test data is efficiently handled and evaluated so that important conclusions about the acceptability of the results can be reached quickly.

B. Key Parameters of a Double-Level Metallization Process

The pivotal attribute of a test chip measurement program is that parameters are measured and used to characterize the degree of process control and to accurately predict process performance [9]. Also important are the abilities to establish the ranges and uniformities of the parameters and to determine the correlations between their variations over a wafer, from wafer to wafer within a lot, and from lot to lot.

The parameters that should be addressed by the testing program fall into the categories of materials parameters, process parameters, layout rules, random faults, and failure mechanisms [7]. Although many of the important parameters depend on the interaction between layers, they are usually associated with one of each of the specific layers [10].

Assuming that there is an electrical test program for the existing fabrication process up to the first level metal, the parameters and information related to the Metal 2 layer and the dielectric layer may be organized as shown in table A-1.

TABLE A-1. PARAMETERS TO CHARACTERIZE DOUBLE-LEVEL METALLIZATION PROCESS STEPS.

Metal 2 Layer

Electrical behavior
- Sheet resistance
- Interconnect continuity
- Capacitance
  - --to Metal 1 layer
  - --to substrate
  - --to other conducting layers
- Contact resistance
  - --to Metal 1 layer

--to other conducting layers
Leakage to adjacent interconnects

Lithography
Etch control
Alignment
--to Metal 1 layer
--to vias
Failure mechanisms
Electromigration resistance

Dielectric Layer

Thickness and thickness uniformity
Defect density
Isolation
Metal 2 to Metal 1 leakage
Fixed and mobile charge density
Charge injection and trapping
Effects of temperature, humidity, and voltage stress
Lithography
Etch control
Alignment of vias to Metal 1 layer
Failure mechanisms
Maximum dielectric strength

The types of test structures needed to obtain the required information are listed in table A-2. To interrogate the process and materials and to provide the necessary data to characterize the process fully, the structures must be designed for the specific process and processing equipment of interest. The listed references detail the design considerations for the recommended structures. Some design parameter considerations are:

Sheet Resistors. The linewidths of sheet resistors should be the minimum linewidths used in the process.

Capacitors. Capacitors should have large enough areas to provide a value of capacitance that is much larger than parasitic capacitances. The shape may be rectangular. The top capacitor plate may be used as one probe pad; if appropriate, the second connection may be made to the back of the wafer unless series resistance effects could compromise the measurement.

Contact Resistors. Contact resistors should be of the cross-bridge Kelvin design. There should be contact resistors having contact areas equal to those on the product chip and resistors having contact areas larger by a factor of two or more, to allow evaluation of the uniformity of the contacts.

Continuity Monitors. The serpentine patterns are replicated over planar and nonplanar topography formed by underlying layers. The serpentines must be relatively widely spaced to reduce the possibility of intralevel shorts. To obtain fault statistics, the structures must have

TABLE A-2. TEST STRUCTURES FOR MONITORING THE PERFORMANCE OF DOUBLE-LEVEL METALLIZATION.

Test Structure	References	Measurement	Parameters Determined
Metal 2 Split-Cross-Bridge Sheet Resistor	11,12,13	Current-Voltage	Metal 2 Sheet Resistance Metal 2 Interconnect Linewidth Metal 2 Over/Underetch Metal 2 Line Spacing
Metal 2-Substrate+ Capacitor	14	Capacitance-Voltage	Fixed and Mobile Charge Density Charge Injection and Trapping Effects of Temperature, Humidity, and Voltage Stress Maximum Dielectric Strength Oxide Integrity
Metal 2-Metal 1 Capacitor	14	Capacitance-Voltage	Dielectric Thickness and Thickness Uniformity Dielectric Integrity Maximum Dielectric Strength Metal 2-Metal 1 Capacitance Effects of Temperature, Humidity, and Voltage Stress
		Current-Voltage	Metal 2-Metal 1 Leakage Effects of Temperature, Humidity, and Voltage Stress Charge Injection and Trapping
Metal 2-Source/Drain Contact Resistor*	4,15	Current-Voltage	Specific Contact Resistivity Contact Resistivity Uniformity
Metal 2-Metal 1 Contact Resistor	4,15	Current-Voltage	Specific Contact Resistivity Contact Resistivity Uniformity

TABLE A-2. TEST STRUCTURES FOR MONITORING THE PERFORMANCE OF DOUBLE-LEVEL METALLIZATION (continued).

Test Structure	References	Measurement	Parameters Determined
Metal 2-Metal 1 Alignment Structure	16	Current-Voltage	Metal 2 x-y Misalignment with Respect to Metal 1
Via-Metal 1 Alignment Structure	16	Current-Voltage	Via x-y Misalignment with Respect to Metal 1
Metal 2 Continuity Monitors#	17,18	Electrical Connectivity	Metal 2 Step Coverage Analysis Metal 2 Continuity Fault Statistics Electromigration and Corrosion Effects of Temperature, Humidity, and Voltage Stress
Metal 2 Line Isolation Monitors#	17,18	Current-Voltage, Capacitance, and Electrical Connectivity	Metal 2 Etching Analysis Metal 2 Isolation Fault Statistics Interconnect Current Leakage Interconnect Capacitance Electromigration and Corrosion Inter- and Intra-level Breakdown Voltage Effects of Temperature, Humidity, and Voltage Stress
Via Contact Chain	18	Current-Voltage	Intermetal Contact Statistics

+Additional capacitors should be formed over each material/level over which Metal 2 interconnects are found.

*There should be a contact resistor for each material/level contacted electrically by the Metal 2 layer.

#Continuity and line isolation monitors are long serpentines formed over the planar substrate and over all appropriate topography generators (e.g., Metal 1 lines).

segments of different lengths appropriate to the process yield for the particular topography condition [7,18].

Line Isolation Monitors. The serpentines for line-to-line isolation monitoring are also replicated over planar and nonplanar topography. They should be wider than minimum linewidth to reduce the possibility of discontinuities. To obtain fault statistics, the structures must be long enough to produce isolation faults at the minimum spacing tested.

Via Contact Chain. The chains should be segmented. To produce reliable statistics, small segments should have a small enough number of contacts so the yield is almost 100%; large segments should have enough contacts to produce a low yield. The contact size should be the minimum contact size in the product chip.

As previously stated, the test structures discussed here are only those required to characterize the additional process steps and materials resulting from adding a second level of metallization to a single-level process.

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11. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)*

An outline for a double-level metal process for the fabrication of circuits having a minimum linewidth of 3 μm is described. The process is designed to be implemented in the Microelectronics Processing Facility at Fort Meade, Maryland, where single-level metallization circuits are already in production. A summary is included of the research performed in the Semiconductor Processing Research Laboratory at the National Bureau of Standards.

12. KEY WORDS *(Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)*

double-level metallization; integrated circuit processing; interlevel dielectric; microelectronic processing; polyimide; semiconductor processing; test structures

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