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Nondestructive Evaluation Activities in the Semiconductor Materials and Processes Division

R. D. Larrabee and M. I. Bell, Editors

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Semiconductor Electronics Division
Gaithersburg, Maryland 20899

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R. D. Larrabee and M. I. Bell, Editors

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
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NONDESTRUCTIVE EVALUATION ACTIVITIES IN THE SEMICONDUCTOR MATERIALS AND PROCESSES DIVISION

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ABSTRACT

This is the first in a planned series of annual reports describing the nondestructive evaluation and measurement development activities of the National Bureau of Standards in the area of semiconductor materials and devices. Present activities include production and certification of standard reference materials, development of new measurement techniques, and coordination of interlaboratory experiments and other activities of voluntary standards organizations. Standard reference materials are produced for the determination of the electrical resistivity of semiconductors and for the optical measurement of linewidths on transparent photomasks. New techniques have been developed for optical deep-level spectroscopy, resistivity and recombination lifetime profiling in ingots of very high resistivity silicon, measurement of oxygen in silicon by infrared absorption, characterization of compound semiconductor wafers by optical and x-ray techniques, and extension of photomask linewidth measurements to thicker lines on silicon substrates. Interlaboratory studies are in progress for electrical deep-level characterization, spreading resistance, and measurement of layer thickness by ellipsometry.

Key Words: deep-level spectroscopy; Fourier-transform infrared spectroscopy; gallium arsenide; linewidth resistivity; nondestructive evaluation; silicon; x-ray topography.

INTRODUCTION

The Semiconductor Materials and Processes Division and the Semiconductor Devices and Circuits Division comprise the Semiconductor Technology Program at the National Bureau of Standards (NBS).[1] This report summarizes the status of selected projects relating to the nondestructive evaluation or characterization of semiconductor materials and the fabrication processes required to make them into commercial devices and integrated circuits.[2] The reports were drafted by those actually performing the work, and the reader is referred to these individual authors for specific additional information about their projects.

[1] In October 1985, the Semiconductor Materials and Processes Division and the Semiconductor Devices and Circuits Division were combined into the Semiconductor Electronics Division.

[2] The Linewidth Metrology activity was transferred to the Center for Manufacturing Engineering early in FY-1986.

The Semiconductor Technology Program (STP) at NBS deals with measurement-related problems of importance to the semiconductor industry, its suppliers, and its customers in other industries and in the government. As part of the Department of Commerce, NBS has a responsibility for objective technical work in developing measurements and standards. Other U.S Government agencies frequently utilize and sponsor the work of the program. All of the work is related in some way to the measurement of a physical quantity such as electrical resistivity, dopant distribution, linewidth, or oxide thickness. The program includes the development and certification of standard reference materials, but does not presently offer any calibration services. Other projects are concerned with the development of new or improved test methods for characterizing semiconductor materials and processes. Program activities include the publication of technical papers and reports, organization of workshops and seminars, supervision of interlaboratory studies (round robins), and assistance to standards organizations such as the American Society for Testing and Materials (ASTM), the Semiconductor Equipment and Materials Institute (SEMI), the Joint Electron Device Engineering Council (JEDEC), and Deutsches Institut für Normung (DIN).

This report has been prepared for the NBS Office of Nondestructive Evaluation as a means of disseminating information about our current work in the broad area of nondestructive evaluation. We welcome the reader's comments and suggestions, not only about the specific projects discussed in this report, but also on how we might do a more effective or complete job in serving the semiconductor industry and the users of semiconductor products.

Descriptions of nondestructive evaluation projects in many other divisions and laboratories of NBS are available in NBSIR 85-3187, "*Nondestructive Evaluation, Technical Activities, 1985*." For further information, contact the NBS Office of Nondestructive Evaluation, Materials Building, Rm. B344, National Bureau of Standards, Gaithersburg, MD 20899.

ELECTRICAL RESISTIVITY OF EXTRINSIC SILICON

James R. Ehrstein

I. Objective

To develop the ability to measure the resistivity of silicon slices or ingot sections in which the resistivity lies in the range 5×10^{-4} to 100 Ω·cm, and is dominated by a single intentional dopant. Precision of about 5% is required for process control applications, while 1% precision is desirable for materials acceptance testing.

II. Background

Resistivity is one of the primary parameters specified in the sale of silicon for semiconductor devices. (Other primary parameters are physical dimensions and conductivity type, i.e., *p*- or *n*-type or the specific atomic species to be used for doping.) Early measurements of resistivity required sectioning of a portion of the silicon ingot to obtain a rectangular bar-shaped specimen onto which contacts were plated or pressed. For this geometrical shape, voltage and current measurements can be readily related to specimen resistivity, but the procedure is clearly destructive. Early attempts to use a mechanical fixture to apply four pointed probes under pressure to the specimen surface in order to do a four-terminal (Kelvin-type) measurement of resistivity suffered from inaccuracy and imprecision. Such measurements were nondestructive, however, in that only four small specimen areas each about 50 μm in diameter are damaged by the probes.

III. Approach

NBS involvement began about 1962, at a time when interlaboratory precision of 10% to 30% was typically achieved for resistivity measurements in the range 0.01 to 100 Ω·cm. Geometric correction factors for the finite thickness of thin circular specimens had been developed, as had an empirical knowledge of proper measurement current levels (as a function of resistivity) which would minimize the effects of Joule heating and minority carrier injection.

Early NBS contributions included the evaluation of the temperature coefficient of resistivity for measurement temperatures in the vicinity of room temperature [1], the development of geometric scaling factors for circular slices with diameters only a small multiple of the probe separation [2], a geometric correction for probes with nonuniform spacing [3], and a calculation to estimate the effects of lateral resistivity nonuniformity [4]. In addition, the use of analog test boxes was introduced to verify instrument performance, and extensive analytical and experimental tests were run to establish the errors that were introduced by various components of the measurement [5,6].

IV. Results

Ensuing interlaboratory round robins, conducted under the auspices of ASTM Committee F-1 on Electronics, showed that, with proper control of experimental conditions and appli-

cation of the full set of geometric corrections, interlaboratory precision of 0.75%, or better, can be attained over the resistivity range 0.001 to 100 Ω·cm. Using the same procedures, subsequent round robins demonstrated interlaboratory precision of 1.7% in the resistivity range 100 to 500 and 5% in the resistivity range 500 to 2000 Ω·cm.

V. Output

NBS Report 9666 was originally published to summarize the NBS contribution to this measurement development as well as the analyses of the round robins to test the multilaboratory precision up to 120 Ω·cm; this report was subsequently reprinted with the addition of the temperature coefficient of resistivity data as NBSIR 74-496 [5].

The tests required to verify proper instrument performance and to evaluate probe spacing are laborious. Further, they do not suffice to predict the quality of measurement data as influenced by the nature of the metal-to-semiconductor contacts between the probe tips and the silicon specimen. As a result, ASTM Committee F-1 petitioned NBS in the early 1970s to make available silicon resistivity standards which could be used to check the calibration of a complete four-probe measurement station.

Such a set of standards, SRM 1520, consisting of two slices of silicon with resistivity levels appropriate to the integrated circuit industry, was first made available in 1973. A second set of standards, consisting of three slices of silicon having higher resistivity values, as appropriate to the manufacture of silicon power control devices, was first made available in 1978. With the advent of eddy-current-based instruments for the rapid nondestructive measurement of resistivity, the availability of resistivity standards became even more important since eddy current instrument-gain must be calibrated against specimens of known resistivity. As a result, SRM 1523, consisting of two specimens with resistivity values specifically chosen to suit the operating characteristics of commercial eddy current instrumentation, was made available in 1980, and SRM 1520 was made available with thinner slices, more appropriate to eddy current instruments, and was renamed SRM 1521. A total of more than 500 sets of these silicon resistivity standards have been sold worldwide for calibrating four-probe or eddy current instruments.

VI. Impact

Procedures have been developed and tested to allow highly repeatable resistivity measurements to be made by four-point probe. A series of calibrated reference specimens allow rapid verification of four-point probe instrument performance, calibration of eddy current testers, and a common base for resistivity scale throughout the semiconductor industry.

VII. List of Publications

1. Bullis, W. M., Brewer, F. H., Kolstad, C. D., and Swartzendruber, L. J., Temperature Coefficient of Resistivity of Silicon and Germanium near Room Temperature *Solid-State Electronics* **11**, 639-646 (1968).

2. Swartzendruber, L. J., Correction Factor Tables for Four-Point Probe Resistivity Measurements on Thin, Circular Semiconductor Samples, NBS Tech. Note 199 (April 15, 1964).

3. Swartzendruber, L. J., private communication.

4. Swartzendruber, L. J., Four-Point Probe Measurement of Non-Uniformities in Semiconductor Sheet Resistivity *Solid-State Electronics* **7**, 413-422 (1964).

5. Bullis, W. M., Standard Measurements of the Resistivity of Silicon by the Four-Probe Method, NBSIR 74-496 (August 1974).

6. Bullis, W. M., Editor, Methods of Measurement for Semiconductor Materials, Process Control, and Devices, Quarterly Report, October 1 to December 31, 1972, NBS Tech. Note 773 (June 1973).

ELECTRICAL RESISTIVITY AND LIFETIME OF NEAR-INTRINSIC SILICON

Robert D. Larrabee

I. Objective

To measure the average bulk resistivity and minority-carrier recombination lifetime of short ingot sections or slices of high-resistivity semiconductor silicon (e.g., resistivities of 10,000 to 50,000 Ω·cm and lifetimes in the millisecond range).

II. Background

There are a wide variety of techniques that have been developed for measuring the resistivity and lifetime of extrinsic semiconductor silicon in the range of resistivities commonly used in the integrated-circuit or power-device industries (i.e., below several hundred Ω·cm). Some of these techniques may be destructive (e.g., techniques depending on ohmic contacts or electrical probing). Others are nondestructive, but have inadequate sensitivity at the low free-carrier densities in higher resistivity silicon (e.g., techniques based on eddy currents or free-carrier infrared absorption). In addition, as the resistivity increases, the relative importance of surface effects increases and gives rise to nonreproducible systematic errors. As applications for near-intrinsic high-resistivity silicon have arisen, a need has developed for rapid, practical, nondestructive, and fairly accurate methods of measuring resistivity and lifetime in this regime.

III. Approach

A. Average Resistivity of Thin Slices

A new approach to resistivity measurement is being developed that takes into account the possibility of relatively large depletion or significant accumulation layers at the specimen surfaces. The nondestructive nature of the measurement is achieved by providing removable capacitive contacts to the end surfaces of thin slices or ingot sections (front and back surfaces) as shown in figure 1A, and by measuring the complex impedance of the resulting lossy capacitor as a function of frequency. The charge-neutral internal (bulk) and the charged surface regions of the specimen are modeled by the equivalent circuit of figure 1B, and the parameters of that circuit found by fitting the model to the measured impedance data. The resistivity of the interior (bulk) region is then computed from the resulting values of the circuit parameters.

B. Profiling Lifetime and Resistivity of Ingot Sections

An electro-optic approach to nondestructive profiling is being developed that uses a 1.15-μm He-Ne laser normally incident on the end surface of the ingot to generate electron-hole pairs in the interior of a silicon ingot and senses the resulting perturbation of resistivity by radio-frequency electrical measurements using externally applied capacitive contacts. This perturbation has been analyzed and solved analytically for the case of a cylindrical

specimen with four linear contacts on the ends of two mutually perpendicular diameters and a small highly penetrating laser beam on a diameter 45° to a line joining the contacts [1], as shown in figure 2. Radial profiling is achieved by scanning the laser beam along this diameter, while azimuthal profiling is achieved by rotating the cylindrical specimen with respect to the four capacitive contacts. Axial profiling is achieved by breaking these four linear contacts into segments and measuring each segment separately. The recombination lifetime is determined by measuring the time constant of decay of the perturbation when the laser beam is turned off, and the relative resistivity is measured by analyzing the magnitude of the electrical response to turning on the laser for a fixed time interval that is short compared to the lifetime.

IV. Results

A. Average Resistivity of Thin Slices

The impedance method has been tested on slices of single-crystal semiconductor silicon in the resistivity range from about 15,000 to 30,000 Ω·cm. The results of the measurement have been shown to be relatively independent (i.e., to within about 10%) of the physical and chemical nature of the contacted surface and of the formulation of the conductive material painted on that surface to form the capacitive contacts. Experiments are currently in progress to compare the results of this impedance technique with the results of other techniques applicable in this resistivity range (which are generally destructive or otherwise impractical).

B. Profiling Lifetime and Resistivity of Ingot Sections

A facility for performing the laser-scan profiling has been built and shown to function as predicted with acceptable signal-to-noise levels for high-resistivity silicon ingots, using a 1-mW He-Ne laser at 1.15 μm. The absorption length of this infrared light is several inches, and therefore, the maximum length of the ingot sections is limited to about this value. Measured lifetimes (in the millisecond regime) are consistent with an average value determined by the conventional technique of photoconductive decay applied to the whole ingot section. The measured resistivity profiles will be checked by cutting a profiled ingot section into smaller test specimens that can be measured by the above slice-impedance method.

V. Output

A publication describing the impedance technique and the initial results summarized above is in preparation. The lifetime and resistivity profiling technique is summarized in NBSIR 83-2792 [1]. A more definitive report will be written after the profiling technique is checked by applying the slice-impedance technique to small specimens cut out of a previously profiled ingot.

VI. Impact

Several companies are participating with NBS to determine the value of these techniques as a way of monitoring the resistivity of near-intrinsic semiconductor silicon to assure compliance with purchase specifications and for in-process quality control. In addition, the Department of Defense is interested in establishing better domestic sources of high-resistivity silicon and has indicated an interest in having NBS participate in their programs to assist in the characterization of high-resistivity silicon, particularly with respect to the measurement of resistivity and minority-carrier lifetime.

VII. List of Publications

1. Larrabee, R. D., and Lowney, J. R., Measurement Techniques for High-Resistivity Detector-Grade Silicon: Progress Report, July 1, 1982 to June 30, 1983, NBSIR 83-2792 (December 1983).

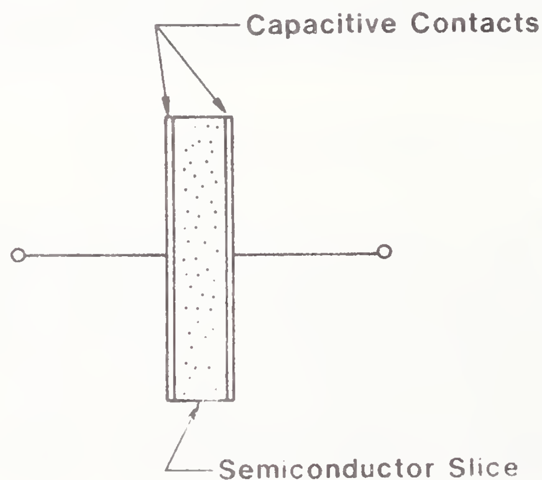

Figure 1A. Semiconductor slice or ingot section provided with capacitive contacts to form a two-terminal test device.

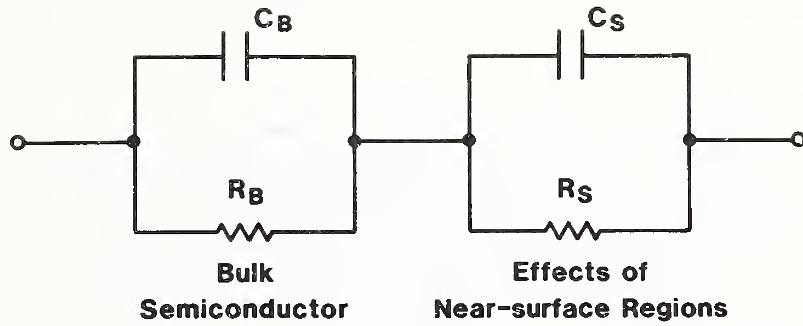

Figure 1B. Equivalent circuit of the test device of figure 1. R_B and C_B represent the bulk resistance and capacitance. R_S and C_S characterize the effects of the near-surface regions (e.g., a surface depletion region).

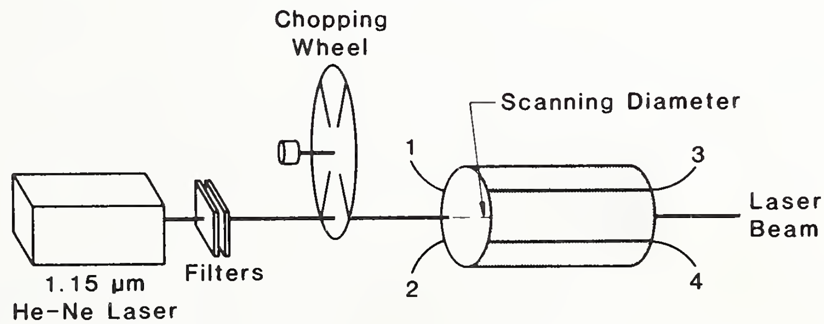

Figure 2. Schematic diagram of the laser-scan lifetime and resistivity profiling technique. The capacitive linear electrical contacts are labeled 1, 2, 3, and 4.

DEEP-LEVEL TRANSIENT SPECTROSCOPY OF SEMICONDUCTOR DEVICES

Jeremiah R. Lowney

I. Objective

To determine the densities, energies, and capture cross sections of deep levels in semiconductor devices.

II. Background

Deep levels are electronic states deep within the energy gap of a semiconductor which are caused by impurities and defects and which can alter or degrade device performance. Some are present in the starting material while others are either accidentally or intentionally added during device fabrication. Since these levels can affect the performance of a device, it is imperative that techniques be available to characterize them. An important technique for doing so is deep-level transient spectroscopy (DLTS). This technique generally measures the liberation of carriers trapped in deep levels when the ambient carrier densities are modulated with either an optical or an electrical pulse. The liberated carriers are measured either by a collected current or by a change in diode capacitance if a diode test device is used. The most common method is to change the reverse bias of a diode abruptly and repetitively and measure the change in capacitance as a function of time as carriers are thermally emitted from deep levels in the space-charge region during the period of greater reverse bias. The measurements may be made at a constant temperature or as the temperature is slowly swept. In conventional DLTS, the temperature is swept, and the capacitance is measured at two times during the transient. The difference in capacitance at these two times is then plotted as a function of the temperature. A peak in the signal is observed at a temperature determined by the so-called rate window given by a known relation between the two measurement times. The rate window is equal to the emission rate of carriers from the trap at that temperature. It is possible to determine the position of a level in the energy gap from the emission rate, and the density of the level from the amplitude of the signal. Trap concentrations can be determined to about one part in a thousand. Subsequent measurements of the filling of the levels with majority carriers (and, if possible, minority carriers) are needed to determine the majority and minority capture cross sections. These measurements are more difficult and involve pulsing the diode rapidly either electrically or optically. From all these data, one can predict the effect of the deep levels on the net carrier density and recombination lifetime of the semiconductor material used to make the device.

III. Approach

A difficulty in the general acceptance of deep-level transient spectroscopy has been that inconsistencies in the results of measurements made at different laboratories have led to distrust of the method. The goal of the NBS effort has been to make the method reliable by improving the control inherent in the instrumentation and the rigor obtained in the

theoretical interpretation. To achieve this goal, a special cryostat was built which can measure and control the temperature of the sample to within 0.1 K. A digital oscilloscope is used to collect the capacitance transients associated with the emission of trapped carriers. These data are taken isothermally, because this method is more accurate than one based on temperature sweeping. The data are then transferred to a computer for analysis. The theory of data analysis is based on a solution of Poisson's equation which takes into account that traps are initially filled with carriers in only part of the space-charge region and that traps do not emit in another part of the space-charge region because they lie below the quasi-Fermi energy. From this theory, simple relations have been derived which are useful in reducing the data and providing accurate values of the deep-level parameters.

A second aspect of this work has been to investigate deep levels in semi-insulating GaAs with a technique called photoresistance deep-level transient spectroscopy (PR-DLTS). An optical pulse is used to generate excess carriers, and the ac resistance of the sample is measured as the traps return to thermal equilibrium. This technique is truly nondestructive because the contacts may be removed after the measurement.

IV. Results

The most recent work centers on the interpretation of nonexponential transients which occur when the trap density is larger than 10% of the dopant density on the lightly doped side of the junction. A method was devised for determining if nonexponentiality of the transient is a problem [1]. A shift in the temperature corresponding to the peak of the DLTS signal is taken as a sign of nonexponentiality when the two times at which the capacitance is measured are varied while maintaining a constant rate window. A theoretical formula was deduced to correct for nonexponentiality so that it is possible to determine the correct emission rate in this case [2]. This formula involves the steady-state capacitances when the diode is biased to fill the traps and when fully reverse biased, as well as that at the beginning of the transient just after the larger reverse bias is restored. Formulas applicable to both isothermal measurements as well as conventional DLTS were derived. This work enables the proper determination of trap energy and resolves a source of disagreement in the literature. Further work is presently being done to obtain improved analysis of trap density.

The PR-DLTS method [3] has yielded good agreement with other techniques such as the dc current-transient method known as photoinduced transient spectroscopy (PITS). Measurements were made on a wide range of samples grown by both horizontal Bridgman and liquid encapsulated Czochralski techniques. Many deep levels were identified.

V. Output

Results of this work have been published [1-6], both as reports to sponsors and in archival journals. Platinum-doped silicon diodes are being produced and, once fully characterized, will serve as an aid for researchers and technicians so that more reliable measurements can be made. Through participation in round robins and interactions with the ASTM, the staff have helped engineers in the field to appreciate better the utility of the method. An ASTM test method is being devised and interactions with various companies who manufacture DLTS and related equipment are continuing.

VII. List of Publications

1. Thurber, W. R., Forman, R. A., and Phillips, W. E., A Novel Method to Detect Nonexponential Transients in Deep Level Transient Spectroscopy, *J. Appl. Phys.* **53**, 7397-7400 (1982).

2. Thurber, W. R., Lowney, J. R., and Phillips, W. E., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1, 1982 to March 31, 1983, NBSIR 84-2838 (U.S.G.P.O., Washington, DC, 1984), p. 4.

3. Seabaugh, A. C., Bell, M. I., Larrabee, R. D., and Oliver, J. D., Jr., High-Frequency Transient-Resistance Spectroscopy of Deep Levels in SI GaAs, in *Semi-Insulating III-V Materials: Kah-nee-ta 1984*, D. C. Look and J. S. Blakemore, Eds. (Shiva Publishing, Ltd., Cheshire, England, 1984), pp. 437-445.

4. Lowney, J. R., Larrabee, R. D., and Thurber, W. R., The Relationship Between Deep-Level Measurements and Lifetime in Devices, *IEEE Proc. Custom Integrated Circuits Conference*, Rochester, New York, May 23-25, 1983, pp. 152-156.

5. Phillips, W. E., and Lowney, J. R., Analysis of Nonexponential Transient Capacitance in Silicon Diodes Heavily Doped with Platinum, *J. Appl. Phys.* **54**, 2786-2791 (1983).

6. Phillips, W. E., Thurber, W. R., and Lowney, J. R., Improved Analysis Procedures for Deep-Level Measurements by Transient Capacitance, *Defects in Silicon* **83-9**, W. M. Bullis and L. C. Kimerling, Eds., pp. 485-490 (Electrochemical Society, Pennington, New Jersey, 1983).

ELLIPSOMETRIC TECHNIQUES OF MATERIALS CHARACTERIZATION

George A. Candela and Deane Chandler-Horowitz

I. Objective

To develop supporting theory and models and to determine optimum measurement conditions for variable angle/wavelength ellipsometry of single and multiple layers of materials used for photomasks and integrated circuits.

To develop, certify, and issue step-height and layer-thickness standard reference materials (SRMs) for silicon dioxide films on single-crystal semiconductor silicon.

II. Background

Thin films of electrically insulating silicon dioxide on semiconductor silicon are used extensively in integrated circuits. In particular, the characteristics of the thin silicon dioxide gate of metal-oxide-semiconductor (MOS) devices are of particular interest because this oxide forms part of the active region of these devices. The need for improved characterization techniques and for tighter standards in thin-film metrology is increasing as the demands on these films increase (e.g., smaller thickness, increased radiation resistance, ability to withstand higher voltages, etc.). Ellipsometry provides a practical and accurate way to measure the thickness and index of refraction of such films. The thickness is important as a critical device parameter that affects performance (e.g., threshold voltage), and the index of refraction is of interest because it provides a measure of the physical condition of the film (e.g., density, composition, microstructure, etc.). Ellipsometry is inherently nondestructive as the probe is a low-intensity beam of light.

The applications of ellipsometry for the characterization of integrated circuit structures extend beyond single films of silicon dioxide on silicon. Other types of films of interest include: photoresist films used for patterning; silicon nitride films used for passivation; and polysilicon films used for conductive lines. These films are usually not deposited on the semiconductor silicon substrate, but on top of some other film (e.g., a film of photoresist on top of a silicon dioxide layer about to be patterned). Multilayer structures such as these have more parameters of interest (e.g., thickness and index of refraction of each layer), and the resulting ellipsometric characterization must provide a correspondingly greater number of independent measurements. This is usually accomplished by making the ellipsometric measurements at several selected angles of incidence (multi-angle ellipsometry) or over a range of wavelengths (spectroscopic ellipsometry).

III. Approach

The approach being pursued for improving ellipsometric metrology involves three basic steps. First, a fully automated state-of-the-art research-grade ellipsometer has been constructed. Second, a complete error analysis of the various ellipsometric methods is in

progress in order to determine how best to use the instrument to minimize the errors of measurement of selected material parameters. Third, a set of SRMs (several thicknesses of silicon dioxide films on silicon) is being developed for the calibration of ellipsometric and other optical and mechanical thickness measurement techniques.

IV. Results

The basic research ellipsometer has been built and is nearing its final stages of check-out and optimization. A complete analytic error analysis for single transparent films on an opaque substrate has been developed and implemented in a computer (FORTRAN) program. This program allows one to design the details of a test specimen (e.g., film thickness) and the ellipsometric parameters (e.g., angle of incidence) to optimize the measurement for any given material property (e.g., real part of the index of refraction of the film). Future plans include extending this approach to multilayer structures. A developmental thin-film SRM has been designed; prototypes are being evaluated, and the procedures for its certification are being developed.

V. List of Publications

The following publications describe some of the recent ellipsometric work:

1. Chandler-Horowitz, D., and Candela, G. A., Principal Angle Spectroscopic Ellipsometry Utilizing a Rotating Analyzer, *Applied Optics* **21**, 2972 (1982).

2. Chandler-Horowitz, D., Ellipsometric Accuracy and the Principal Angle of Incidence, *Proc. Soc. Photo-Optical and Instrumentation Engineers* **342**, *Integrated Circuit Metrology*, 121 (1982).

3. Chandler-Horowitz, D. and Candela, G. A., On the Accuracy of Ellipsometric Thickness Determinations of Very Thin Films, *J. de Physique* **44**, C10-23 (December 1983).

4. Candela, G. A. and Chandler-Horowitz, D., An Ellipsometry System for High Accuracy Metrology of Thin Films, *Proc. Soc. Photo-Optical and Instrumentation Engineers* **480**, *Integrated Circuit Metrology II*, 2 (1984).

5. Chandler-Horowitz, D., Ellipsometric Metrology of Ultrathin Films: Dual Angle Measurements, *Proc. Soc. Photo-Optical and Instrumentation Engineers* (to be published).

6. Chandler-Horowitz, D., *Semiconductor Measurement Technology:* Analytic Analysis of Ellipsometric Errors, NBS Special Publication 400-79 (to be published).

OPTICAL LINEWIDTH MEASUREMENTS

Diana Nyyssonen

I. Objective

To develop optical measurement and calibration techniques for accurate linewidth measurements of 0.5- to 10-μm features patterned on integrated-circuit photomasks, reticles, wafers, and in photoresist.

To develop, certify, and issue photomask, reticle, and silicon-wafer standard reference materials (SRMs).

II. Background

Accurate linewidth measurements are needed by the integrated circuit (IC) industry to ensure that optical, electron-beam, and x-ray lithographic systems, as well as critical dimension measuring systems, perform to specifications and to ensure that the corresponding lithographic patterning and etching processes are under control and produce feature sizes within the required tolerances. Optical linewidth measurements are inherently nondestructive as the probe is a low-intensity beam of light. In recent years, the minimum feature size of commercial integrated circuits has decreased steadily and is presently approaching the submicrometer regime. As feature sizes approach the wavelength of the light used for their measurement, diffraction effects and the three-dimensional nature of the features and edge geometry become dominant and begin to seriously affect the measurement. Therefore, new and specialized techniques are required for accurate measurement at these small dimensions.

III. Approach

Two basic approaches are being pursued depending upon the nature of the specimen. For features patterned in thin layers, i.e., less than approximately one-quarter of the illuminating wavelength, accurate measurements can be made using coherent, bright-field microscopy in either: (1) transmitted light using a tungsten-halogen source (opaque photomasks on a transparent glass substrate), or (2) reflected (incident) light using an ion-laser source (integrated circuit structures). Algorithms have been developed for accurate edge detection and linewidth measurement using the scalar theory of partially coherent imaging of thin layers in a microscope. This approach is practical for linewidths greater than approximately 0.5 μm (for a wavelength of 530 nm). For lines of smaller dimensions, the diffraction effects from the optical system dominate, and shorter wavelengths must be used.

The second approach was developed to deal with the more complicated measurements of lines patterned in thicker layers (greater than one-quarter of the illuminating wavelength) including resist, thick metal, and dielectric layers on wafers. For these thick layers, scalar imaging theory cannot be used to predict or analyze the image structure. A waveguide

model has been developed to predict the scattering and resulting image structure for such three-dimensional features patterned in thick layers with the complex edge geometries found on integrated circuit wafers and in developed resist.

IV. Results

The first approach was applied to the measurement of antireflecting-chromium photomasks and has been used routinely for more than five years for calibration of an NBS-developed SRM covering the linewidth range from 0.5 to 10 μm.

For thin layers of oxide and metal on semiconductor wafers (which must be viewed in reflected laser illumination), calibration techniques have been developed, and extensive work has been done on the development of a suitable SRM for which prototypes are currently being fabricated. An interlaboratory study involving the prototype SRM and the accompanying calibration and measurement procedures is planned before this SRM is issued.

Measurement and calibration techniques for lines patterned in thicker layers are also being developed. For this case, a waveguide model has been developed, and it is now possible to predict the scattered field and resulting image structure for any combination of different component materials and arbitrary edge geometry. The task of implementing practical measurement and calibration techniques based on this model has not been completed, and fabrication of suitable SRMs with controlled edge geometry will require better process control than is currently available.

V. List of Publications

The following key publications describe the progress of these two approaches:

1. Nyyssonen, D., Theory of Optical Edge Detection and Imaging of Thick Layers, *J. Opt. Soc.* **72**, 1425 (1982).

2. Kirk, C. P., and Nyyssonen, D., Modeling of the Optical Microscope Images of Thick Layers for the Purpose of Linewidth Measurement, *Proc. Soc. Photo-Optical and Instrumentation Engineers* **538** *Optical Microlithography IV*, 179 (1985).

3. Nyyssonen, D., Design of an Optical Linewidth Standard Reference Material for Wafers, *Proc. Soc. Photo-Optical and Instrumentation Engineers* **342**, *Integrated Circuit Metrology*, 27 (1982).

Numerous other publications relating to the various aspects of linewidth measurement on IC photomasks and wafers are available. Photomask SRMs 474/475 have been available since 1979 and more than 100 have been sold at costs of $4689 (SRM 474) and $3092 (SRM 475). Two other closely related photomask SRMs are nearing completion and are expected to be available in the near future: SRM 476, a bright chromium photomask, and SRM 473,

an antireflecting-chromium reticle SRM with 3X dimensions. For current price listings and availability, consult the NBS Office of Standard Reference Materials, Chemistry Building, Rm. B311, National Bureau of Standards, Gaithersburg, MD 20899.

NBS has conducted and sponsored (in cooperation with SPIE) over a dozen state-of-the-art seminars on linewidth measurement and calibration for the IC industry.

VI. Impact

The NBS photomask SRMs 474 and 475 are the smallest, most accurate dimensional standards in the world today. They provide world-wide traceability to the national standard of length at micrometer dimensions. NBS is seen as the world leader in the development of accurate linewidth measurement and calibration techniques and thousands of copies of its publications in this area have been requested and distributed.

This project has had a long and continuing history of collaboration with major IC producers, equipment manufacturers, standards laboratories, and academia including: research associates (currently with HP and Vickers Instruments), co-op and graduate students (Rochester Institute of Technology, University of Rochester, etc.), collaborations with the IC industry (IBM, Hewlett-Packard, RCA, Honeywell, etc.), collaborations with instrument manufacturers (Vickers Instruments, Nikon, Leitz, etc.), interactions with academia (University of California at Berkeley, University of Arizona, Stanford, etc.), and visits and interactions with visitors to NBS from all these groups. Virtually all major U.S. semiconductor houses use SRM 474 as the basis for linewidth measurement, and the demand for NBS-sponsored seminars on linewidth measurement continues.

CHARACTERIZATION OF SEMICONDUCTORS BY INFRARED SPECTROSCOPY

Aslan Baghdadi

I. Objective

To determine the concentration of impurities in semiconductor substrates.

II. Background

The processing of semiconductor substrates into integrated circuits (ICs) can be described as the introduction of very low levels (in the ppm range) of impurities into a nearly perfect host lattice under carefully controlled conditions. Thus, the presence of even very small concentrations of undesirable impurities in a substrate can have dramatic effects on the performance of IC devices manufactured on that substrate. For example, impurities can result in emitter-to-collector leakage in a bipolar transistor or can reduce the time an NMOS dynamic memory cell can hold a charge. Consequently, careful characterization of the substrate prior to fabrication can significantly increase the yield of the manufacturing process.

Impurities in semiconductors can be classified by their electrical activity: they can be neutral, shallow levels (i.e., acceptors or donors), or they can be deep levels. Shallow levels are ionized at the operating temperature of the device, and thus they determine whether the semiconductor is *n*-type or *p*-type. Deep levels are levels closer to the middle of the band gap of the semiconductor. These levels can either release or trap an electron or a hole and thus act as generation/recombination centers.

Infrared spectroscopy can be used as a tool to detect and quantify of all three kinds of impurities.

III. Approach

A. Neutral Impurities

Neutral impurity atoms which are lighter than the atoms of the host lattice, such as oxygen or carbon in silicon, can be detected by infrared absorption spectroscopy because they have local vibrational modes which absorb infrared radiation with a characteristic wavelength. These measurements can often be carried out at room temperature. Such room temperature measurements are quick, nondestructive, and are easily amenable to automation. They are sufficiently inexpensive so that 100% of the material can be evaluated by this method, if necessary. The primary difficulty in accomplishing this goal lies in adapting the test method to as-received substrates, so that no special preparation of the material is needed to make the measurement. In other words, the measurement method must be adapted to the material, rather than the material to the measurement.

B. Shallow Impurities

These impurities can be detected by infrared absorption spectroscopy because the shallow electronic levels can absorb infrared radiation. These measurements must be carried out at low temperatures, e.g., 10 K. In principle, this would be a nondestructive measurement, since the measurement itself does not alter the sample in any way. However, most low-temperature equipment cannot accommodate samples larger than about a centimeter, so that in many cases the semiconductor wafer (which may be 15 cm or more in diameter) must be cut up in order to fit into the low-temperature cryostat. Moreover, since some time is needed for the sample to equilibrate at these low temperatures, this would not be a very fast measurement. Given these limitations, the measurement of shallow impurities would not be considered nondestructive. These limitations are not fundamental, however, and equipment could possibly be designed to make this a nondestructive technique.

C. Deep Impurities

These impurities may be detected by infrared spectroscopy using their electronic levels or from their local vibrational modes if their atomic masses are lighter than the atomic mass of the host lattice. However, this is not anticipated to become a test method used for the routine evaluation of semiconductor substrates, because most deep-level impurities of interest can be detected better by electrical measurements.

IV. Application: Impurities in Silicon

A. Neutral Impurities

The most important neutral impurities present in semiconductor silicon are oxygen and carbon. Oxygen is present at roughly the 10 to 20 ppma level in all silicon grown by the conventional Czochralski method. Carbon is present at levels ranging from the limit of detectability (about 0.1 ppma) to 2 ppma in both Czochralski and float-zone silicon. Although both these impurities, being neutral, do not directly influence the device performance, they are present in such high concentrations (actually often greater than the concentrations of the intentionally introduced impurities) that they can have serious second-order effects. Either too high or too low an oxygen concentration can result in reduced structural strength in Czochralski silicon. Small oxygen complexes can pin dislocations, thus preventing their propagation. At much higher concentrations, however, large oxide precipitates actually become the source of undesirable dislocations.

Carbon has been shown to be a nucleation center for the formation of either structural defects, such as dislocation loops, or precipitates. Since the carbon distribution in the silicon is generally nonuniform, the presence of carbon can result in a variation in the physical properties of the material across the substrate. This variation in the material properties implies a variation in the diffusion rates of the dopant impurities – thus, it can result in an undesired distribution of the dopant after processing.

B. Shallow Impurities

Shallow impurities such as boron, phosphorus, and arsenic are occasionally present in the silicon feedstock prior to crystal growth. Since all of these impurities have moderate segregation coefficients (0.3 to 0.8), they cannot be eliminated easily during crystal growth. The presence of any of these impurities in material intended to isolate two independent devices could lead to an unwanted channel between these devices.

C. Deep Impurities

Most metallic impurities can produce deep levels in silicon. These impurities have very low segregation coefficients, so that they are removed from the silicon during growth. However, some metallic impurities, such as copper, iron, or gold can be introduced into the silicon during processing. These impurities are fast diffusers in silicon and are not easily removed by surface cleaning. One method has been developed for controlling metallic impurities in silicon by "gettering" the impurities. Oxygen precipitates of controlled size and distribution are formed beneath the surface during high-temperature anneals. The metallic impurities are trapped in the bulk of the silicon by these precipitates, and are thus prevented from affecting the active regions of the devices fabricated on the substrate surface. The oxygen content of these substrates must be known within narrow limits (typically $\pm 10\%$) in order for oxide precipitation to occur with the desired size and distribution. Thus, the oxygen content measurement, discussed in section IV A, is the first step in the control of deep impurities in silicon substrates during processing.

V. Results and Output

A. Measurements on As-Received Substrates

Typical semiconductor substrates are not ideally suited for infrared measurements for two reasons: they are too thin, and they are not polished on both the front and the back surfaces. Methods have been developed for working with thin samples [1-3] and for dealing with the effects of unpolished surfaces [2-5].

B. Automated Data Reduction

An algorithm has been developed, and a computer program written implementing that algorithm, for calculating the oxygen content of as-received silicon wafers [3,6].

C. FT-IR Metrology

The success of these test methods also depends upon the basic accuracy and precision of the infrared measurement. Commercial Fourier transform infrared (FT-IR) spectrometers have only recently become a standard instrument in analytical laboratories. These instruments are vulnerable to a different set of systematic errors than the dispersive infrared spectrometers they are replacing. Thus, the best accuracy possible can only be achieved after examining all possible sources of systematic errors in an FT-IR instrument, and after

understanding how they affect the spectrum after Fourier transformation. We have worked on the effects of different instrument design [7], compositional striations [8,9] instrumental artifacts [1,5,7,10] and errors in the analog-to-digital converter [11,12] of Fourier transform instruments.

VI. Impact

This work, by increasing the accuracy and interlaboratory reproducibility of infrared absorption measurements, will ultimately result in an improved yield for microelectronics fabrication processes. A test method incorporating some of this work has been proposed for consideration by the American Society for Testing and Materials [3].

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2. Baghdadi, A., Multiple Reflection Corrections in Fourier Transform IR Spectroscopy of Back Surface Damaged Wafers, Proc. Symposium on Defects in Silicon, May 1983, San Francisco, CA The Electrochemical Society, p. 293.

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6. Slaughter, S., Gladden, W. K., Duncan, W., and Baghdadi, A., Computer Algorithm and Programs for the Automatic Determination of Interstitial Oxygen in Silicon (manuscript in preparation).

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8. Forman, R. A., Bell, M. I., Baghdadi, A., and Mayo, S., The Effect of Striations on the Compositional Analysis of Silicon Crystals, *Proc. Symposium on Defects in Silicon*, May 1983, San Francisco, CA (The Electrochemical Society), 303.

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55, 547 (1984).

10. Baghdadi, A., Implicit Apodization of Interferograms in Fourier Transform Spectroscopy, *Appl. Spectrosc.* **37**, 520 (1983).

11. Baghdadi, A., and Gladden, W. K., ADC Errors in Quantitative FT-IR Spectroscopy, *Proc. Soc. Photo-Optical and Instrumentation Engineers* **553** *Fourier and Computerized Infrared Spectroscopy*, 207 (1986).

12. Baghdadi, A., Gladden, W. K., and Flach, D. R., Nonlinear Effects of Digitizer Errors in FT-IR Spectroscopy, submitted for publication to *Applied Spectroscopy*.

CHARACTERIZATION OF COMPOUND SEMICONDUCTOR WAFERS BY X-RAY TOPOGRAPHY

Richard A. Forman, Santos Mayo, and Michael I. Bell

I. Objective

To develop rapid, nondestructive methods for imaging the distribution of strain, dislocations, and other defects in semiconductor wafers.

II. Background

The production of III-V compound semiconductor crystals by the liquid-encapsulated Czochralski (LEC) process is of growing commercial importance. Wafers of this material are used as substrates in the fabrication of transistors and integrated circuits which offer significant advantages in speed, power consumption, and radiation hardness over their counterparts made of silicon. A major drawback of this technology is the variability of the starting material and the lack of effective techniques to screen out poor quality wafers before they enter the lengthy and expensive device fabrication process.

At present, the only technique in common use for wafer quality control is etching. This is destructive to the wafer surface and has meant that only small samples of production lots can be tested. Experience indicates, however, that examination of every wafer to be processed would be desirable; defects induced during crystal growth tend to be localized, causing wafer characteristics to vary significantly within a boule as well as from boule to boule. Further, wafer-finishing steps such as lapping and polishing can introduce strain and microcracks which can be expected to vary from wafer to wafer in an unpredictable way.

III. Approach

Strain and defect patterns are easily observed in reflection x-ray topographs of these materials. A rapid, low-cost, nondestructive method has recently been developed for qualitative x-ray reflection topography [1]. Results demonstrate the feasibility of 100% inspection of incoming wafers by fabrication facilities of the size contemplated in plans recently announced by government agencies and industrial firms. The asymmetric double-crystal topography (DCT) system developed achieves high speed and ease of operation at the expense of reduced sensitivity to individual microdefects such as dislocations. This is not a major sacrifice in studying materials such as LEC GaAs which have a very high defect density. Three features of this system contribute significantly to its low cost and high throughput:

1. A commercial silicon wafer is used as a low-magnification monochromator for a conventional laboratory x-ray source. Both the low magnification and the exceptionally good surface finish of the monochromator aid in achieving high intensity in the x-ray beam incident on the specimen.

2. An efficient method for precise specimen alignment was devised [2] which greatly simplifies the process of alignment for both reflection and transmission topographs.

3. Topographs are recorded on high-speed instant film, using x-ray fluorescent screens. In the present application, the loss of resolution is more than compensated by the reduction in measurement time.

IV. Applications

A. Dislocations in LEC GaAs

The new methods have made it possible to obtain both reflection and transmission topographs of LEC GaAs wafers in reasonably short exposure times. The transmission topographs exhibit the characteristic cellular patterns and four-fold symmetric distributions of dislocations. The reflection topographs reveal regions of slip and sub-grain boundaries which result from the same conditions of temperature and stress during crystal growth which produce the dislocation patterns.

B. Growth Striations in LEC GaAs

Growth rate fluctuations can lead to nonuniform incorporation of impurities. If the presence of an impurity produces a sufficiently large change in the lattice constant, variations in its concentration will produce contrast in an x-ray topograph. These inhomogeneities (known as growth striations) are important not only because they lead to point-to-point variations in the electrical and mechanical properties of the material, but also because they can be used to study important aspects of the crystal growth process. The surfaces of constant impurity concentration represent approximate "snapshots" of the instantaneous shape of the liquid-solid interface as the crystal is pulled from the melt, and valuable information about the shape and stability of the interface at various stages of growth can be obtained by examination of the topographs. Recent work on the incorporation of indium into GaAs in order to reduce the generation of dislocations has had the side effect of producing crystals with pronounced striations in the indium concentration, and the opportunity provided by this material is being exploited in order to examine the influence of crystal diameter and growth conditions on the behavior of the interface between the crystal and the melt.

C. Strain and Breakage in GaAs Wafers

GaAs wafers, whether cut from ingots grown by the LEC or horizontal Bridgman (HB) method, often exhibit considerable internal strain and a tendency to fracture "spontaneously." Large, slightly strained regions generally result from the growth process, while small regions of high strain can be produced by lapping, polishing, and handling during wafer fabrication. Double-crystal topographs reveal these strains, as well as occasional buried or incipient cracks which are not visible optically, but which can lead to fracture. Unfortunately, wafers with considerable strain or distortion cannot be imaged completely in a single topograph, especially when relatively high resolution is required as in examining

low-dislocation-density HB substrates for optoelectronic applications. In such cases, it is necessary to generate composite images from a series of topographs. This, together with the demands of 100% incoming inspection, creates a need for continued improvement in techniques and apparatus in order to achieve further reductions in measurement time.

V. Results and Output

The design and operation of the DCT system have been reported in two publications and a talk at a major international conference. The results have attracted the attention of a number of industrial crystal growth and device fabrication groups which now collaborate with NBS in projects designed to correlate the results of x-ray topography with the conditions under which the crystal was grown and with the outcome of attempts to use the material in devices.

VI. Impact

The information which can be obtained from x-ray topographs is of potential value to crystal growers wishing to optimize and control the growth process and to device manufacturers needing to screen out poor quality wafers prior to processing. The basic advances in methods and instrumentation made in this work can be translated into significant reductions in cost in an industrial setting. This will lead to increased use of double-crystal x-ray topography as a tool in process development and control and as a method for incoming inspection.

VII. List of Publications

1. Forman, R. A., and Mayo, S., In Situ Alignment Procedure for X-ray Topography, *J. Appl. Crystallog.* **18**, 106 (1985).

2. Forman, R. A., Bell, M. I., and Mayo, S., Rapid X-Ray Topographic Examination of GaAs Crystals, *Proc. Symp. Defect Recognition and Image Processing in III-V Compounds*, to be published.

CHARACTERIZATION OF SEMICONDUCTORS BY RAMAN AND PHOTOLUMINESCENCE SPECTROSCOPY

Michael I. Bell and Richard A. Forman

I. Objective

To develop and refine laser spectroscopic methods to identify, characterize, and quantify impurities and structural defects in semiconductors.

II. Background

The introduction of small, carefully controlled quantities of electrically active impurities into semiconductor crystals is used to control the electrical properties of the material, permitting the fabrication of electronic devices. Sensitive measurement methods, preferably noninvasive and nondestructive, are required to verify that sufficiently precise control of impurity concentration and distribution has been obtained. The structural perfection of the crystal lattice also influences the device fabrication process.

III. Approach

A. Raman Spectroscopy

Raman scattering can be used to detect and quantify impurities (both electrically active and inactive) and to assess the structural perfection of a crystal. The technique requires essentially no sample preparation, can be used to examine regions as small a few cubic micrometers, and can often be performed at room temperature.

B. Photoluminesence

Laser-excited photoluminescence shares many of the advantages of Raman spectroscopy as a method of nondestructive evaluation. The experimental apparatus and procedures have many similarities, with photoluminescence generally offering greater sensitivity but often requiring cryogenic temperatures.

IV. Application

A. Raman Spectroscopy of Substitutional Impurities

A substitutional impurity with smaller mass than the host ion it replaces can be observed by Raman scattering because it gives rise to a local vibrational mode at a frequency which does not overlap those of the host lattice. Since the local mode frequency depends on the ionic mass, characteristic isotope shifts can be used to confirm the identification of these spectral features [1]. With appropriate care, measurements of local mode intensity can be used to determine the concentration and distribution of impurity ions [2].

In addition, electrically active impurities give rise to electronic Raman scattering in the form of a broad continuum [2] which often interacts with vibrational modes to produce characteristic interference lineshapes. These features can be analyzed to yield estimates of the free carrier concentration. In polar semiconductors such as GaAs, there is an additional interaction between collective electronic excitations (plasmons) and the lattice phonons which give rise to coupled transverse plasmon-phonon modes. Measurement of the frequencies of these modes yields accurate values of the free carrier concentration. This procedure is used routinely in our laboratory to verify the results of Hall effect and resistivity measurements.

B. Raman Spectroscopy of Strain and Lattice Damage

Homogeneous deformation of the crystal lattice (strain) causes frequency shifts and splittings of the vibrational modes, and lattice damage alters the selection rules that govern which vibrations (phonons) give rise to Raman scattering. The calculation of the quantitative effects of stress [3] permits the interpretation of Raman scattering data to yield the magnitude and distribution of strain. The authors have also observed the effects of residual ion implantation damage [2] and of the disorder created by a very high density of impurity ions [1].

C. Photoluminescence of Hot Carriers

Photoexcited carriers with energies greater than the minimum of the band they occupy can recombine before reaching thermal equilibrium. This produces emission (hot photoluminescence) at energies greater than the bandgap. Careful examination and interpretation of the hot photoluminescence of acceptor-doped GaAs have led to more precise knowledge of the structure of the conduction band of this material and to improved understanding of its transport properties [4].

V. Results and Output

The results of this work have been reported in four publications and in talks at major conferences and numerous government, industrial, and university laboratories.

VI. Impact

A. Raman Spectroscopy

The procedures developed for quantitative determination of impurity concentration from local mode intensity [2] have been adopted by many laboratories and used or cited in all subsequent publications of which the authors are aware.

B. Photoluminescence

The improved values for the energy difference between conduction band minima obtained in this study of hot photoluminesence [4] have been used by several groups involved in

the modeling of GaAs transport properties and device behavior. Informal reports indicate that calculations which incorporate these results yield better agreement with experiment than had been obtained previously.

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This is the first in a planned series of annual reports describing the nondestructive evaluation and measurement development activities of the National Bureau of Standards in the area of semiconductor materials and devices. Present activities include production and certification of standard reference materials, development of new measurement techniques, and coordination of interlaboratory experiments and other activities of voluntary standards organizations. Standard reference materials are produced for the determination of the electrical resistivity of semiconductors and for the optical measurement of linewidths on transparent photomasks. New techniques have been developed for optical deep-level spectroscopy, resistivity and recombination lifetime profiling in ingots of very high resistivity silicon, measurement of oxygen in silicon by infrared absorption, characterization of compound semiconductor wafers by optical and x-ray techniques, and extension of photomasks linewidth measurements to thicker lines on silicon substrates. Interlaboratory studies are in progress for electrical deep-level characterization, spreading resistance, and measurement of layer thickness by ellipsometry.

12. KEY WORDS (*Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons*)

deep-level spectroscopy; Fourier-transform infrared spectroscopy; gallium arsenide; linewidth resistivity; nondestructive evaluation; silicon; x-ray topography

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