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TERRY-2: A Test Chip for Characterization of the Performance of Buried-Channel Charge-Coupled Device (CCD) Imagers

G. P. Carver and R. A. Wachnik

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
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Table of Contents

	Page
Abstract	1
Introduction	2
CCD Fabrication Process and Design Rules	3
Test Structure Descriptions	4
Layout	6
Test Structure Measurement Procedures	7
Measurement Program and Test Result Evaluation	18
References	20
Appendix: Charge Pumping	121

List of Tables

1.	Layer and Mask Labels	23
2.	Minimum Geometry Design Rules	24
3.	Cross-Bridge Sheet Resistors	25
4.	Contact Resistors	26
5.	Transistors	27
6.	Large Capacitors and Transistors	29
7.	X- and Y-Coordinates of Cell Origins	30
8.	X- and Y-Coordinates of Bonding Pad Origins	31
9.	Bonding Pad Connections	32
10.	Devices Listed by Cell	34
11.	List of Symbols for Transistor Models	38
A1.	List of Symbols for Charge Pumping	126

List of Figures

		Page
1.	Cross-bridge sheet resistor CB-1	39
2.	Cross-bridge sheet resistor CB-2	40
3.	Cross-bridge sheet resistor CB-3	41
4.	Cross-bridge sheet resistor CB-4	42
5.	Cross-bridge sheet resistor CB-6	43
6.	Cross-bridge sheet resistor CB-7	44
7.	Cross-bridge sheet resistor CB-8	45
8.	Cross-bridge sheet resistor CB-9	46
9.	Cross-bridge sheet resistor CB-10	47
10.	Cross-bridge sheet resistor CB-11	48
11.	Contact resistor CR-1	49
12.	Contact resistor CR-2	50
13.	Contact resistor CR-3	51
14.	Contact resistor CR-4	52
15.	Contact resistor CR-5	53
16.	Contact resistor CR-6	54
17.	Contact resistor CR-7	55
18.	Contact resistor CR-8	56
19.	Contact resistor CR-9	57
20.	MOSFET T-1	58
21.	MOSFET T-2	59
22.	MOSFET T-3	60
23.	MOSFET T-4	61
24.	MOSFET T-5	62
25.	MOSFET T-6	63
26.	MOSFET T-7	64
27.	MOSFET T-8	65
28.	MOSFET T-9	66
29.	MOSFET T-10	67
30.	MOSFET T-11	68
31.	MOSFET T-12	69
32.	MOSFET T-13	70
33.	MOSFET T-14	71
34.	MOSFET T-15	72
35.	MOSFET T-16	73
36.	MOSFET T-17	74
37.	MOSFET T-18	75
38.	MOSFET T-19	76
39.	MOSFET T-20	77
40.	MOSFET T-21	78
41.	MOSFET TN-1	79
42.	MOSFET TN-2	80
43.	MOSFET TN-3	81
44.	MOSFET TN-4	82
45.	MOSFET TN-5	83
46.	MOSFET TN-6	84
47.	MOSFET TN-7	85
48.	MOSFET TN-8	86
49.	MOSFET TN-9	87

List of Figures (cont'd)

		Page
50.	MOSFET TN-10	88
51.	Triple-Gate MOSFET TN-11	89
52.	Triple-Gate MOSFET TN-12	90
53.	Triple-Gate MOSFET TN-13	91
54.	Triple-Gate MOSFET TN-14	92
55.	Triple-Gate MOSFET TN-15	93
56.	Triple-Gate MOSFET TN-16	94
57.	Capacitor/Transistor T-101	95
58.	Capacitor/Transistor T-102	96
59.	Capacitor/Transistor T-103	97
60.	Capacitor/Transistor T-104	98
61.	Capacitor/Transistor T-105	99
62.	Capacitor/Transistor T-106	100
63.	Capacitor C-1	101
64.	Capacitor C-2	102
65.	Capacitor C-3	103
66.	Capacitor C-4	104
67.	Capacitor C-5	105
68.	Gated-diode Electrometer GDA-1	106
69.	Gated-diode Electrometer GDA-2	107
70.	Gated-diode Electrometer GD-1	108
71.	Gated Diode GD-2	109
72.	Gated Diode GD-3	110
73.	Gated Diode GD-4	111
74.	Probe-Fault Error Structure P	112
75.	Ground G	112
76.	Cell probe pad array used for TERRY-2	113
77.	Schematic of TERRY-2 showing the locations of each probe pad cell	114
78.	Schematic of TERRY-2 showing the locations and identifications of bonding pads	115
79.	Schematic of TERRY-2 showing interconnections between test structures, probe pads, and bonding pads	116
80a.	TERRY-2 test chip layout schematic produced by the CAD system used to digitize the chip	117
80b.	Photograph of a TERRY-2 test chip	118
81.	Schematic of a six-terminal metal-to-diffusion contact resistor	119
82.	Schematic cross sections of triple-gate transistors showing the effect of a misalignment ΔX, in the source-to-drain current direction, between the PS1 mask and the DIFF mask	120
A1.	Comparison between trapezoidal pulse and three-level pulse	127
A2.	Capture and emission processes during charge pumping on a p-type substrate	128

PREFACE

This work was conducted as a part of the Semiconductor Technology Program at the National Bureau of Standards (NBS). This program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

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ABSTRACT

Test chip TERRY-2 is intended to be used for characterization of process and performance parameters associated with buried-channel charge-coupled device (CCD) imagers fabricated with a double-polysilicon-gate process which includes several implants. Test structures in TERRY-2 permit evaluation of material properties which are useful for predicting CCD performance and processing quality. TERRY-2 is a modular chip designed for automatic testing; selected devices can be wire bonded for testing various environmental effects; a region containing test structures can be thinned in the same manner as a back-side-illuminated CCD would be; and large devices can be beveled for spreading resistance or physical analysis. This report describes TERRY-2, the test structure designs, and the measurement procedures. The technique of charge pumping for measuring interface state density is discussed in an appendix.

Key Words: CCD; charge-coupled device; charge pumping; contact resistor; microelectronic test chip; sheet resistor; test chip; test pattern; test structure

INTRODUCTION

This report documents the charge-coupled device (CCD) test chip TERRY-2. It contains information for understanding the layout, test structures, and test methods associated with the test chip and for implementing the test chip and test methods.

The CCD test chip TERRY-2 is intended to be used for characterization of the processing steps and the performance of buried-channel CCD imagers fabricated with a double-polysilicon-gate process which includes several implants. With adaptive changes, it could be useful to monitor other fabrication processes.

Some of the special features incorporated in TERRY-2 are as follows:

1. Modularity. All the probe pad arrays are located on a constant grid spacing.

2. Testability. All test structures are accessible electrically for automated testing using the 2 by 10 probe pad array cells.

3. Bondability. Test structures useful for evaluation of environmental effects are accessible both from the probe pad arrays and from bonding pads.

4. Thinnability. Selected test structures for evaluating the effects of thinning are located in a region which can be thinned in the same manner as back-side-illuminated CCD imagers are thinned. After thinning, these test structures remain accessible by probe pads, and in some cases by bonding pads also, located on unthinned regions.

5. Availability for Beveling. Structures large enough to bevel for spreading resistance measurements are located at the top edge of the chip.

The implementation of a test chip measurement program depends on a variety of factors which may change with time as the process evolves and as test results are accumulated and evaluated. In the beginning, it is necessary to identify those parameters associated with the materials and device characteristics which are sensitive to process control, to establish their variability, to characterize excursions from expected results, and to identify sources of process variations.

When a test chip is first introduced into a process, all test devices should be measured. These initial test results can be used to correct or improve the process and also to identify specific tests which provide the information most needed to monitor the process performance, to characterize the materials, and to evaluate critical performance parameters. When the process is determined to be under reasonable control, the initial complete test program may be reduced to a less complete set of test chip measurements which still provides the most useful data.

Test data must be interpreted in association with a mathematical model. When choosing a model for the interpretation of test data, the accuracy with which the model represents the test device becomes an issue. A complex model requiring a large number of measurements may in principle yield very accurate values of material or device parameters. Alternatively, a simple model may describe device behavior over a specified range using less accurate or more general parameters. The simpler model may avoid the need for large amounts of test data and measurement time, while retaining sufficient sensitivity to variations in material parameters. Yet, too simple a model or measurement can provide incorrect results or can fail to detect unacceptable device behavior. A complex model and large amounts of data taking may mean in actuality that no data will be acquired because the investment is too great. There are no simple guidelines to choose the optimal degree of complexity or the optimal amount of data. Practical considerations particular to each case determine both.

Ideally, well-designed test structures provide accurate, sensitive methods of easily measuring selected parameters with simple models and automated instrumentation. In the following sections, models are described which should be sufficiently sensitive and simple to be useful with test chip TERRY-2. In general, the notation in each section is consistent with the primary reference for the section.

CCD FABRICATION PROCESS AND DESIGN RULES

A fabrication process used to fabricate *n*-buried-channel CCD arrays for which test chip TERRY-2 is intended is outlined in table 1. The process includes two levels of polysilicon gates. There are ten mask levels, plus one mask for an optically active back-side-thinned region beneath the CCD.

Table 2 specifies the process geometrical design rules used for the test structures in TERRY-2. There are a few instances where the design rules were violated. These violations were necessary to solve specific geometrical problems which arose in sequences of structures where one dimension differs from structure to structure but all other dimensions are constant. The design rules stated in table 2 were violated in structures CB10, T13, T14, T16, T17, and T19.

TEST STRUCTURE DESCRIPTIONS

The test structures in TERRY-2 include ones for use in measuring process and material properties, active device parameters, and device and material properties related to CCD performance. In addition, several structures are designed to be used in experimental studies on interface states and other measurements and phenomena of probable high value in evaluating the performance of CCD imagers.

Cross-Bridge Sheet Resistors. The cross-bridge sheet resistor is a combined four-terminal van der Pauw sheet resistor and a bridge resistor. The parameters which can be measured are the conducting layer sheet resistance and linewidth. Cross bridges made in source/drain polysilicon 1, polysilicon 2, n^-, n^0, and aluminum are designed at or near the minimum process linewidth. In addition, there are gated structures in n^- and n^0 to evaluate the effects

of fixed oxide charge on the surface of these implants. The gates are also accessible so that effects of fixed oxide charge and possible unwanted depletion can be overcome. Finally, there are cross bridges in field channel stop, column channel stop, and epi. The epi structures are defined by source/drain regions. Cross-bridge sheet resistors are designated CB-1 through CB-11 and are listed in table 3.

Contact Resistors. Six-terminal contact resistors are used to determine the interfacial contact resistance and the front and end contact resistance of ohmic contacts between the aluminum layer and the source/drain polysilicon 1, and polysilicon 2 layers. Each of the three contact types is addressed by three contact resistors having square contact windows with sides of 5 (minimum geometry), 10, and 20 μm. This combination allows evaluation of the area dependence of the contact. Contact resistors are designated CR-1 through CR-9, as described in table 4.

Practical-Style Transistors. The "practical-style" four-terminal MOSFETs include four sets of devices with either polysilicon 1 or polysilicon 2 gates and either with an *n*-type implant (depletion mode) or without an implant (enhancement mode). The widths and lengths in μm (W/L) in each set are 60/10, 120/10, and 60/20. In addition, there are several transistors with various gate layers over field oxide and with field channel stop or column channel stop in the channel.

The enhancement- and depletion-mode sets are used to determine device parameters such as the threshold voltage, source-to-drain leakage current, source-to-drain breakdown voltage, and other transistor operating properties. Availability of three different gate length/width ratios gives the advantage of being able to verify the expected behavior of the devices in relation to their geometical dimensions and to evaluate deviations from the design dimensions. The enhancement-mode devices can also be used for interface state density measurements using charge-pumping techniques.

The nonconventional transistors (field oxide, channel stop-doped channels) can be used to evaluate the unwanted threshold and breakdown voltages present in unavoidable parasitic transistor structures in the circuit.

The design of the input-output circuit transistors incorporates the scheme of extending the gate and gate oxide cut beyond the ends of the source and drain (at the ends of the channel) to overlap the field channel stop. This strategy gives the capability to turn the transistor off even when the surface beneath the oxide surrounding the source and drain, where there is no channel stop, may have become inverted. In the test chip, some practical-style transistors include this design feature and some do not. The reason for not including this inversion protection on all practical-style transistors is that the effective active gate area is better known when the active area is defined by the gate oxide cut. For measurements of the effects of thinning, interface state density, lateral diffusion, etc., a well-known gate area is important.

The practical-style transistors are designated T1 through T21 and are described in table 5.

Wide-Gate Transistors. The four-terminal MOSFETs with wider gates than the practical-style series are all enhancement-mode devices. They provide larger dimensions and a larger range of gate lengths primarily for verification of the smaller practical transistor results and for studies requiring a more accurately known gate area, such as the development of measurement procedures for quantifying the interface state density value obtained from charge pumping. The wide-gate transistor series listed in table 5 includes devices designated TN1 through TN10.

Triple-Gate Transistors. The triple-gate MOSFETs have a center gate formed from one polysilicon layer and two outer gates, between the center gate and the source or drain, formed from the other polysilicon layer. These enhancement-mode transistors are six-terminal devices. They are intended for further verification of charge-pumping results and for studies relating leakage current measurements to charge-pumping measurements. The critical feature is that the center gate can be operated like an MOS capacitor when the outer gates are "OFF" or like a conventional transistor gate when the outer gates are "ON." Therefore, gated-diode-like reverse-bias leakage current measurements, MOS capacitance-voltage measurements, and charge pumping measurements can be performed on the same interface.

The triple-gate transistors are wide-gate structures (and their gates do not overlap the field channel stop) so that their gate area is large enough to be known accurately. They are in a series where the center gate has lengths of 10, 20, and 30 μm. The outer gate lengths are 10 μm. The series is repeated with the polysilicon 1 and polysilicon 2 layers reversed. Triple-gate transistors have designations TN11 through TN16. They are listed in table 5.

Large Area Capacitors/Transistors. There are eight different structures with areas large enough for accurate capacitance-voltage and capacitance-time measurements, for electrical dopant profiling, and for spreading resistance measurements. Two devices are MOS capacitor structures formed of polysilicon 1 or polysilicon 2 and gate oxide over the p-type epilayer. These devices are designated C1 and C2. Two devices are enhancement-mode MOSFETs with n^+ sources and drains, designated T101 and T102. Two pairs of additional devices are depletion-mode transistors with n^- or n^0 implanted layers in their channel region, designated T103 through T106. They are identified in table 6. All eight devices have equal gate active-region areas.

The unique value of these structures is their large area and the associated large gate capacitance. These devices will be necessary for precise diagnostics, although they may not be tested on a regular basis. When measurements on other transistors require comparison with a structure having a much larger gate area, these devices will be valuable for verification purposes. Also, the depletion-mode transistors can be used to perform bulk deep-level transient spectroscopy (DLTS).

Gated Diodes. There are six gated diodes for measuring reverse-bias leakage current and surface recombination velocity. The reverse-bias leakage current value can be used to determine the bulk generation rate and the bulk lifetime; these parameters can be determined as a function of depth. Over the

thinned area, it may be possible to measure the back-side-thinned surface recombination velocity.

Two devices, designated GDA1 and GDA2, are the previously developed gated diode test structures with built-in electrometers for easy automated measurement [Carver and Buehler, 1980; Carver, 1981]. These devices have gates of polysilicon 1 or polysilicon 2. Four other gated diodes, GD1 through GD4, are dual-gate devices and are either surface channel or buried channel. Buried-channel devices have the n^- implant beneath their gates. The dual-gate gated diodes are intended to be used for a variety of measurements, some of which duplicate the measurements that can be performed on single-gate or triple-gate transistors. However, the geometry of the gated diodes is optimized for reverse-bias leakage current measurements and the results are more straightforward to interpret. The disadvantage is that, without the built-in electrometer, gated-diode measurements are more difficult to perform and are not suitable, generally, for automated measurement. Results of comparisons between measurements made on these gated diodes and on the various transistor configurations will indicate the most appropriate strategy for actual use of the devices. It is likely that the gated diodes will provide additional information not available otherwise, and some information more accurately than otherwise available but at a greater expense of time and effort.

Probe-Fault Error Structure. The probe-fault error structure is simply a metal connection between two adjacent probe pads. The absence of an electrical short between the two pads would indicate the likelihood of a probe position error. This device is placed wherever two probe pads occur in a column in a location where they cannot be used for anything else. This structure is labeled P.

Computer-generated drawings of the test structures contained in CCD test chip TERRY-2 are presented in figures 1 through 75. The drawings are all to the approximate scale of one inch equals 50 μm. The smallest interval used is 2.5 μm. This distance corresponds to one-half the grid spacing on the mylar sheets used for the original master drawings. No overlapping lines were allowed except where absolutely necessary to preserve some dimensional requirement in one device of a sequence.

Interconnects between devices and probe or bonding pads are 12.5 μm in width.

LAYOUT

CCD test chip TERRY-2 is a square chip and fits within an area 5200 μm on a side. It has alignment targets designed for use with positive photoresist.

TERRY-2 is modular for convenient access by automated probing systems. All test structures can be probed electrically via uniformly arrayed probe pads. In addition, certain test structures are connected also to bonding pads. These devices can be conveniently wire bonded for measurement when the chip is packaged for environmental testing.

Some devices are located over a region which can be back-side-etched to evaluate effects of thinning processes used for back-side-illuminated CCDs. These structures are connected to probe pads, and in some cases, bonding pads located outside the thinned area.

Large area test structures containing the n^- and n^0 layers are situated near the upper edge of the chip for convenience when beveling to perform spreading resistance profiling measurements.

The selection of test structures for the thinning area and for connection to the wire bonding pads involved an assessment of the process and material parameters which would be important to evaluate the performance of CCDs. The choices were based on some knowledge of the performance of the existing process and anticipated process and materials characterization needs. Just as in the selection of measurements to be made, choices of test structures involve tradeoffs that can be best evaluated only with knowledge of the process status and with a guiding test philosophy. These considerations are discussed in the "Test Structure Measurement Procedures" section.

The TERRY-2 test chip employs modular test structures and a 2 by 10 probe pad array [Buehler, 1979]. Except for the large area capacitor/transistors, all test structures have probe pads contained in their design.

The probe pad array within one cell is shown in figure 76. One probe pad array is a cell of 20 pads, two pads wide and ten pads high. Probe pad spacing is 160-μm center-to-center. This spacing is preserved between cells so that each probe pad is positioned at a distance which is a multiple of 160 μm from any other probe pad in the chip. All probe pads are square, 80 μm on a side.

Table 7 gives the x- and y-coordinates of the origins (lower left corner) of the cells. The lower left corner of the chip boundary is the reference origin (0,0) for the chip. The locations of the cells are shown in figure 77.

The square bonding pads are 120 μm on a side. Locations and designations of the bonding pads are shown in figure 78 and the location of the origins (lower left corner) of all bonding pads is tabulated in table 8. A list of the device connections to each bonding pad is provided in table 9. Figure 79 shows a schematic of the connections between the bonding pads and the probe pads. The overall layout of the test chip is shown in the composite drawing in figure 80a and the photograph of an actual chip in figure 80b.

All test structures are listed by cell in table 10. The numbers at the right are the pad numbers associated with each test structure. Pads within each cell are numbered according to the scheme shown in figure 76; the pads are counted down from number one at the top left and then up to number 20 at the top right.

TEST STRUCTURE MEASUREMENT PROCEDURES

The particular strategy chosen to implement the TERRY-2 test chip as part of a comprehensive testing program depends on a variety of factors associated

with the performance of the fabrication process [Carver, 1980; Buehler, 1983]. Some of these factors and their implications regarding test strategy are discussed in the next section. In this section, emphasis is on the specific measurements which can be performed using the individual test structures in the test chip.

Detailed measurement procedures for certain of the test structures are described in many widely available publications; those procedures are not repeated in this report. However, to provide a useful and reasonably complete report, many of the required measurement procedures and mathematical relationships are briefly described.

Cross-Bridge Sheet Resistors. Cross-bridge sheet resistors are designed to allow measurement of the conducting layer sheet resistance at the cross and the effective average electrical linewidth in the bridge portion of the structure [Buehler *et al.*, 1978 and Buehler and Thurber, 1978]. The measurements are performed by sensing a voltage between two probe pads while a current flows between two separate probe pads. The measurements are potentiometric and avoid interfering current-induced voltage drops in the voltage-sensing connections. The appropriate current levels are chosen to maximize the resolution of the voltage measurement while avoiding thermal effects.

Carrying out the suggested permutations of the sheet resistance measurement allows calculation of an asymmetry factor. When the asymmetry factor is small enough, a high degree of assurance is obtained that the measured sheet resistance value is reliable [Buehler and Thurber, 1978].

Measurement of the sheet resistance and linewidth of the n^+ source/drain layer (cross-bridge CB1), the two polysilicon layers (CB2 and CB3), and the aluminum layer (CB4) is straightforward and is unlikely to be affected by other process or material characteristics. Measurement of the n^- image area implant and the n^0 depletion transistor implant could be affected by charges in the oxide and overglass covering the cross bridges made of these layers (CB5 and CB8). Therefore, additional n^- and n^0 cross-bridge structures are provided which are gated. In principle, the gate voltage is adjusted to obtain the flatband condition at the oxide interface of these structures when the sheet resistance and linewidth measurements are performed. The required gate voltage can be determined from high-frequency capacitance-voltage measurements on the large capacitor/transistors (T103, T104, T105, and T106). Cross-bridge sheet resistors CB6 and CB7 are n^- layer devices with gates formed of polysilicon 1 and polysilicon 2 layers, respectively. Cross-bridge sheet resistor CB9 is an n^0 depletion transistor layer device with a polysilicon 2 gate.

Using a cross-bridge structure, measurement of the sheet resistance and linewidth of the image area column channel stop layer CS2 presents special problems because the substrate is p-type. In this case, the n^+ source/drain layer is used to define the lateral shape of the column channel stop conducting channel (because there is no n-type tub in the CCD fabrication process) to create cross-bridge CB10. However, since there is no isolation beneath the column channel stop layer, an additional cross-bridge structure, CB11, is provided which is identical with CB10 except that the column channel stop

layer is absent. It is likely that the comparison of results from these two structures will provide a measure of the column channel stop sheet resistance. Since the linewidth in these structures is determined by the n^+ layer lateral diffusion, the bridge portion of the devices may be used to provide an additional estimate of the column channel stop sheet resistance. The effective linewidth would be assumed from information about the amount of n^+ layer lateral diffusion

It is possible, using a detailed model of the current distribution in CB11, that the resistivity of the *p*-type epilayer could be estimated using this structure.

Contact Resistors. The "contact resistance" at a test contact is not adequately described by a single resistance value; unless a complete set of parameters associated with a particular contact is known, measurements on that contact cannot be used to predict the behavior of other contacts.

Six-terminal contact resistors can be used to determine electrically four parameters which can be used to describe the contact performance and to predict the behavior of other contacts. These parameters are the interfacial contact resistance, the end contact resistance, the front contact resistance, and the specific contact resistance [Proctor *et al.*, 1983]. The first two parameters are directly measured using the contact resistor test structure; the latter parameters are calculated using expressions based upon a two-dimensional resistor network model.

The interfacial contact resistance R_c, in ohms, is the total resistance of the interfacial layer in a metal-semiconductor contact; it does not include any interconnect resistance. The end contact resistance R_e, in ohms, is the resistance given by the voltage drop across the interfacial layer at the edge of the contact where the current density is least divided by the total current through the contact. The front contact resistance R_f, in ohms, is similarly defined except that the edge of interest is the contact edge where the current density is greatest. These two resistances are different, even in a uniform contact, because at a contact the current tends to flow in the layer with the lower sheet resistance, usually the metal layer. Therefore, if the current flows in a straight path through a contact between a diffusion layer and an aluminum layer, the edge of the contact where the current density is greatest (the "front" edge) is the edge toward the diffusion since near that contact edge much of the current will cross the interfacial layer and flow through the aluminum. The specific contact resistance, in ohm·cm^2, is the resistance of a unit area of the interfacial layer in a metal semiconductor contact. It is the voltage drop across the interfacial layer divided by the current density through the interfacial layer and is constant across a uniform interfacial layer.

A series of devices with different contact window areas can be used to determine the uniformity of the interfacial layer and the uniformity of the interfacial contact resistance, relying on the assumption that the interfacial contact resistance is inversely proportional to the contact window area. This assumption is required for all the parameter determinations using these test structures. If the data indicate that the expected inverse proportionality is not realized, then the specific contact resistance cannot be defined

and the interfacial contact resistance from a particular structure cannot be used to predict reliably the interfacial contact resistance of any other contact [Proctor *et al.*, 1983].

Contact resistors in TERRY-2 address the aluminum to the source-drain layer, the aluminum to the polysilicon 1 level, and the aluminum to the polysilicon 2 level. The devices are replicated with square contact windows of three edge lengths: 5, 10, and 20 μm.

The measurements are made by forcing a current through two probe pads and measuring the voltage between two separate pads on the structure as described in the reference [Proctor *et al.*, 1983]. Similar to cross-bridge sheet resistor measurements, this is a potentiometric measurement. Using the probe pad notations in figure 81, the interfacial contact resistance R_c is determined by measuring the voltage between probe pads 2 and 4, while a known current is flowing between probe pads 1 and 3. A second voltage measurement is made between pads 6 and 4. Then, with the current flowing between pads 5 and 3, the voltage is measured between pads 2 and 4 and between pads 6 and 4. All four voltage measurements are averaged to calculate R_c. The end contact resistance R_e is determined by measuring the voltage between probe pads 4 and 5 with a known current flowing between probe pads 1 and 3. Results with the current flowing in the opposite (negative) direction should also be included to average out thermoelectric voltages.

The set of expressions required for complete analysis of the four parameters is as follows:

$$R_c = \left| \frac{V_{nm}}{I_{nm}} \right| \tag{1}$$

$$R_e = \left| \frac{V_{nm}}{I_{nm}} \right| \tag{2}$$

$$R_e = \frac{(R_s \rho_c)^{1/2}}{w} \operatorname{csch} \left[\left(\frac{R_s}{\rho_c} \right)^{1/2} d \right] \tag{3}$$

$$R_f = R_e \cosh \left[\left(\frac{R_s}{\rho_c} \right)^{1/2} d \right] \tag{4}$$

$$\rho_c = A R_c \, . \tag{5}$$

V_{nm} and I_{nm} are the voltage in volts and current in amps, respectively, measured between pads n and m, R_s is the sheet resistance of the nonmetal layer in ohms (per square), d is the contact window length (i.e., the distance between the front and back edges in cm), w is the contact window width in cm, and A is the contact window area in cm^2. The calculation of R_c, R_e, and ρ_c is straightforward using the first, second, and fifth expressions. Using the determined values of R_e and ρ_c, the third equation is

evaluated to calculate R_s. This value of R_s is then used in the fourth expression to determine R_f.

If a series of contact resistors having different areas is found to have the same value of ρ_c, then the uniformity of the interfacial layer is verified and the above expressions can be used to predict reliably the values of R_c, R_e, and R_f. These values completely characterize the low-frequency behavior of a given contact.

Transistors. As test devices, transistors can be used for a variety of purposes, including device and process parameter extraction and random fault and reliability analysis. The transistors in TERRY-2 are designed primarily for measuring device and process parameters.

Methods used to determine test transistor behavior and models to define transistor parameters are discussed extensively in many common references and are therefore not treated in detail here. Only a brief overview is presented to provide a guide to typical forms of the models and to illustrate the types of parameters that can be determined. In addition, some measurement approaches are suggested. There is, however, no definitive set of transistor parameters which can be prescribed as a critical set. The importance of each parameter depends on too many factors specific to the quality of the process and the demands of the product circuit.

"Normally-off" Enhancement-Mode Transistors. For "normally-off," or enhancement-mode, MOSFETs, an idealized model [Sze, 1981, p. 438] gives the linear region drain current for small V_D as

$$I_D \cong \frac{Z}{L} \mu_s C_{ox} \left(V_G - V_T\right) V_D \; ; \qquad (\underline{\text{linear}}) \qquad (6)$$

and, when the transistor is operated in the saturated region with $V_D \geq (V_G - V_T)$, as

$$I_{Dsat} \cong \frac{Z}{2L} \mu_s C_{ox} \left(V_G - V_T\right)^2 , \qquad (\underline{\text{saturated}}) \qquad (7)$$

where all symbols are defined in table 11. In the linear region, the channel conductance is described by

$$g_D \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G \text{ constant}} = \frac{Z}{L} \mu_s C_{ox} \left(V_G - V_T\right) , \qquad (\underline{\text{linear}}) \qquad (8)$$

and the transconductance is given as

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D \text{ constant}} = \frac{Z}{L} \mu_s C_{ox} V_D . \qquad (\underline{\text{linear}}) \qquad (9)$$

A conduction factor may be defined as

$$K = \frac{1}{2V_D} \frac{\partial I_D}{\partial V_G} \Bigg|_{V_D \text{ constant}} \qquad \text{(linear)} \qquad (10)$$

which, for this model, is then given by

$$K = \frac{Z}{2L} \mu_s C_{ox} . \qquad \text{(linear)} \qquad (11)$$

In the saturated regime, the transconductance is

$$g_{msat} = \frac{Z}{L} \mu_s C_{ox} (V_G - V_T) , \qquad \text{(saturated)} \qquad (12)$$

and the conduction factor becomes

$$K_{sat} = \left[\frac{\partial \sqrt{I_D}}{\partial V_G} \right]^2 \Bigg|_{V_D \text{ constant}} \qquad \text{(saturated)} \qquad (13)$$

or

$$K_{sat} = \frac{Z}{2L} \mu_s C_{ox} . \qquad \text{(saturated)} \qquad (14)$$

In a method described by Buehler [1983], following a procedure proposed by Ham [1980], eight drain current measurements are made to determine seven device parameters which characterize the linear and saturation portions of the MOSFET current-voltage operating characteristics. The determined device parameters are the threshold voltage, conduction factor, and transconductance, each measured in the linear and in the saturated regions, and also the output conductance in the saturation region. The procedure involves two-point estimations of the parameters, based on the partial derivative definitions given above.

There are different ways to define MOSFET operating parameters, and in most cases more detailed information may be obtained at the expense of additional time and effort. On the other hand, less complex measurements may provide misleading or erroneous results.

A good example of the tradeoffs is the threshold voltage measurement. The threshold voltage reflects the various oxide charges and surface doping [Sze, 1981]. The value of the threshold voltage in the linear operating region may be ambiguous since there is no clear turn-on; instead there is initially a gradual exponential increase of drain current with gate voltage due to the diffusion current.

The simplest definition of threshold voltage is the gate voltage required to pass a prescribed drain current for a specified value of drain voltage. Because of the diffusion current, this single operating point definition may give an erroneous result. Also, use of this definition requires additional knowledge to assure the particular transistor is operating properly; for example, it must be known that there is no significant gate-leakage current or that the drain-substrate junction breakdown voltage is not exceeded. A definition based on a two-point procedure involving linear extrapolation to

zero current [Buehler, 1983] requires additional measurement time, but provides greater assurance that the determined value is reliable. Alternatively, ASTM Standard Method F 617-79, "Measuring MOSFET Linear Threshold Voltage," requires measurement of several values of drain current for different gate voltages, at a fixed drain voltage, to determine the maximim slope of the drain current-gate voltage curve. The more complex procedures may be worthwhile because they involve examination of the behavior of the device current-voltage relationship. In a sense, they provide screening or qualification criteria that may save time because there is a higher probability of identifying and eliminating defective devices. Characteristic parameters other than the traditional ones may be defined and measured and sometimes additional useful information may be gained.

According to Takacs [1980], another useful parameter is the peak transconductance, $g_{m,peak}$, which is the maximum slope in the measured I_D versus V_G curve and occurs near V_T. The peak transconductance may be useful since it does not require a measurement of threshold voltage, is not a function of oxide charge variation, and is easy to measure experimentally using a lock-in amplifier. It can be used to monitor gate length using data from a series of transistors of different gate lengths. This may be done by plotting the mask-defined L_{mask} versus $\frac{1}{g_{m,peak}}$ using the equation

$$\frac{1}{g_{m,peak}} = k \left(L_{mask} - \Delta L\right) . \qquad (15)$$

The proportionality constant k is determined by the slope of the line or from a single data point on a transistor where L_{mask} is much larger than ΔL.

Gate dielectric breakdown strengths, source-to-drain breakdown strengths, and source-to-drain leakage currents are also important parameters which may be measured on transistors to characterize the materials and the process. The values of voltage or current used in these tests are chosen to reflect the range of operating points expected for the device.

A sequence of several transistors having different dimensions allows more precise determination of the material parameters and the dimensional parameters than can be obtained using only one device. As an example the surface mobility calculated for one transistor should be that calculated for a second transistor with different dimensions (assuming that short-channel effects are unimportant). Such a comparison verifies that a suitable model is being obeyed. Therefore, data on a series of transistors can be used to plot I_D as a function of Z/L for the same V_G and V_D; the slope of the resulting linear fit can be used to obtain a value for μ_s (eq (6)). C_{ox} is determined from an appropriate MOS capacitor nearby and Z and L are the design dimensions. If the surface mobility varies in a systematic fashion with design gate length, it could be evidence for lateral diffusion of the source/drain dopant. A simpler analysis has been demonstrated to determine systematic deviations in gate length and gate width from design values while accounting for parasitic resistance in series with the channel resistance [Chern et al., 1980].

There are two groups of transistors in TERRY-2. One group contains small, practical-style devices labeled T1 through T21; the other group contains

wider gate devices labeled TN1 through TN10 (and triple-gate devices labeled TN11 through TN16, discussed in a following section).

Among the practical-style transistors, T1 through T6 are enhancement-mode devices having polysilicon 1 or 2 gates. Within each gate type, there is a minimum design-rule gate length device (T1 and T4), a device having twice the gate width (T2 and T5), and a device having twice the gate length (T3 and T6). Among the TN series, TN1 has a polysilicon 1 gate and the minimum gate length; TN2, TN3, and TN4 have successively longer gate lengths. The sequence TN5 through TN8 repeats the series except that the gates are formed of polysilicon 2. Transistors TN9 and TN10 are polysilicon 1-gated and polysilicon 2-gated devices whose channel length is much longer than their width.

Among the practical-style enhancement-mode transistors are some devices that only serve to provide specialized information about the process or materials, rather than information about a realistic device characteristic. Transistors T13 and T14 have a stripe of column channel stop in their channel regions and gates of polysilicon 1 and polysilicon 2, respectively. These transistors are meant to be used to investigate the breakdown properties of the column channel stops used in the CCD array.

Transistors T15 and T16 have field oxide rather than gate oxide under their gates. Both have gates formed of polysilicon 2, but T16 also has a stripe of field channel stop in the conducting channel. Transistor T17 is similar, except that it has gate oxide and a stripe of the field channel stop. Transistor T18 is similar to T15 (field oxide, no channel stop), except that the gate is aluminum. These four devices are intended for use in examining the effectiveness of the field channel stop and the degree of protection against parasitic transistor action. The threshold voltage of these devices may also be monitored before and after environmental exposure.

"Normally-On" Transistors. The properties of "normally-on" or depletion-mode transistors are determined by the properties of the implant which forms the conducting channel and are controlled by the gate-to-channel voltage and the channel-to-substrate voltage. There are three contributions to the drain-to-source current, depending upon the condition of the semiconductor surface: the carrier concentration in the undepleted portion of the channel, the current reduction due to the depletion of carriers in the channel-substrate depletion region, and when the surface is accumulated, the excess accumulated carriers. Several models have been developed to describe these effects [Huang, 1973; Huang and Taylor, 1975; and Edwards and Marr, 1973].

In the model of Huang and Taylor [1975], the drain current of a depletion-mode transistor is related to the gate, drain, and substrate potentials through an average capacitance $\bar{C}$ which relates the gate voltage to the amount of mobile charge in the channel. The model assumes that the conducting channel may be approximated by a step profile. For a conducting channel formed by an n-type implant into a p-type substrate, when the gate voltage is adjusted so that the surface is depleted, the drain current is given by:

$$I_D = \frac{W}{L}\mu_B\{Q_i V_{DS} + \bar{C}[(V_{GS} - V_{FB})V_{DS} - \frac{1}{2}V^2_{DS}] - \frac{2}{3}(2K_s\varepsilon_o qN_{A'})^{1/2}[(V_{BS} + V_{Bi} + V_{DS})^{3/2} - (V_{BS} + V_{Bi})^{3/2}]\} . \quad (16)$$

While the equation for the depletion-mode transistor drain current is more complicated than the enhancement-mode equation, the characteristics are very similar. If the drain-to-source voltage is small, then the device is pinched off uniformly along the channel at some voltage V_T which may be called the threshold voltage. The threshold voltage is given by

$$V_T = V_{FB} - \frac{Q_i}{\bar{C}} + \frac{1}{\bar{C}} \left[2K_s \varepsilon_o q N_A' (V_{Bi} + V_{BS})\right]^{1/2} . \qquad (17)$$

A plot of V_T versus $(V_{BS} + V_{Bi})^{1/2}$ will have an intercept on the V_T axis of $-Q_i/\bar{C} + V_{FB}$. $\bar{C}$ is determined by the slope of the curve near $V_{BS} + V_{Bi} = 0$. The flatband voltage V_{FB} is determined by a 1-MHz C-V curve on the gate-to-buried-channel capacitors (T102 to T106). The total activated implant Q_i may be then determined from the intercept.

This method of measuring the total implant, proposed by Huang and Taylor [1975], underestimates the actual total activated implant by 20 percent according to their data for a 6×10^{11} cm^{-2} implant which is ~0.5 μm deep. It is probably less accurate for deeper implants. Still, this threshold technique might serve as a precise but inaccurate method of process monitoring. Techniques similar to those described for the surface channel enhancement-mode transistors can be applied to the depletion-mode transistors.

The bulk trap concentration and emission kinetics may be measured using a depletion-mode transistor using a technique due to Collet [1975]. The transistor is biased very close to pinch-off so that only a small current flows. The gate bias is pulsed to increase the current; during this time, the conducting portion of the channel increases in thickness. Bulk traps now included in the conducting channel which were above the Fermi level are moved below the Fermi level and the traps are filled. When the gate pulse ends, the conducting channel is again nearly pinched off. As the filled traps in the surface depletion region emit charge, the depletion region thickness is reduced, further increasing the channel thickness. A steady-state current is reached only some time, determined by the emission rate of the traps, after the original gate bias is restored. The current transient may be modeled, as in deep-level transient spectroscopy, to find the bulk trap concentration and the trap emission kinetics. Possibly, the trap concentration can be profiled as a function of depth. This measurement should be sensitive to those traps in the implanted layer which affect the performance of buried-channel CCDs.

Triple-Gate Transistors. The triple-gate transistors are surface channel (enhancement-mode) devices with three separately connected, overlapping gates. Their gate widths are the same as most of the wider gate TN series. Triple-gate transistors are labeled TN11 through TN16. Three transistors have center gates of layer polysilicon 1 (TN13, 14, and 16) and three of layer polysilicon 2 (TN11, 12, and 15). The center gate channel lengths are 10, 20, or 30 μm, and the outer gate channel length is 10 μm.

Triple-gate transistors are intended to be used for a variety of nonroutine, but potentially very valuable, measurements relevant to the characterization of interface and oxide traps. The unique capability provided by triple-gate

transistors is that MOS capacitor and reverse-bias junction leakage measurements can be performed on a single gate, a gate that can also be used to measure transistor properties. With the outer gate biased to the flatband voltage, the center gate is isolated and can be used for MOS capacitor measurements, for example, using transient capacitance or admittance methods to determine the interface state density. With the outer gates biased to strong inversion, the center gate can be used, as in a gated-diode measurement, to measure the surface recombination velocity. Since the surface recombination velocity is the product of the interface state density and capture cross section, a determination of the capture cross section near midgap can be made. This quantity is otherwise very difficult to measure accurately [Nicollian and Brews, 1982, p. 221].

In addition, the interface state density on the center gate can be measured using charge pumping techniques (see Appendix). The measurement of interface state density using charge pumping has not been quantitatively evaluated by comparison with another more completely understood method using the same interface. If these devices can be used to interpret charge pumping results, or even to calibrate the charge pumping current against a more reliable interface state density method, it is possible that the easy-to-perform charge pumping technique could be used reliably on the smaller transistors and could become a new "routine" measurement.

Furthermore, the opportunity is available to compare interface state measurements with transistor transport measurements, and to address such issues as the effect of interface state density on transconductance.

The triple-gate transistors can also be used to measure relative misalignment in the direction of the channel current flow between the polysilicon layers and the source-drain layer. The procedure is similar to the peak transconductance method of Takacs [1980]. In this application, the transconductance is measured separately in each outer gate of a device, while the other outer gate and the center gate are held in strong inversion. The misalignment ΔX between the polysilicon-1 level and the source-drain level is given by [Takacs, 1980]

$$\Delta X = \frac{L' g_m'}{2} \left(\frac{1}{g_m(\text{outer gate left})} - \frac{1}{g_m(\text{outer gate right})} \right) ,$$

where L' and g_m' are the effective channel length and transconductance from a single-gate transistor having the same polysilicon layer gate type as the outer gates on the test device and the same gate width, and g_m (outer gate left) and g_m (outer gate right) are the transconductances of the left and right outer gates, respectively. The single-gate transistor length and transconductance provide an empirical relationship between gate length and transconductance for the polysilicon layer being measured. However, it does not matter which layer is being measured; the result always gives the relative misalignment between the polysilicon-1 layer and the source-drain layer. This is shown in figure 82.

Large Area Capacitor/Transistors. There are a great number of ac measurement techniques involving capacitance and conductance as a function of time, frequency, and dc bias voltage, applicable to MOS structures. (See e.g., the

Simmons and DeClerck articles in Zemel, 1979; Nicollian and Brews, 1982; and Sze, 1981.) These techniques can be used to obtain information on the electrical characteristics of the MOS structure, including the oxide layer, the oxide-silicon interface, and the bulk silicon substrate. Examples of characteristics amenable to measurement include:

for the oxide:	trapped charge density, neutral trap density, dielectric breakdown strength, and thickness;
for the interface:	trap density, trap energy distribution, trap capture/emission rates, and fixed charge density; and
for bulk silicon:	deep-level trap density, trap energy, trap capture/emission rates, shallow-level (dopant) profiles, and minority carrier lifetime.

The most common MOS measurement is probably the high-frequency capacitance versus bias voltage measurement. From this measurement it is possible to obtain or estimate the oxide thickness, threshold voltage, flatband voltage, silicon dopant density, interface state density (for relatively large values of interface states by today's integrated circuit standards), and minority carrier lifetime. Special considerations must be applied to the polysilicon gate capacitors because of depletion effects in the polysilicon [Yaron and Frohman-Bentchkowsky, 1980].

In TERRY-2, there are six MOS structures of interest. They are the two polysilicon layers and their respective gate oxides over the substrate (p-type epilayer), the n^- implant, and the n^0 implant. To address each of these structures and to provide optimal structures for a variety of measurements, eight large capacitor/transistor test structures are available. For each polysilicon-gate oxide pair, there is a capacitor (C1 or C2), enhancement-mode transistor (T101 or T102), and two depletion-mode transistors (T103 or T104 for the n^- implant and T105 or T106 for the n^0 implant). The depletion-mode transistors can be thought of, and treated as, junction-isolated MOS capacitors where the "substrate" is the implant layer; the source-and-drain connections provide contacts to the "substrate." The arrangement of two separate substrate contacts on opposite sides of the gate conveniently forms a transistor and allows the performance of additional types of measurements, such as pinch-off voltage and deep-level transient spectroscopy (DLTS) using a deep depletion MOS transistor [Collet, 1975]. The depletion-mode transistor measurements on these large devices can be compared with results obtained on the smaller, practical-size transistors. Similarly, the large enhancement-mode transistors (T101 and T102) can be used to provide data for comparison with the smaller transistors.

The large depletion-mode transistors provide a convenient junction (either n^--substrate or n^0-substrate) for dopant profiling through the epilayer to the substrate using high-frequency capacitance-voltage techniques. The large enhancement-mode devices (T101 and T102) can be used to profile using the dc MOSFET dopant profiling technique [Buehler, 1980, and Carver, 1983].

The large depletion-mode transistors are also intended for use as spreading resistance samples for profiling the implanted layers. They are located at the top edge of the chip for ease in beveling. These devices are large enough to allow several measurements to be made on each device for assessing

the reproducibility of the measurement. Also, the devices are large enough to permit a suitably shallow bevel angle for high resolution in the profile depth scale.

In addition, the large capacitors and transistors can be used to perform deep-level transient spectroscopy (DLTS) measurements for bulk and surface trap parameters [Tredwell and Viswanathan, 1980].

Gated Diodes and Gated-Diode Electrometers. The gate-controlled diode structure is a useful device for studying the effects of the interface, and space-charge regions at the interface, on the behavior of *p-n* junctions [Grove, 1967]. These effects primarily involve generation/recombination processes and they cause excess reverse-bias leakage current in the diode and a reduction in the junction reverse-bias breakdown voltage. In CCDs, these effects lead to higher levels of dark current. (Even in buried-channel CCDs, higher dark current levels are experienced due to intersection of depletion regions at the periphery of the gates with the interface.) Also, bulk leakage sources can be monitored, including depth profiling of bulk leakage sources. (Leakage sources in the bulk are deep-level traps where generation and recombination can take place.)

The gated-diode electrometer is a test structure that combines a MOSFET electrometer amplifier with a gated diode [Carver and Buehler, 1980]. Instead of measuring the small leakage currents, typically picoamperes, directly in series with the high impedance of the reverse-biased junction, a voltage transient at the output of a source-follower amplifier is measured. The junction is initially reverse-biased and disconnected from the voltage source. The leakage currents discharge the depletion capacitance and the voltage across the junction is dissipated. The voltage decrease is monitored by the electrometer amplifier. With this arrangement, leakage current measurements are more accessible to automated measurement systems.

Grounds and Probe Placement Detectors. In various places, as space dictated, pairs of probe pads are connected together. Some of these pairs are grounded (device G) and some are ungrounded (P). These devices can provide assurance of proper placement of probes and continuity between probe pads.

Devices GG are grounded bonding pads.

MEASUREMENT PROGRAM AND TEST RESULT EVALUATION

The implementation of a test chip measurement program depends on a variety of factors which may change with time as the process evolves and as test results are accumulated and evaluated. Initially, it is necessary to [Linholm, 1981, p. 11]:

1. Identify and measure process parameters, both fundamental materials parameters and device characteristics, which can be used to characterize the degree of process control to and accurately predict process performance; and
2. Establish the ranges and uniformities of these materials parameters and device characteristics and determine the correlations between

their variations over a wafer, from wafer-to-wafer within a lot, and from lot-to-lot.

Only after the completion of these two steps can a minimum set of measurements be established and procedures set up to monitor excursions from expected results and to collect data to identify the source of unexpected process performance variations. It is important that these principles are understood by those implementing a test chip metrological program.

The first version of a test chip should contain test structures suitable for measuring accessible and appropriate material properties, even though their ranges and acceptable variations may not be known beforehand. Therefore, the initial design of a test chip should contain a broad spectrum of test structures and representative devices to characterize the process and the intended product performance. In order to characterize a new process, or one previously untried for a given product or performance level, new unproven test structure designs and test methods may have to be used in addition to the set of fully characterized devices and test methods already known to be dependable and proven in use. Every process is different; the critical, yield- or performance-limiting parameters are different. These critical parameters will likely change with time as process control improves and the process evolves to maturity. In addition, certain critical parameters relating to product performance may require more sophisticated (non-automated) test methods.

Buehler [1983] identifies six use categories of test structures. TERRY-2 was designed to address only two of these areas judged to be key ones for CCD performance and process control: device parameters and process parameters, including processed materials properties. In the case of TERRY-2, prior knowledge of the maturity of the process and of the CCD performance, both before and after environmental exposure, facilitated some decisions related to the design and selection of test structures. A broad variety of process and device parameters are addressed and there are many devices aimed at characterizing interface and bulk trap distributions spatially and energetically. Most of these latter devices are capacitor/transistors, gated diodes, and multigate transistors. Some test methods suggested for measuring interface and bulk traps are promising, but they may not be practical in a production environment and they are unproven and untried on the CCD process. Most of these methods are mentioned in the previous section; some of them are likely to provide important and critical information not available from any other source.

When TERRY-2 is included in the CCD process (as a drop-in), all test devices should be measured. The initial test results must be obtained and interpreted quickly so they can be used to correct or improve the process [Linholm, 1981] and to:

1. Provide averages and standard deviations of all process parameters to determine statistically significant variations.
2. Provide average and standard deviations of parameters across a wafer, between wafers in a given lot, and between lots.

3. Determine which of the promising, but not yet evaluated on this CCD process, devices and techniques can be used to provide information on critical parameters, including environmental effects.
4. Develop a realistic test program which will provide information useful to monitor the process performance, to characterize the materials, and to evaluate critical parameters related to the desired performance of the CCD.

When the process is determined to be under acceptable control, the initial test program may be reduced to a less complete set of test chip measurements. In this sense, a test chip and the associated test methodology are like an insurance program. The criteria which determine which properties should be routinely measured and how often they should be measured include whether the parameters lie within target design windows, the size of the parameter variations, and the amount of effort required to obtain the information. Only the data can provide the input needed by process engineers to make meaningful judgments and decisions.

The key attribute of a successful test program is the efficient handling and evaluation of test data so that important conclusions about the acceptability of the results can be reached quickly.

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Table 1. Layer and Mask Labels.

Process Layer or Feature	Note	Defining Mask	Conductivity Type
Field channel stop	(a)	CS1	*p*
Source/drain	(b)	DIFF	*n*
Gate oxide	(c)	TO	-
n^- implant	(d)	NW	*n*
n^0 implant	(d)	NW2	*n*
Image area column channel stop	(e)	CS2	*p*
Polysilicon 1	(f)	PS1	*n*
Polysilicon 2	(f)	PS2	*n*
Contact window	(g)	CT	-
Aluminum	(h)	AL	-
Passivation	(i)	PAD	-

(a) Allows the inactive field region to be doped to increase the field threshold.

(b) Allows the diffusing or implanting of sources or drains of transistors, CCD input and output diodes, and undercrossings.

(c) Removes all oxide over CCD gate area, transistor gate area, etc.

(d) NW and NW2 are two masks for doping the silicon surface for (1) the CCD buried channel and (2) optional depletion-mode transistors in the input and output circuitry.

(e) Defines the well areas in the CCD.

(f) PS1 and PS2 define the gates of the CCD or transistors and other structures.

(g-i) These mask levels have the usual functions in an MOS process.

Table 2. Minimum Geometry Design Rules.*

Level/Mask Layer	Rule Definition	Minimum Nominal Distance (μm)
Source/Drain (DIFF)	width	7.5
	source-to-drain spacing	10.0
	spacing-to-channel stop	12.5
	overlap of thin oxide cut	2.5
	overlap of contact window	5.0
Field Channel Stop (CS1)	width	5.0
Column Channel Stop (CS2)	width	2.5
Thin Oxide (TO)	width	5.0
	overlap of contact window	2.5
n^- Implant (NW)	width	5.0
	overlap of thin oxide	2.5
First Polysilicon (PS1)/ Second Polysilicon (PS2)	width	7.5
	same-level polysilicon-to-polysilicon spacing	2.5
	overlap of channel stop	2.5
	overlap of contact window	2.5
	overlap of source/drain	2.5
	overlap between polysilicon levels	2.5
Contact Window (CT)	width	5.0
Aluminum (AL)	width	10.0
	aluminum-to-aluminum spacing	12.5
	overlap of contact window	5.0

* Note that these design rules apply specifically to test chip TERRY-2. They are related to the design rules for the CCD but do not correspond to them.

Table 3. Cross-Bridge Sheet Resistors.

Parameters determined: Sheet resistance and linewidth of various conducting layers.

Device Designation	Cell*	Conducting Layer	Specifications and Notes (dimensions in μm)
CB1	1	n^+ source/drain	nominal linewidth: 10.0
CB2	7	polysilicon 1	nominal linewidth: 10.0, polysilicon 1 over gate oxide
CB3	2	polysilicon 2	nominal linewidth: 10.0, polysilicon 2 over gate oxide
CB4	3	aluminum	nominal linewidth: 10.0
CB5	4	n^- implant	nominal linewidth: 10.0
CB6	8	n^- implant	same as CB5, except gated using polysilicon 1
CB7	9	n^- implant	same as CB5, except gated using polysilicon 2
CB8	10	n^0 implant	nominal linewidth: 10.0
CB9	11	n^0 implant	same as CB8, except with polysilicon-2 gate
CB10	18	column channel stop	linewidth determined by n^+ boundaries, nominally 10.0
CB11	23	p^- epilayer	same as CB10, except no column channel stop implant

*Cell designations are identified in the section entitled "Layout."

Table 4. Contact Resistors.

Parameters determined: Interfacial contact resistance, end contact resistance, front contact resistance, and specific contact resistance.

Device Designation	Cell	Conducting Layers	Contact Window Edge Length (μm)
CR1	13	Metal-source/drain	5.0
CR2	16	Metal-source/drain	10.0
CR3	11	Metal-source/drain	20.0
CR4	2	Metal-polysilicon 1	5.0
CR5	3	Metal-polysilicon 1	10.0
CR6	4	Metal-polysilicon 1	20.0
CR7	8	Metal-polysilicon 2	5.0
CR8	9	Metal-polysilicon 2	10.0
CR9	10	Metal-polysilicon 2	20.0

Table 5. Transistors.*

Parameters determined: Threshold voltage (enhancement devices), pinch-off voltage (depletion devices), interface state density (enhancement devices), and transistor properties.

Practical-Style Transistors

Device Designation	Cell	Enhancement (E) or Depletion (D)	Channel Layer	Gate Layer	Oxide Type	W/L (μm)
T1	5,23	E	epi(p)	PS1	gate	60/10
T2	1	E	epi(p)	PS1	gate	120/10
T3	2	E	epi(p)	PS1	gate	60/20
T4	6,23	E	epi(p)	PS2	gate	60/10
T5	3	E	epi(p)	PS2	gate	120/10
T6	4	E	epi(p)	PS2	gate	60/20
T7	7,17	D	n^-	PS1	gate	60/10
T8	15	D	n^-	PS1	gate	120/10
T9	16	D	n^-	PS1	gate	60/20
T10	6,17	D	n^-	PS2	gate	60/10
T11	8	D	n^-	PS2	gate	120/10
T12	9	D	n^-	PS2	gate	60/20
T13	21	E	CS2	PS1	gate	60/15
T14	10	E	CS2	PS2	gate	60/15
T15	22	E	epi(p)	PS2	field	60/10
T16	22	E	CS1	PS2	field	60/15
T17	16	E	CS1	PS2	gate	60/15
T18	11	E	CS1	AL	field	60/15
T19	11,14	D	n^0	PS2	gate	60/10
T20	2,15	D	n^0	PS2	gate	120/10
T21	3	D	n^0	PS2	gate	60/20

Wide-Gate Transistors

TN1	19	E	epi(p)	PS1	gate	230/10
TN2	1,20	E	epi(p)	PS1	gate	230/15
TN3	12	E	epi(p)	PS1	gate	230/20
TN4	13	E	epi(p)	PS1	gate	230/30
TN5	4	E	epi(p)	PS2	gate	230/10
TN6	5	E	epi(p)	PS2	gate	230/15
TN7	6	E	epi(p)	PS2	gate	230/20
TN8	7	E	epi(p)	PS2	gate	230/30
TN9	13	E	epi(p)	PS1	gate	55/160
TN10	14	E	epi(p)	PS2	gate	55/160

Table 5. Transistors (cont'd).

Triple-Gate Transistors**

Device Designation	Cell	Center Gate Layer	Center Gate Length (μm)	Outer Gate Layer	Outer Gate Length (μm)
TN11	1,6,22	PS2	10	PS1	10
TN12	13	PS2	20	PS1	10
TN13	16,19	PS1	10	PS2	10
TN14	19	PS1	20	PS2	10
TN15	5	PS2	30	PS1	10
TN16	7	PS1	30	PS2	10

*Among the practical-style transistors, all are of the radiation-hard extended-gate design except T1 in cell 5, T4 in cell 6, T7 in cell 7, T10 in cell 6, T19 in cell 14, and T20 in cell 15. Of the wide-gate transistors, only TN2 in cell 1 is the radiation-hard design. Only TN11 in cell 22 and TN13 in cell 19 are the radiation-hard design among the triple-gate transistors. T15 and T16 in cell 22 and T18 in cell 11 are not radiation-hard because they have field oxide under the gate. The *p*-type regions in the channels of T13, T14, and T16-T18 are confined to 5-μm wide stripes in the center of the channel.

**All triple-gate transistors are enhancement-mode, in the *p*-type epilayer. Gate widths are 230 μm.

Table 6. Large Capacitors and Transistors.*

Parameters determined: Dopant profile (spreading resistance, capacitance-voltage where possible), capacitance-voltage properties, transistor properties (including threshold and pinchoff voltages, where applicable), interface properties, bulk traps in n^- buried layer (where applicable). Comparisons can be made between thick and thin regions (except for T105 and T106).

Device Designation	Cell	Channel	Gate	Notes
C1	20	epi(p)	polysilicon 1	surface capacitor
C2	21	epi(p)	polysilicon 2	surface capacitor
T101	20	epi(p)	polysilicon 1	enhancement-mode transistor
T102	21	epi(p)	polysilicon 2	enhancement-mode transistor
T103	14,19	n^-	polysilicon 1	depletion-mode transistor
T104	15,22	n^-	polysilicon 2	depletion-mode transistor
T105	20	n^0	polysilicon 1	depletion-mode transistor
T106	21	n^0	polysilicon 2	depletion-mode transistor

*All large transistors have a channel length of 255 μm and a channel width of 425 μm. The active area of the large capacitors is also 255 μm by 425 μm.

Table 7. X- and Y-Coordinates of Cell Origins.

The coordinates of the cell origins are given relative to the chip origin. The chip origin is at the lower left corner of the chip. All cell origins are at the lower left corner of the cell when the cell is "upright." A cell is upright when the origins of each of the test structures within the cell are at the left margin of the cell. The master drawings of the test structures were oriented so that when the test structure designs were digitized and the cells were created by stacking the test structures, the cells would automatically be stored digitally in an upright orientation.

Certain test structures that lie outside the cells are not in an upright position on the chip.

cell number	coordinates (x,y) in μm
1	(200, 0)
2	(520, 0)
3	(840, 0)
4	(1160, 0)
5	(1800, 0)
6	(2440, 0)
7	(3080, 0)
8	(3720, 0)
9	(4040, 0)
10	(4360, 0)
11	(4680, 0)
12	(200, 1600)
13	(520, 1600)
14	(840, 1600)
15	(4040, 1600)
16	(4360, 1600)
17	(4680, 1600)
18	(200, 3200)
19	(520, 3200)
20	(840, 3200)
21	(4040, 3200)
22	(4360, 3200)
23	(4680, 3200)

Table 8. X- and Y-Coordinates of Bonding Pad Origins.

Pad Designation	Coordinates (x,y) in μm	Pad Designation	Coordinates (x,y) in μm
1L	(40, 4600)	1R	(5040, 4600)
2L	(40, 4360)	2R	(5040, 4360)
3L	(40, 4120)	3R	(5040, 4120)
4L	(40, 3880)	4R	(5040, 3880)
5L	(40, 3640)	5R	(5040, 3640)
6L	(40, 3400)	6R	(5040, 3400)
7L	(40, 3160)	7R	(5040, 3160)
8L	(40, 2920)	8R	(5040, 2920)
9L	(40, 2680)	9R	(5040, 2680)
10L	(40, 2440)	10R	(5040, 2440)
11L	(40, 2200)	11R	(5040, 2200)
12L	(40, 1960)	12R	(5040, 1960)
13L	(40, 1720)	13R	(5040, 1720)
14L	(40, 1480)	14R	(5040, 1480)
15L	(40, 1240)	15R	(5040, 1240)
16L	(40, 1000)	16R	(5040, 1000)
17L	(40, 760)	17R	(5040, 760)
18L	(40, 520)	18R	(5040, 520)
19L	(40, 280)	19R	(5040, 280)
20L	(40, 40)	20R	(5040, 40)
21L	(1200, 3920)	21R	(3880, 3920)
22L	(1200, 3680)	22R	(3880, 3680)
23L	(1200, 3440)	23R	(3880, 3440)
24L	(1200, 3200)	24R	(3880, 3200)
25L	(1200, 2960)	25R	(3880, 2960)
26L	(1200, 2720)	26R	(3880, 2720)
27L	(1200, 2480)	27R	(3880, 2480)
28L	(1200, 2240)	28R	(3880, 2240)
29L	(1200, 2000)	29R	(3880, 2000)
30L	(1200, 1760)	30R	(3880, 1760)
31L	(1400, 1680)	31R	(3680, 1680)
32L	(1520, 1880)	32R	(3560, 1880)
33L	(600, 5040)	33R	(4480, 5040)
34L	(560, 4800)	34R	(4520, 4800)
35L	(1200, 4640)	35R	(3880, 4640)
36L	(1440, 4640)	36R	(3640, 4640)
37L	(1680, 4640)	37R	(3400, 4640)
38L	(1880, 4800)	38R	(3200, 4800)
39L	(1880, 5040)	39R	(3200, 5040)
40L	(2440, 5000)	40R	(2640, 5000)
41L	(2480, 4800)	41R	(2560, 4600)
42L	(2160, 4480)	42R	(2800, 4480)
43L	(1560, 1440)	43R	(3520, 1440)

Table 9. Bonding Pad Connections.

Pad Designation	Device Designation	Function
1L	T103	source-drain
2L	G	ground
3L	GD1	outer gate
4L	GD1	inner gate
5L	GD2	outer gate
6L	GD2	inner gate
7L	G	ground
8L	GD3	outer gate
9L	GD3	inner gate
10L	GD4	outer gate
11L	GD4	inner gate
12L	G	ground
13L	TN11	source-drain
14L	TN11	center gate
15L	TN11	source-drain
16L	TN11	left outer gate
17L	TN11	right outer gate
18L	TN2	gate
19L	TN2	source-drain
20L	TN2	source-drain
21L	C1	gate
22L	T101	source-drain
23L	T101	gate
24L	T101	source-drain
25L	T103	gate
26L	T103	source-drain
27L	T103	source-drain
28L	GDA1	reset
29L	GDA1	reverse bias voltage
30L	GDA1	amplifier supply voltage
31L	GDA1	output
32L	GDA1	inner gate
33L	T103	source-drain
34L	T103	gate
35L	C1	gate
36L	T105	source-drain
37L	T105	gate
38L	T105	source-drain
39L	T101	source-drain
40L	T101	gate
41L	T101	source-drain
42L	GG	ground
43L	GDA1	outer gate
43	GD1	junction
44	GD2	junction
45	GD3	junction
46	GD4	junction

Table 9. Bonding Pad Connections (cont'd).

Pad Designation	Device Designation	Function
1R	T104	source-drain
2R	T1	gate
3R	T1	source-drain
4R	T1	source-drain
5R	T4	gate
6R	T4	source-drain
7R	T4	source-drain
8R	G	ground
9R	T7	gate
10R	T7	source-drain
11R	T7	source-drain
12R	T10	gate
13R	T10	source-drain
14R	T10	source-drain
15R	T19	gate
16R	T19	source-drain
17R	T19	source-drain
18R	T18	gate
19R	T18	source-drain
20R	T18	source-drain
21R	C2	gate
22R	T102	source-drain
23R	T102	gate
24R	T102	source-drain
25R	T104	gate
26R	T104	source-drain
27R	T104	source-drain
28R	GDA2	outer gate
29R	GDA2	inner gate
30R	GDA2	output
31R	GDA2	amplifier supply voltage
32R	GDA2	reverse bias voltage
33R	T104	source-drain
34R	T104	gate
35R	C2	gate
36R	T106	source-drain
37R	T106	gate
38R	T106	source-drain
39R	T102	source-drain
40R	T102	source-drain
41R	T102	gate
42R	GG	ground
43R	GDA2	reset

Table 10. Devices Listed by Cell.

Cell 1	
TN11	1,2,3,18,19,20
T2	4,5,16,17
CB1	6,7,8,13,14,15
TN2	9,10,11,12

Cell 2	
CR4	1,2,3,18,19,20
T3	4,5,16,17
CB3	6,7,8,13,14,15
T20	9,10,11,12

Cell 3	
CR5	1,2,3,18,19,20
T5	4,5,16,17
CB4	6,7,8,13,14,15
T21	9,10,11,12

Cell 4	
CR6	1,2,3,18,19,20
T6	4,5,16,17
CB5	6,7,8,13,14,15
TN5	9,10,11,12

Cell 5	
GD1	1,2,3,18,19,20
T1	4,5,16,17
TN15	6,7,8,13,14,15
TN6	9,10,11,12

Cell 6	
TN11	1,2,3,18,19,20
T4	4,5,16,17
T10	6,7,14,15
G	8,13
TN7	9,10,11,12

Table 10. Devices Listed by Cell (cont'd).

Cell 7

CB2	1,2,3,18,19,20
T7	4,5,16,17
TN16	6,7,8,13,14,15
TN8	9,10,11,12

Cell 8

CR7	1,2,3,18,19,20
T11	4,5,16,17
CB6	6,7,8,9,12,13,14,15
P	10,11

Cell 9

CR8	1,2,3,18,19,20
T12	4,5,16,17
CB7	6,7,8,9,12,13,14,15
P	10,11

Cell 10

CR9	1,2,3,18,19,20
T14	4,5,16,17
CB9	6,7,8,9,12,13,14,15
P	10,11

Cell 11

CR3	1,2,3,18,19,20
T19	4,5,16,17
CB8	6,7,8,13,14,15
T18	9,10,11,12

Cell 12

G	1,20
GD3	2,3,4,17,18,19
GD4	5,6,7,14,15,16
P	8,13
TN3	9,10,11,12

Table 10. Devices Listed by Cell (cont'd).

Cell 13	
CR1	1,2,3,18,19,20
TN9	4,5,16,17
TN12	6,7,8,13,14,15
TN4	9,10,11,12
Cell 14	
G	1,20
T103	2,3,18,19
TN10	4,5,16,17
T19	6,7,14,15
GDA1	8,9,10,11,12,13
Cell 15	
G	1,20
T104	2,3,18,19
T8	4,5,16,17
T20	6,7,14,15
GDA2	8,9,10,11,12,13
Cell 16	
CR2	1,2,3,18,19,20
T9	4,5,16,17
TN13	6,7,8,13,14,15
T17	9,10,11,12
Cell 17	
C3	1,2,3,18,19,20
T7	4,5,16,17
C4	6,7,8,13,14,15
T10	9,10,11,12
Cell 18	
CB10	1,2,3,18,19,20
GD1	4,5,6,15,16,17
GD2	7,8,9,12,13,14
P	10,11

Table 10. Devices Listed by Cell (cont'd).

Cell 19

T103	1,2,19,20
TN13	3,4,5,16,17,18
TN14	6,7,8,13,14,15
TN1	9,10,11,12

Cell 20

C1	1,20
T105	2,3,18,19
T101	4,5,16,17
C1	6,15
T101	7,8,13,14
TN2	9,10,11,12

Cell 21

C2	1,20
T106	2,3,18,19
T102	4,5,16,17
C2	6,15
T102	7,8,13,14
T13	9,10,11,12

Cell 22

T104	1,2,19,20
P	3,18
T15	4,5,16,17
TN11	6,7,8,13,14,15
T16	9,10,11,12

Cell 23

CB11	1,2,3,18,19,20
T1	4,5,16,17
C5	6,7,8,13,14,15
T4	9,10,11,12

Table 11. List of Symbols for Transistor Models.

a. Enhancement-Mode MOSFETs

C_{ox}	oxide capacitance
ΔL	gate-drain overlap
I_D	drain current
L	channel length
μ_s	surface mobility
V_D	drain voltage
V_G	gate voltage
V_S	source voltage
V_T	threshold voltage
Z	gate width

b. Depletion-Mode MOSFETs

C_{ox}	gate oxide capacitance
$\bar{C}_s$	average seimiconductor capacitance
$\bar{C}$	$C_{ox}\,\bar{C}_s/(C_{ox} + \bar{C}_s)$, average capacitance
d	channel junction depth
ε_s	silicon dielectric constant
ε_o	vacuum dielectric constant
K_S	relative dielectric constant of silicon
L	channel length
μ_o	bulk mobility
$N_{A'} = \frac{N_A N_D}{N_A + N_D}$	, composite doping concentration
N_A	substrate doping concentration
N_D	average implant doping concentration
q	electron charge
Q_i	total active implant
t_{ox}	oxide thickness
V_{Bi}	built-in junction voltage
V_{BS}	source-body voltage
V_{DS}	drain-source voltage
V_{FB}	flatband voltage
V_T	threshold voltage
W	gate width

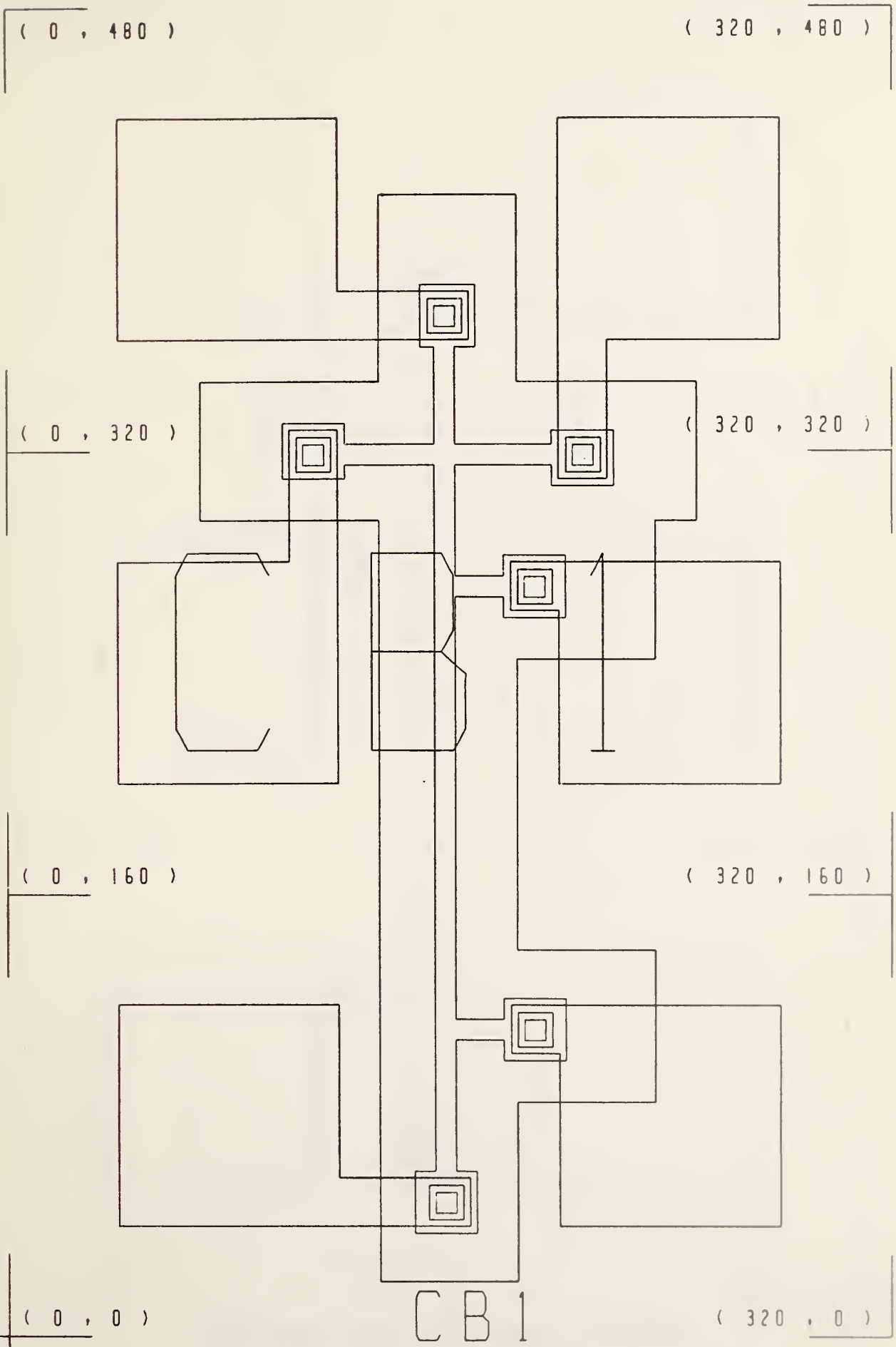


Figure 1. Cross-bridge sheet resistor CB-1.

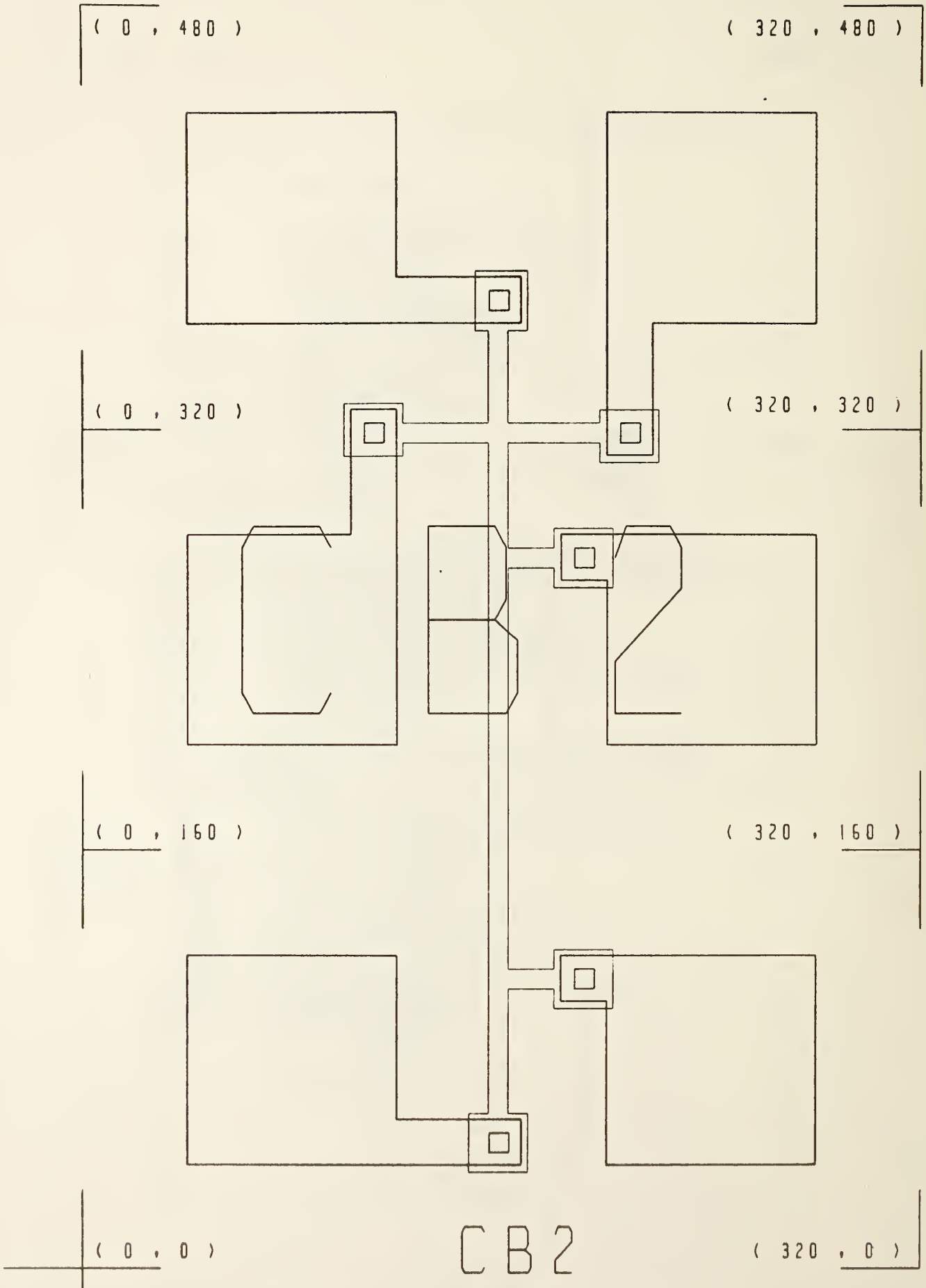


Figure 2. Cross-bridge sheet resistor CB-2.

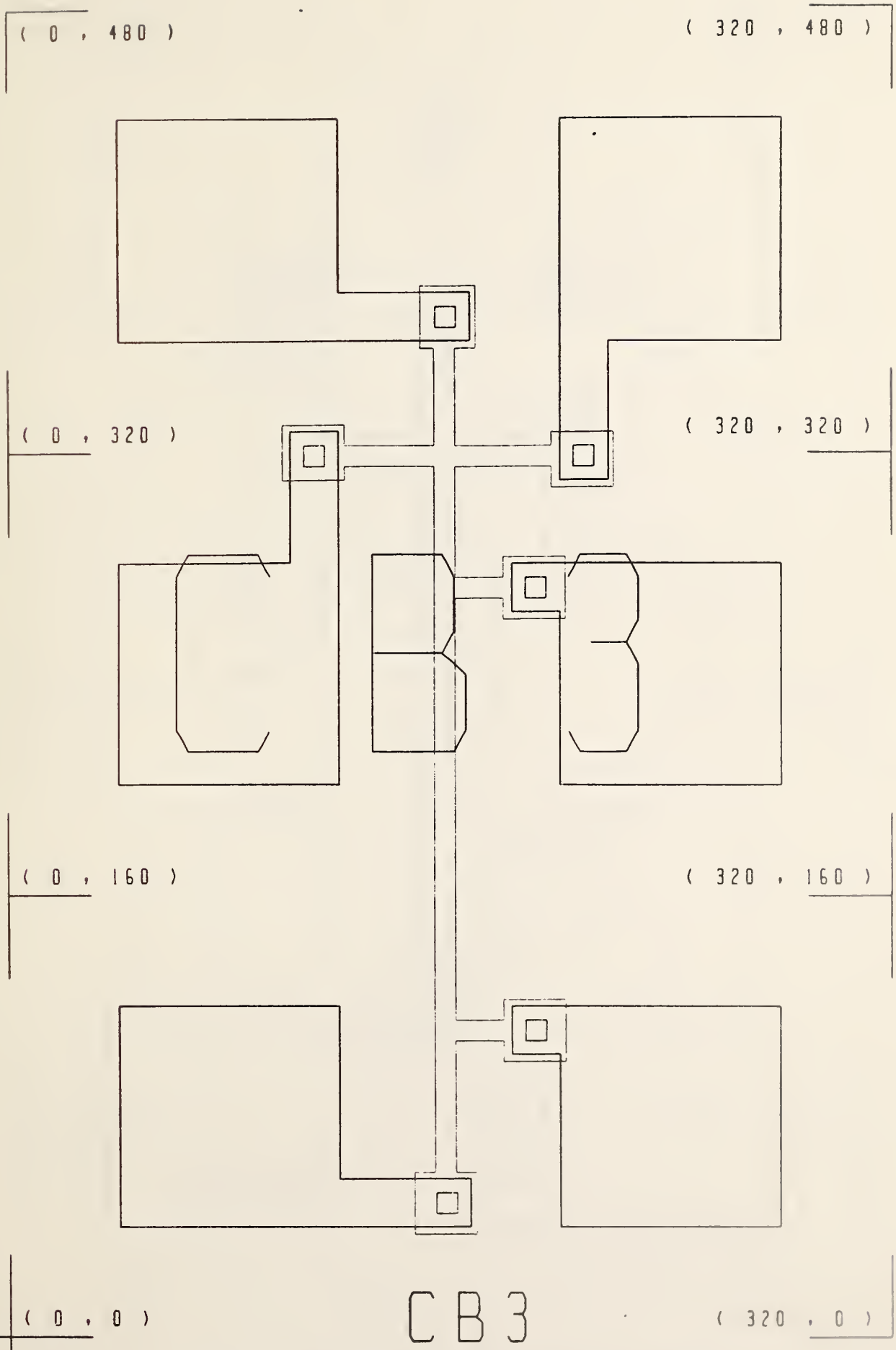


Figure 3. Cross-bridge sheet resistor CB-3.

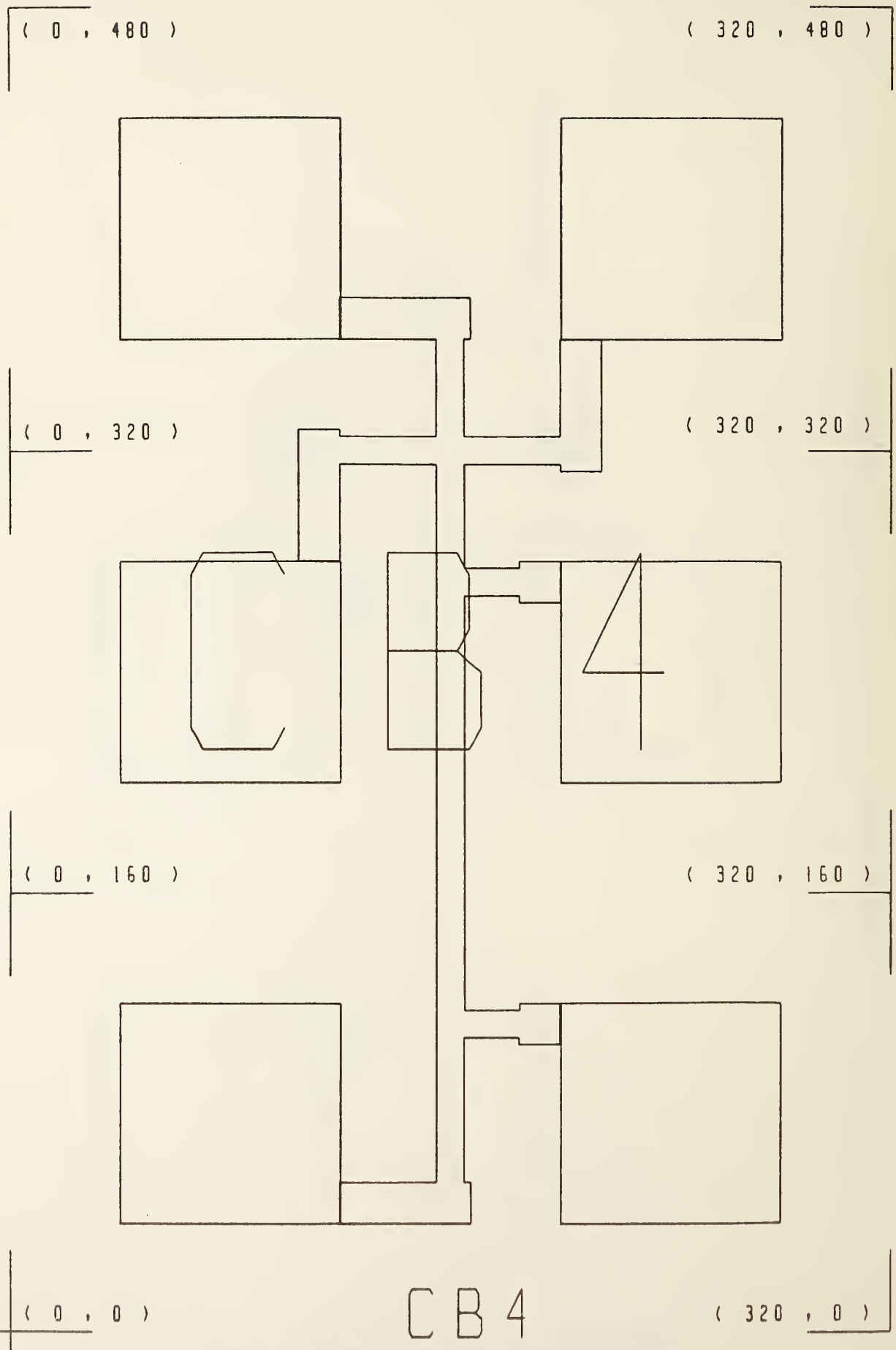


Figure 4. Cross-bridge sheet resistor CB-4.

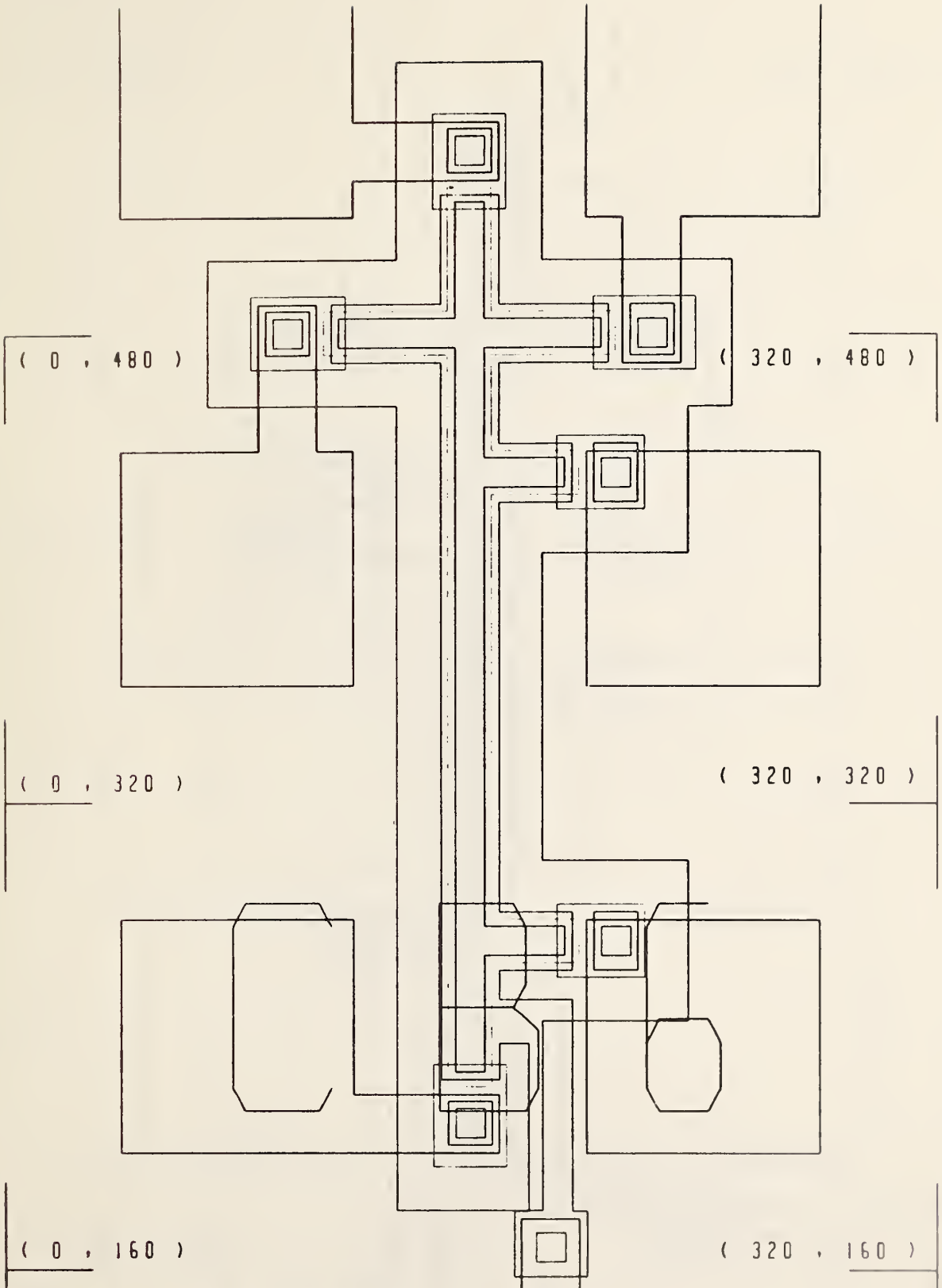


Figure 5. Cross-bridge sheet resistor CB-6.

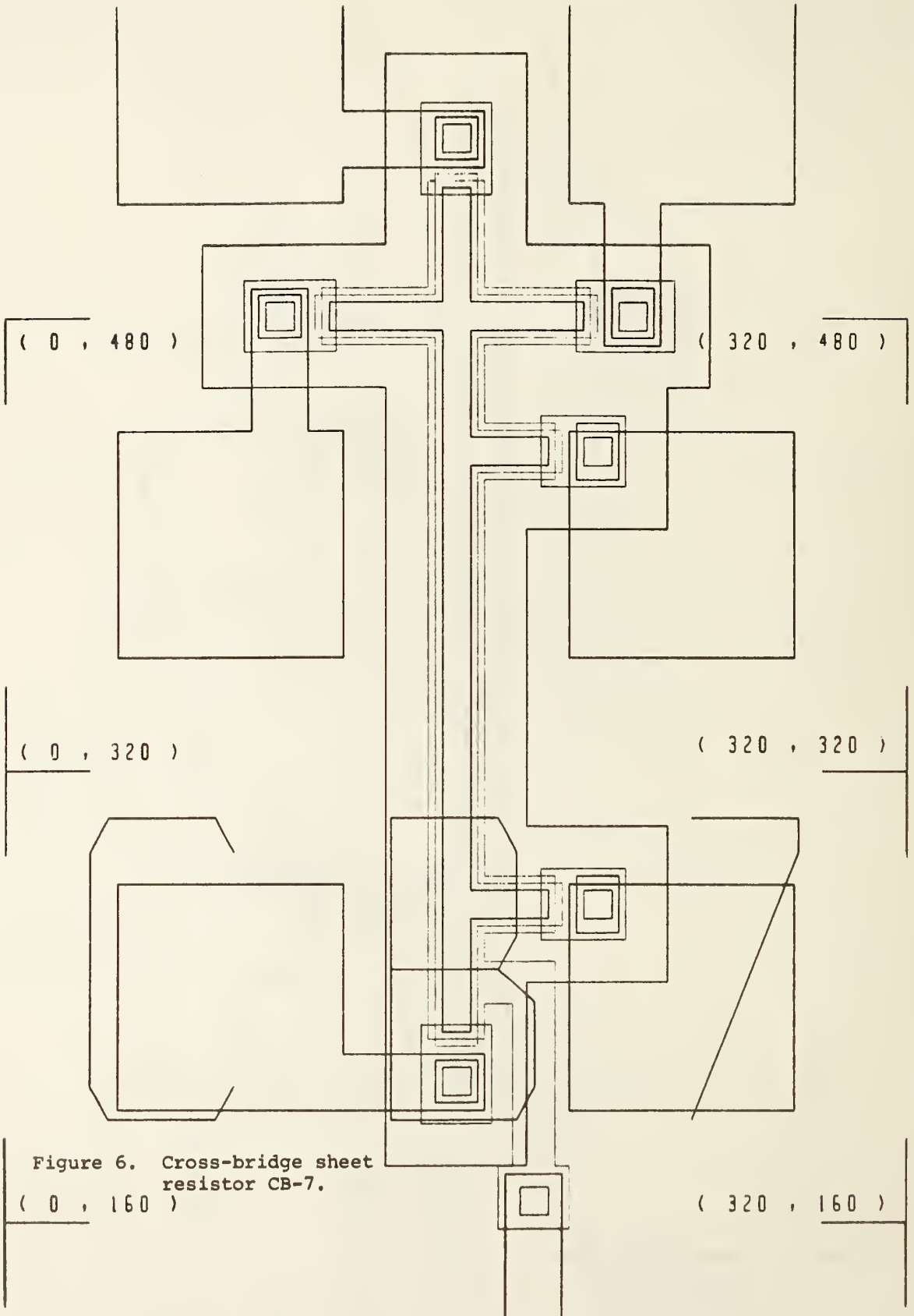


Figure 6. Cross-bridge sheet resistor CB-7.

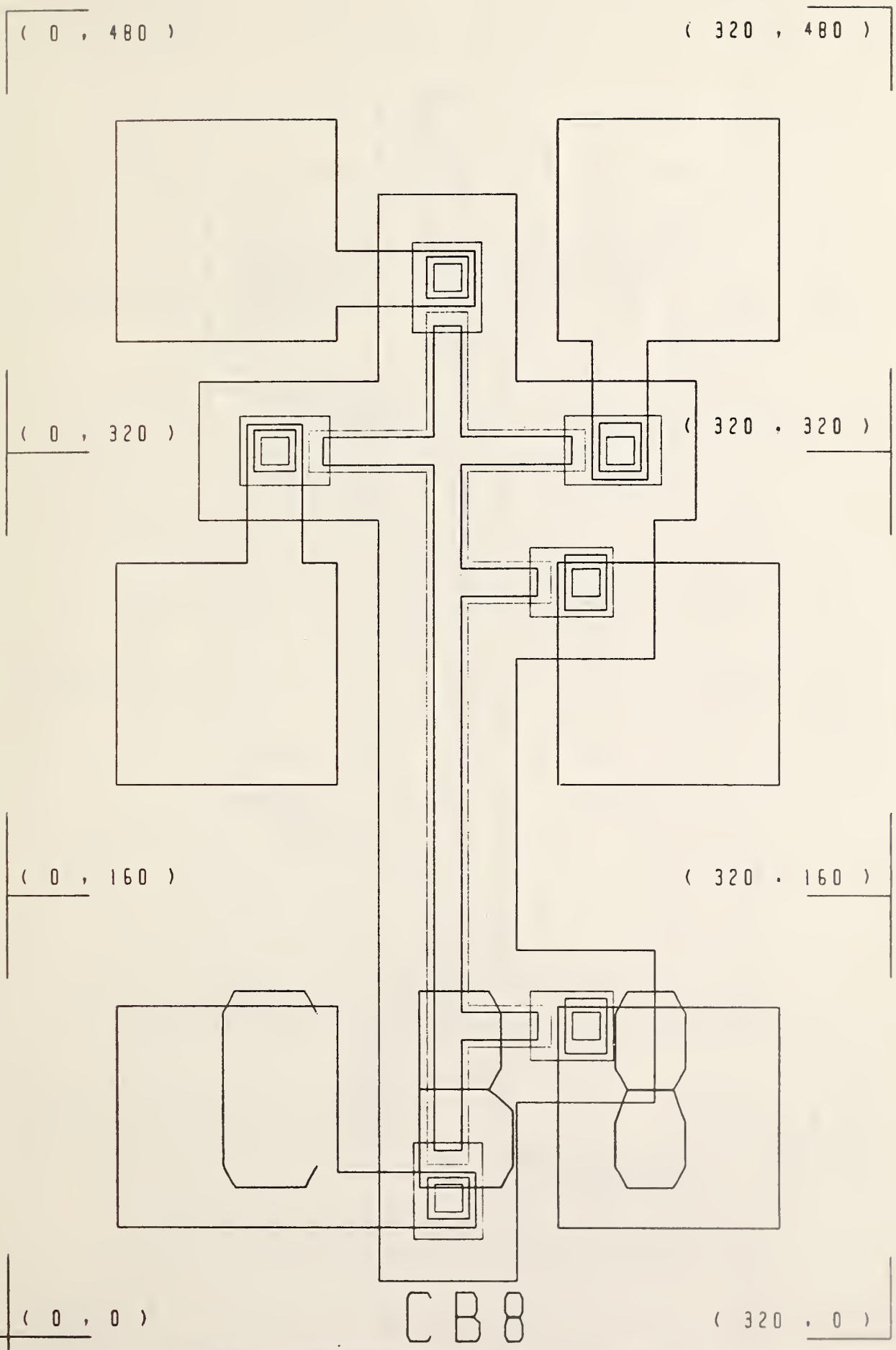


Figure 7. Cross-bridge sheet resistor CB-8.

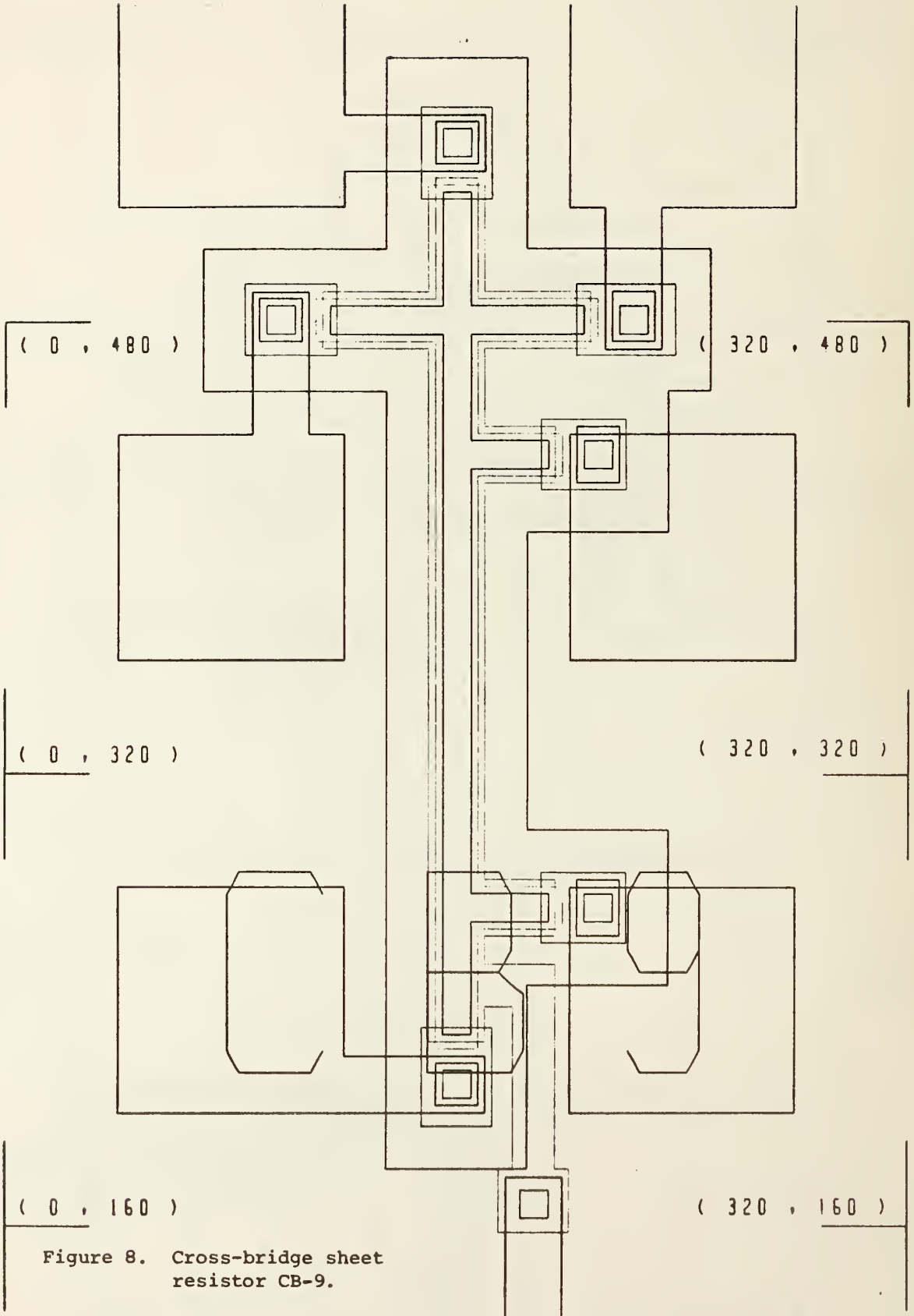


Figure 8. Cross-bridge sheet resistor CB-9.

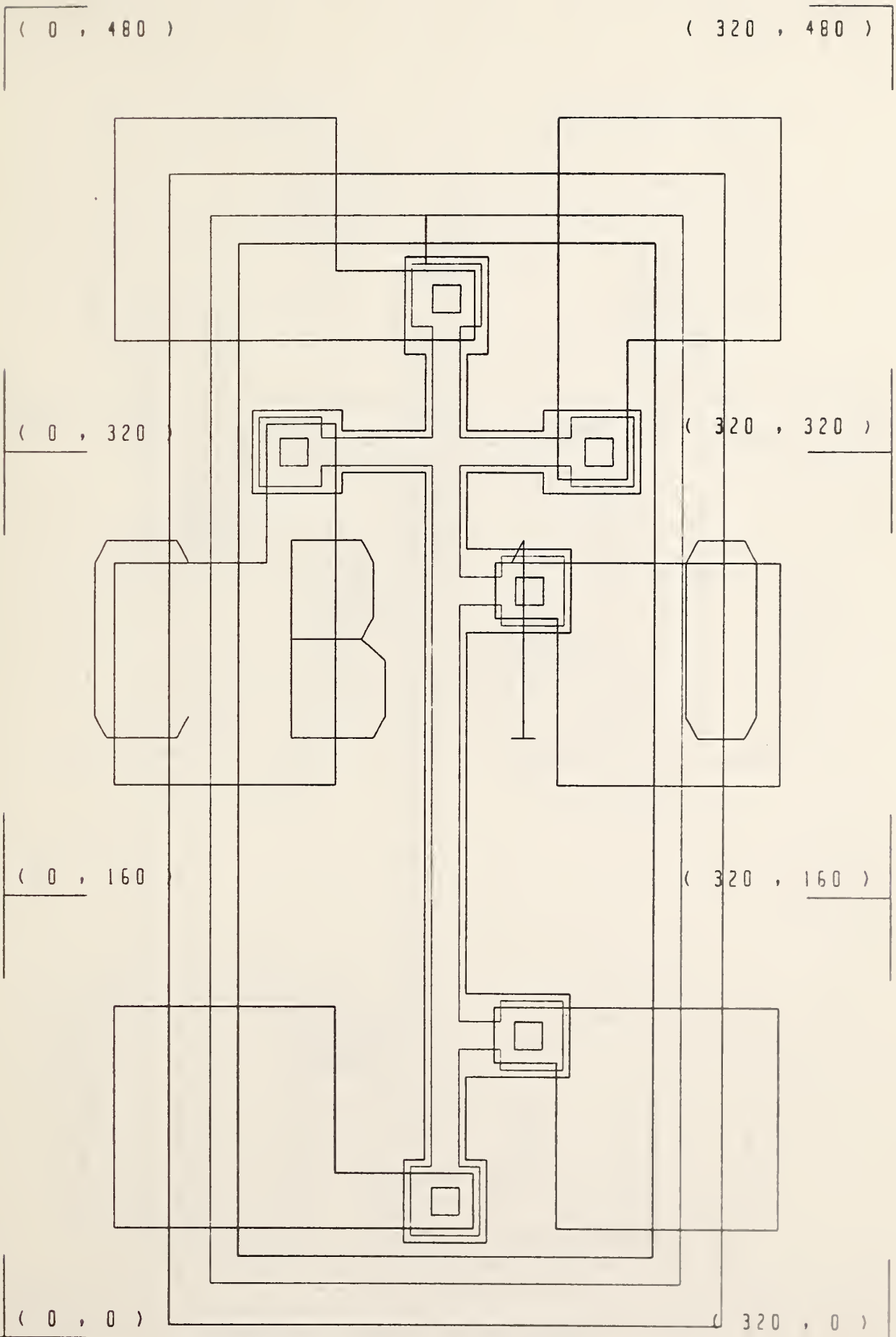


Figure 9. Cross-bridge sheet resistor CB-10.

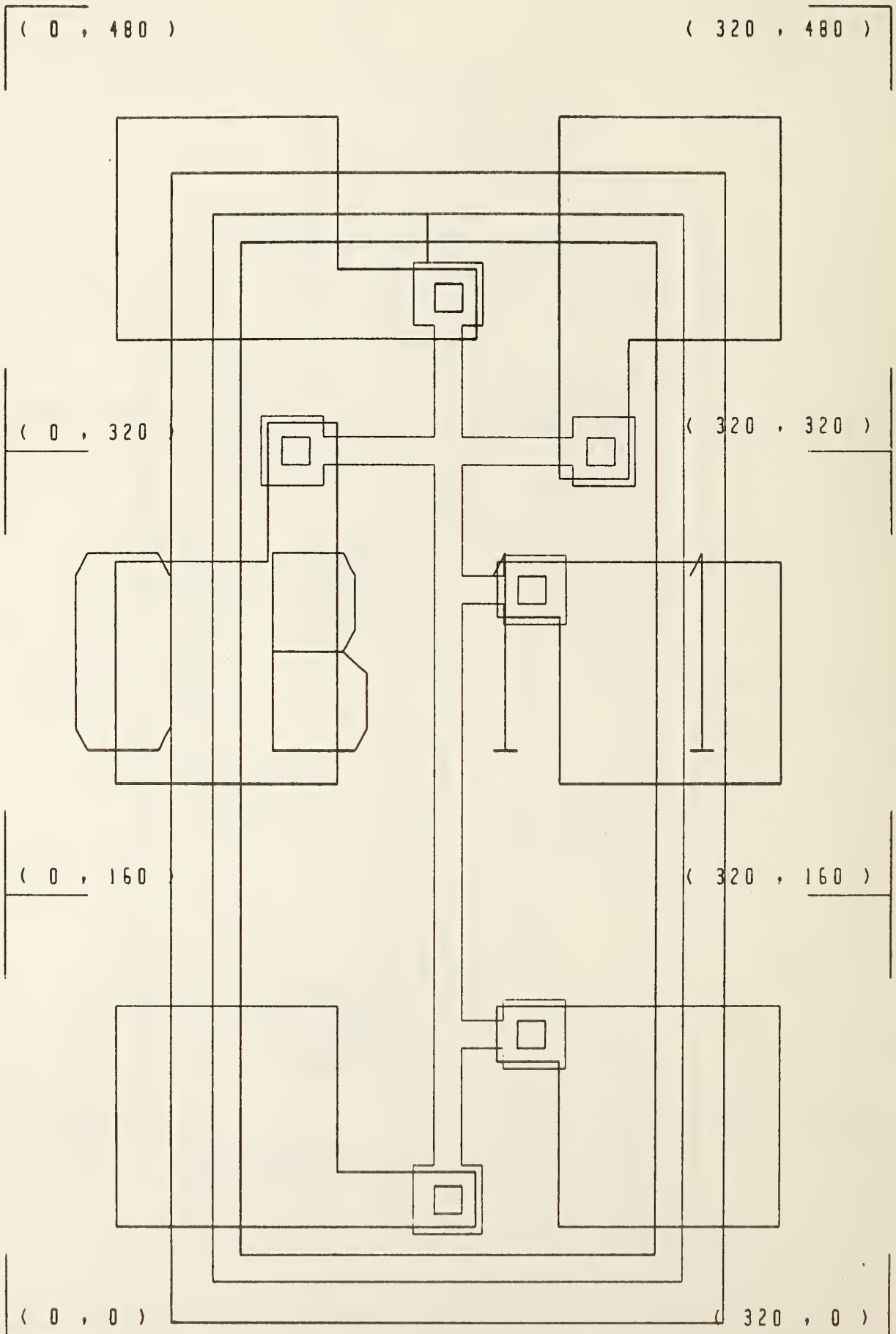


Figure 10. Cross-bridge sheet resistor CB-11,

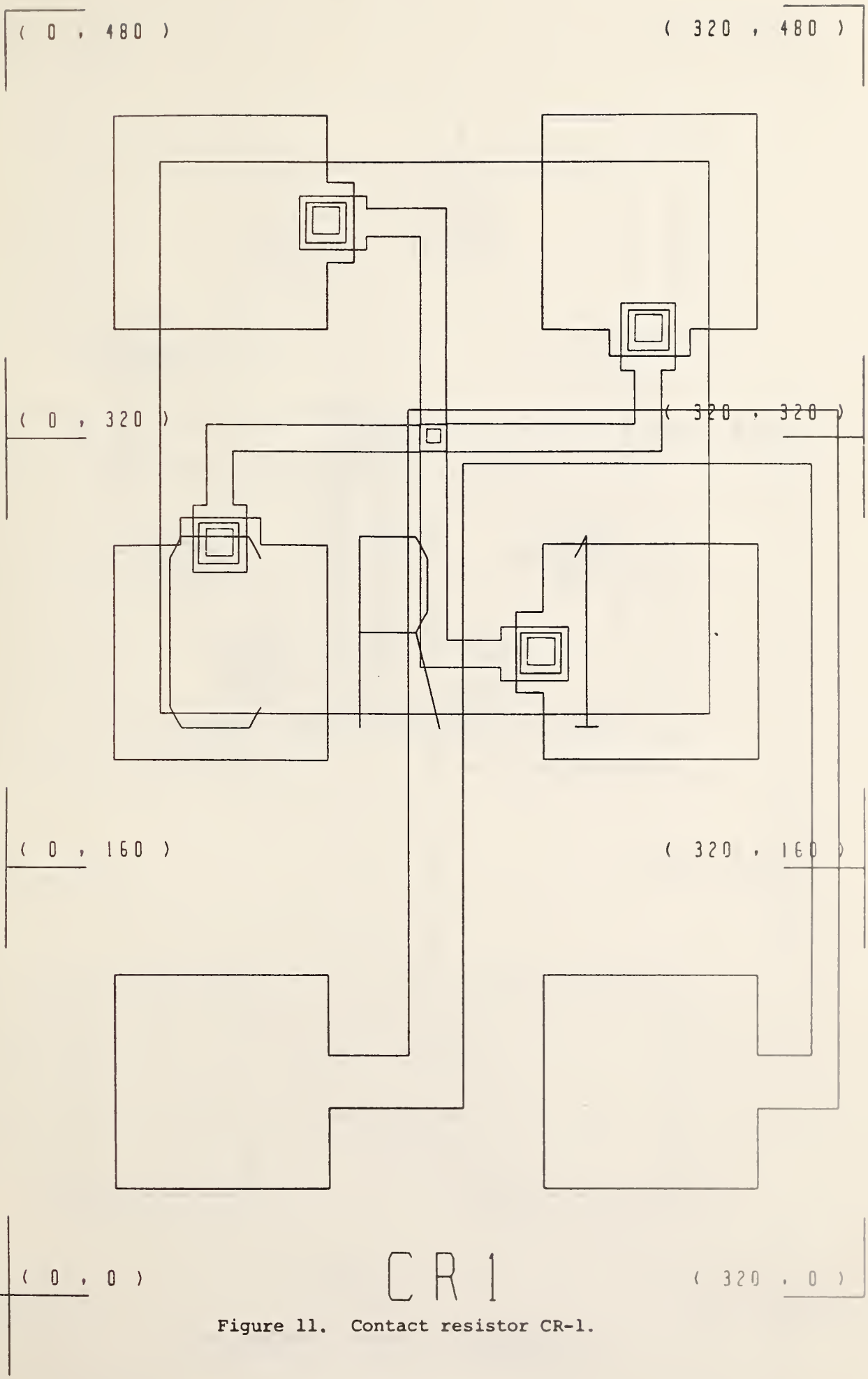


Figure 11. Contact resistor CR-1.

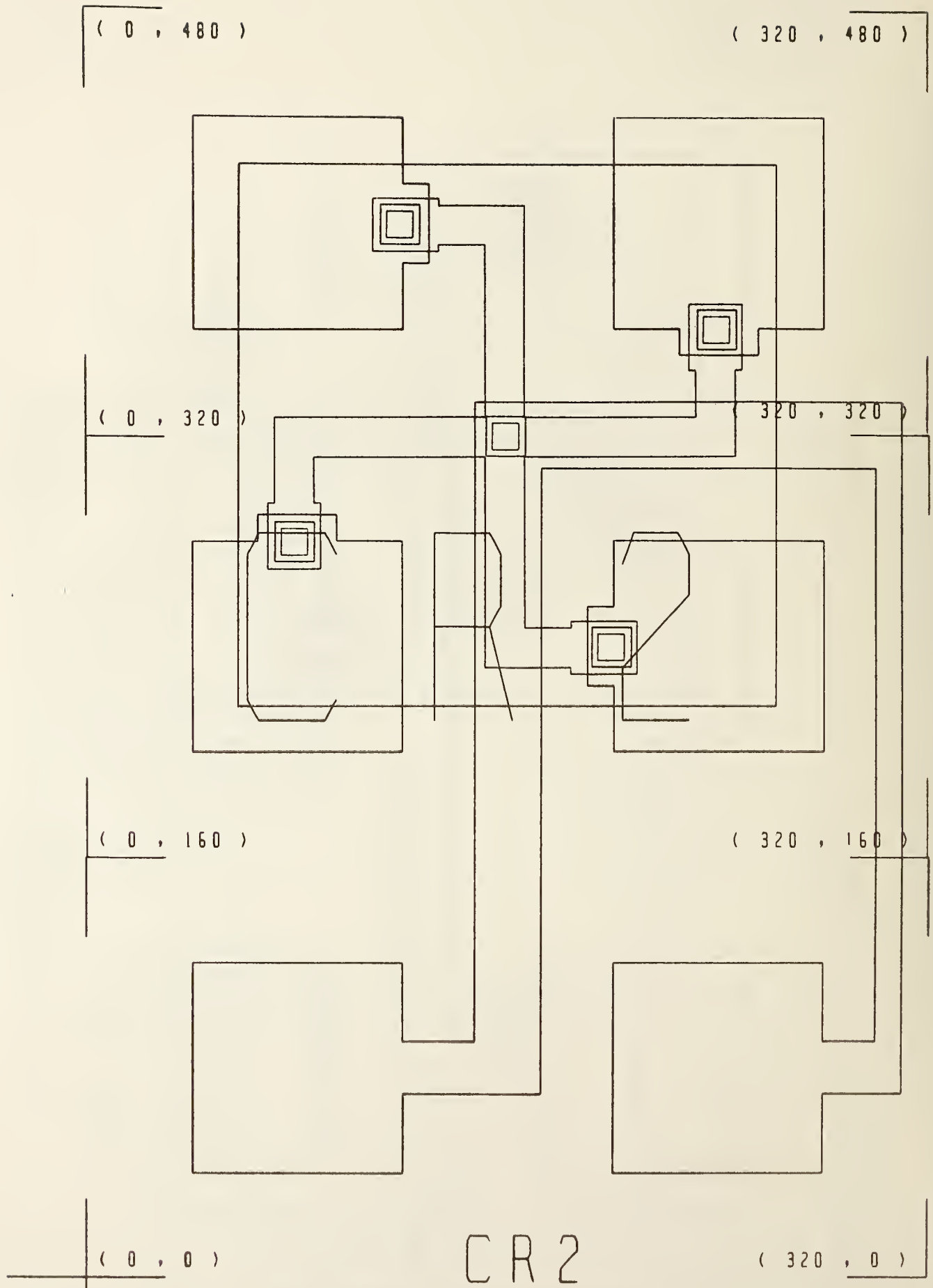


Figure 12. Contact resistor CR-2.

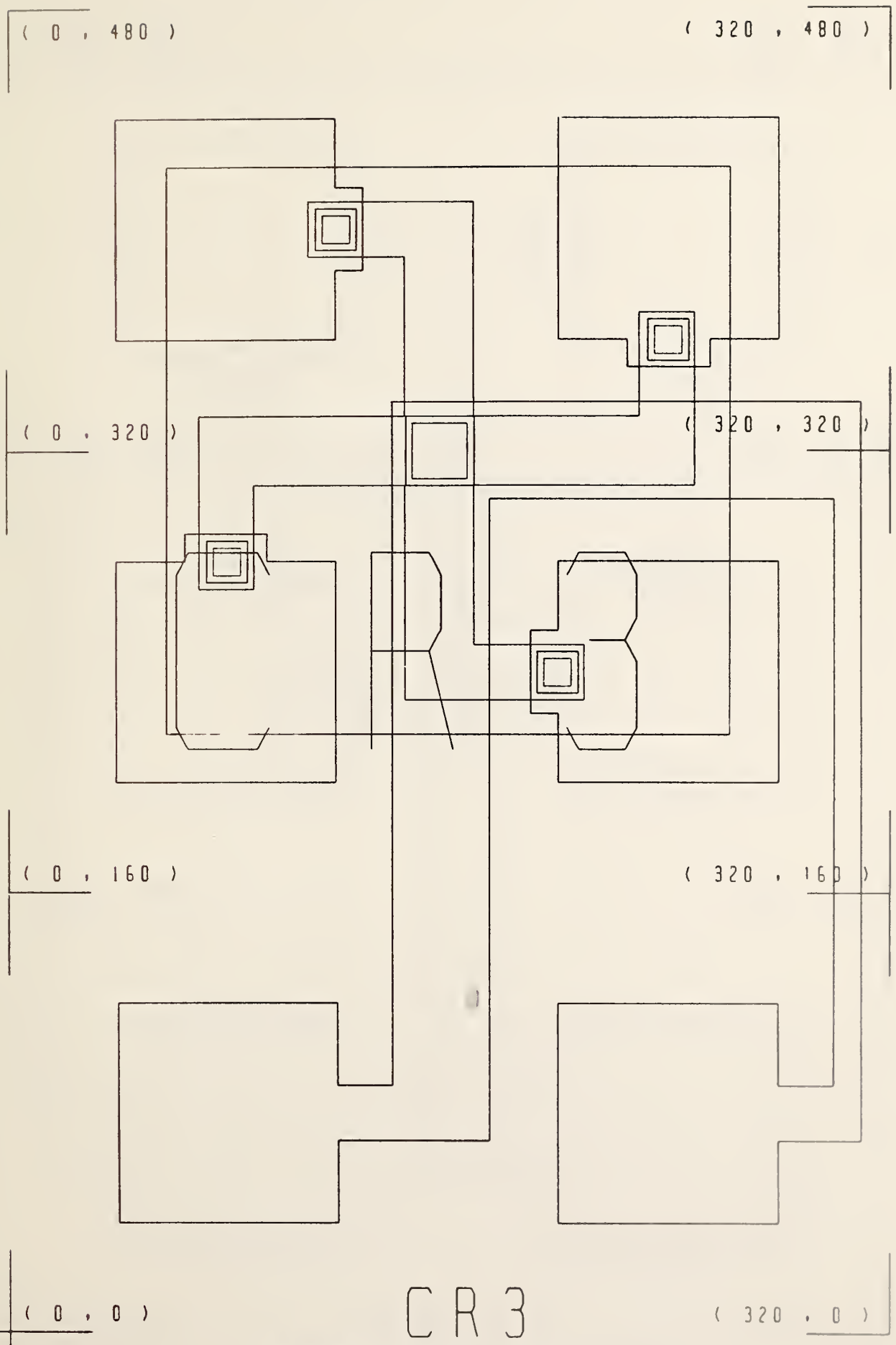


Figure 13. Contact resistor CR-3.

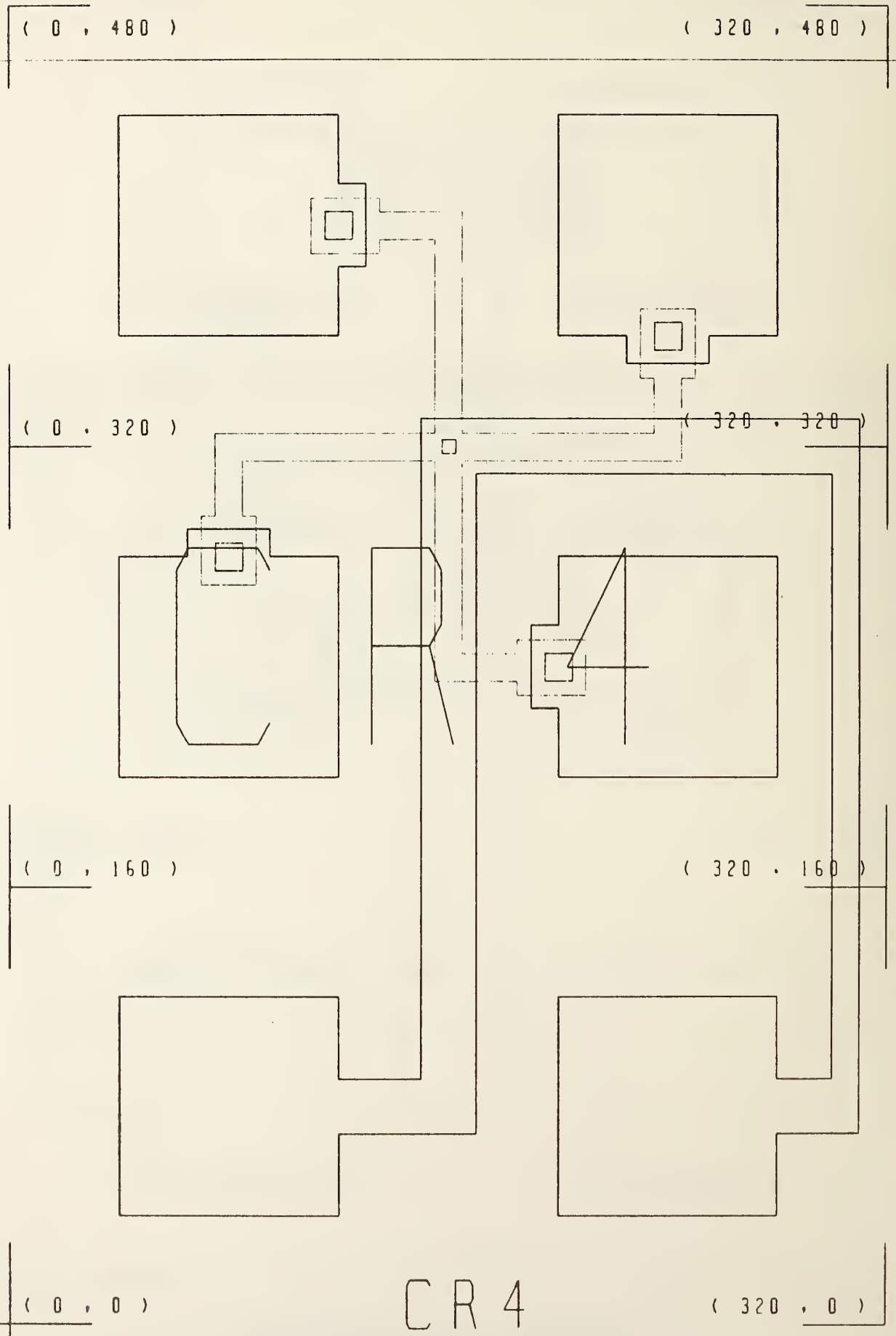


Figure 14. Contact resistor CR-4.

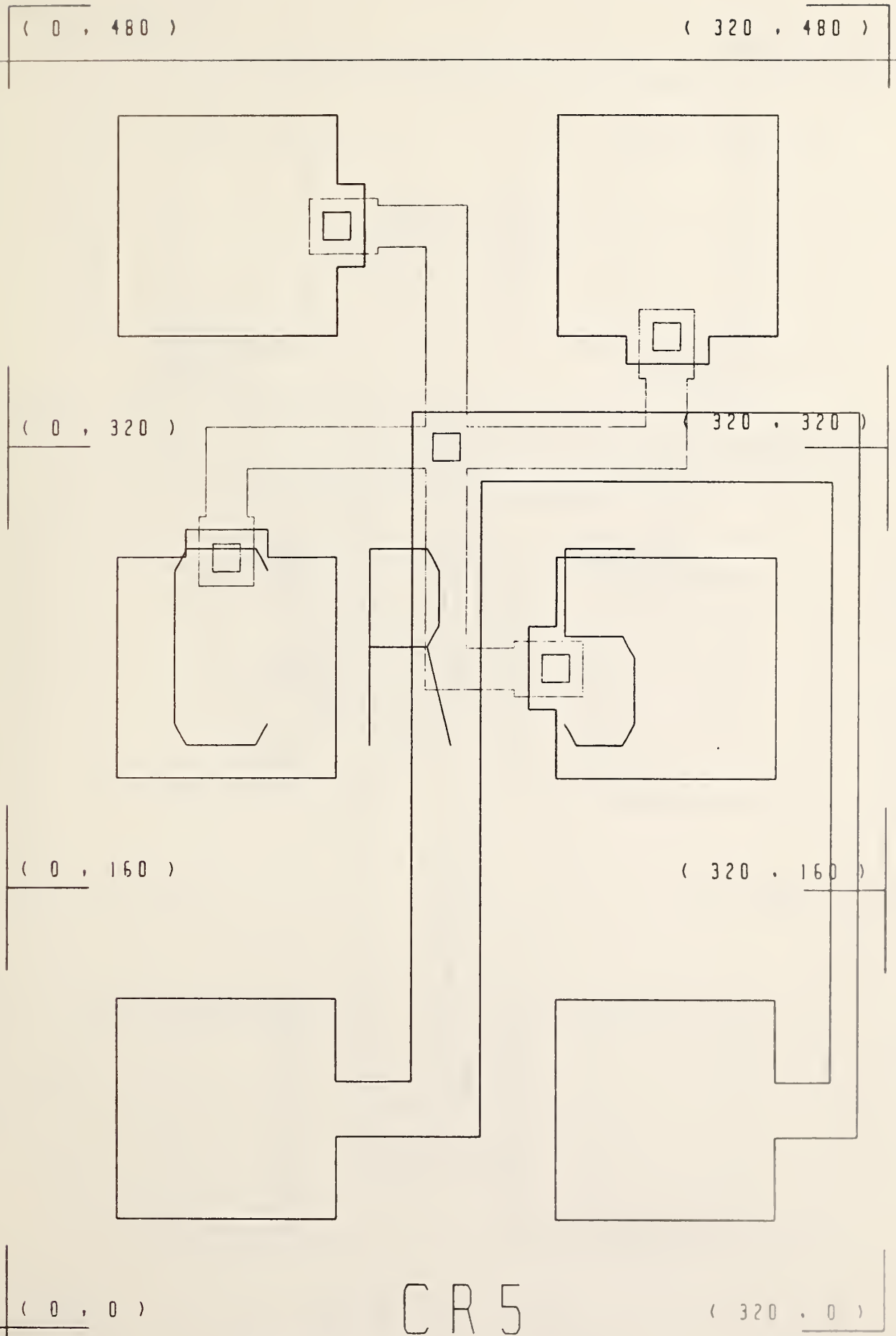


Figure 15. Contact resistor CR-5.

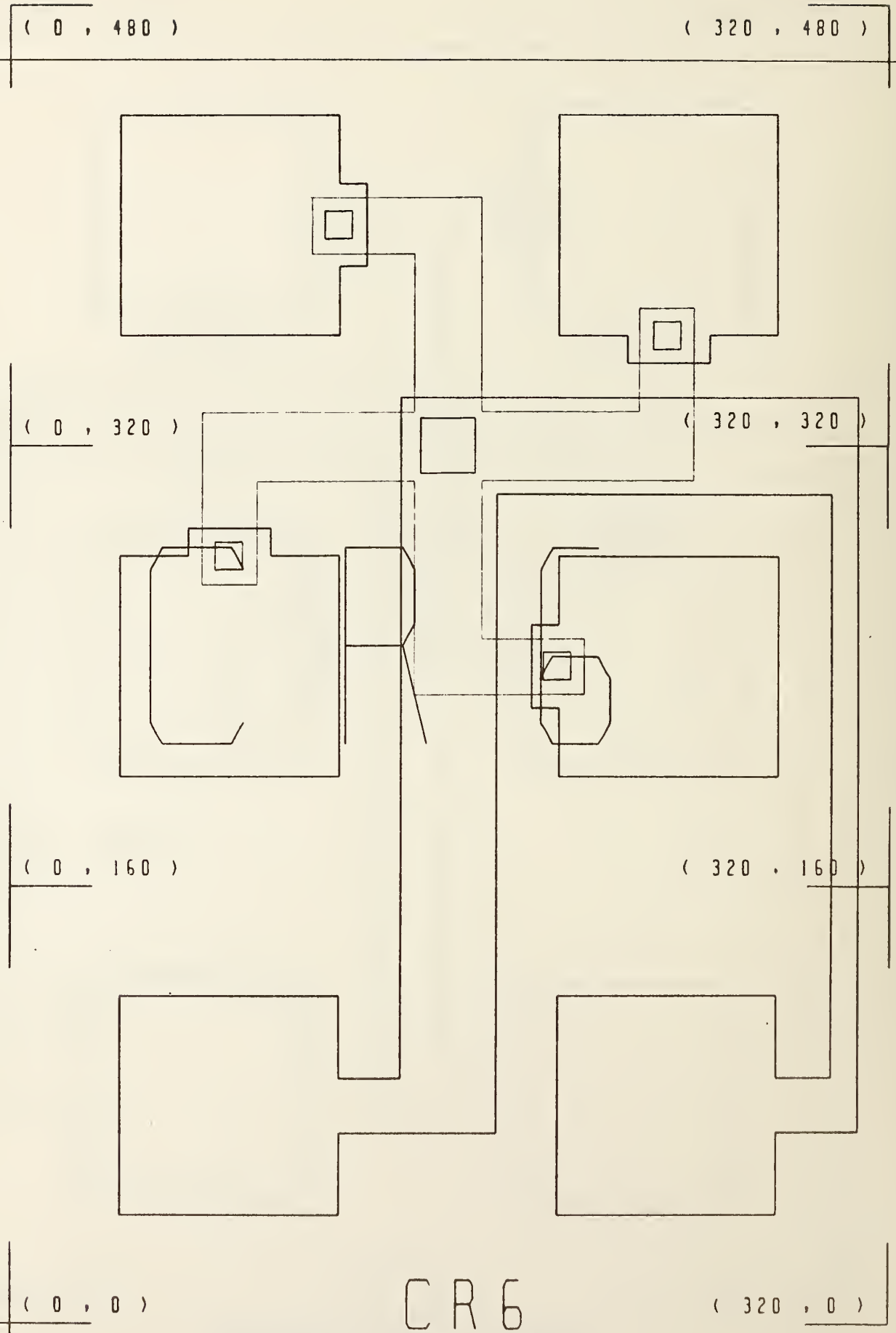


Figure 16. Contact resistor CR-6.

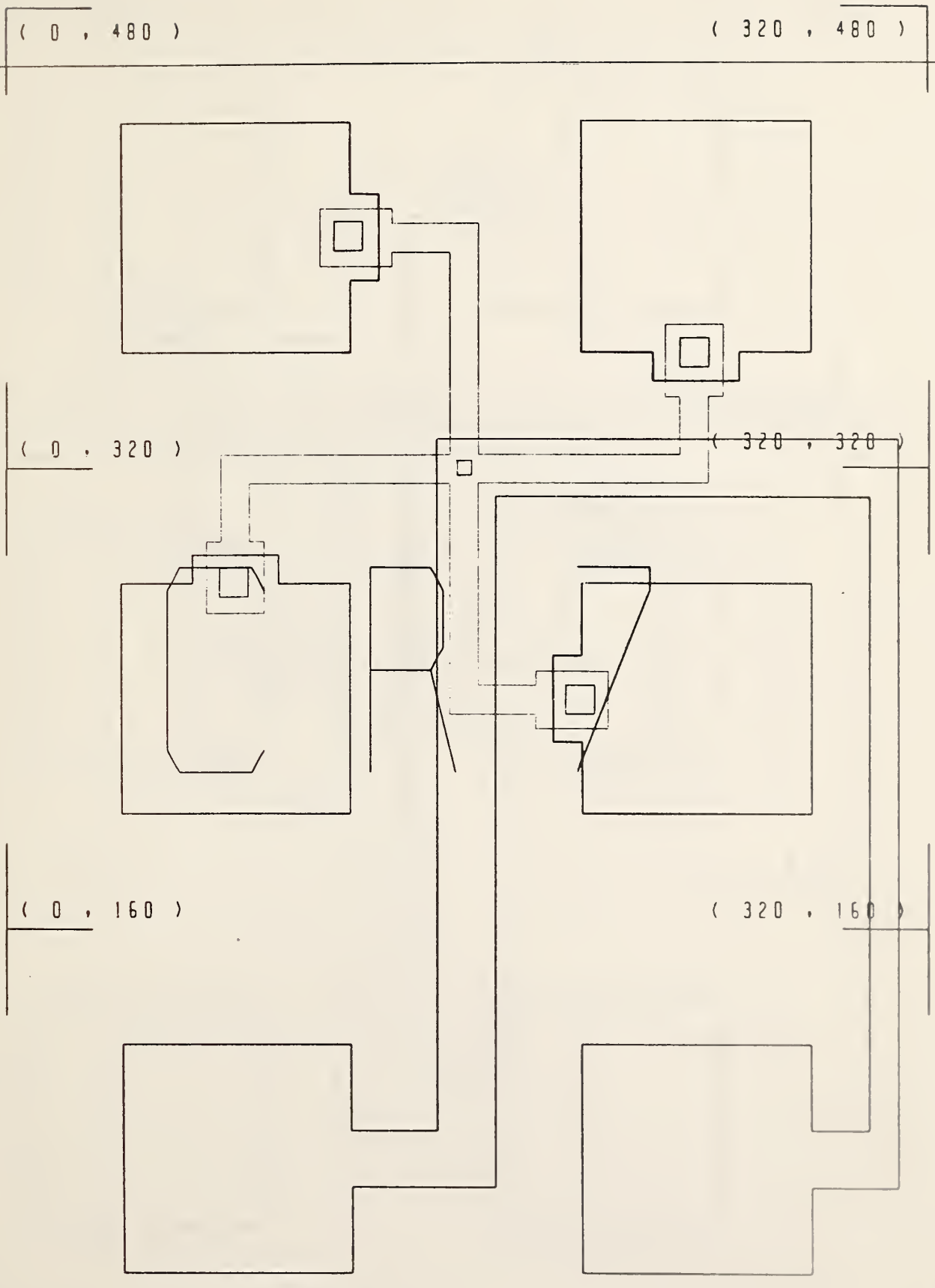


Figure 17. Contact resistor CR-7.

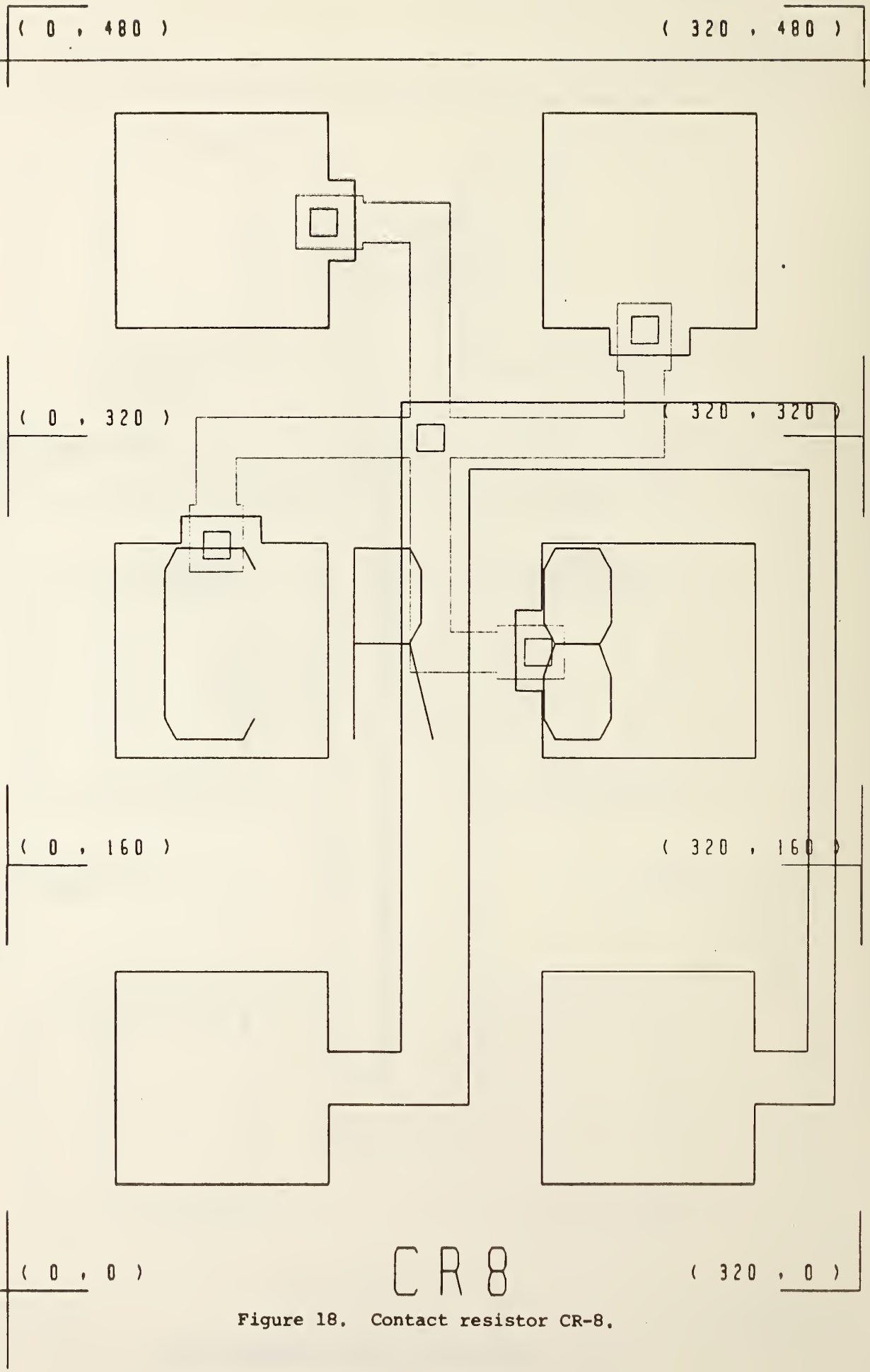


Figure 18. Contact resistor CR-8.

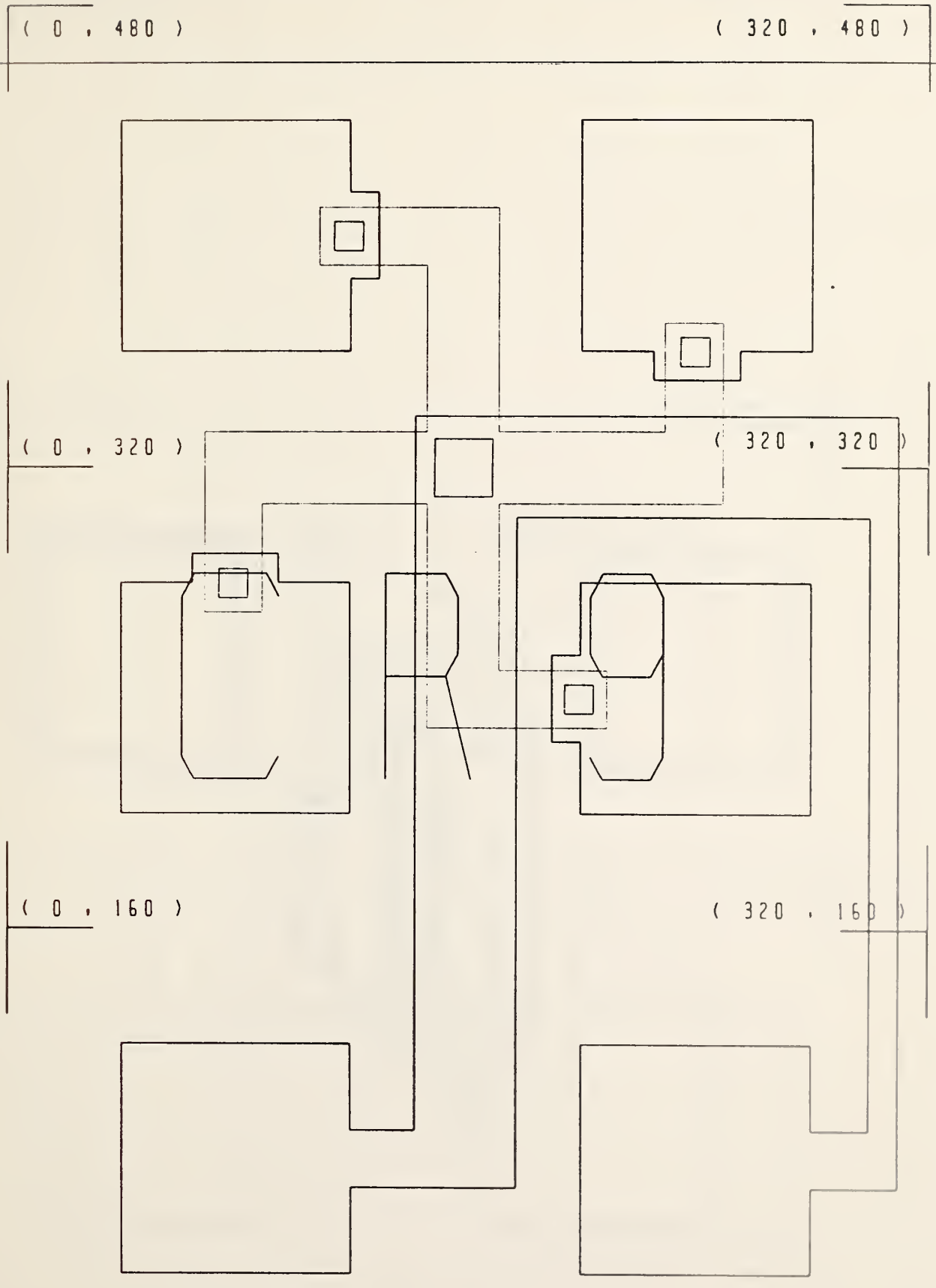


Figure 19. Contact resistor CR-9.

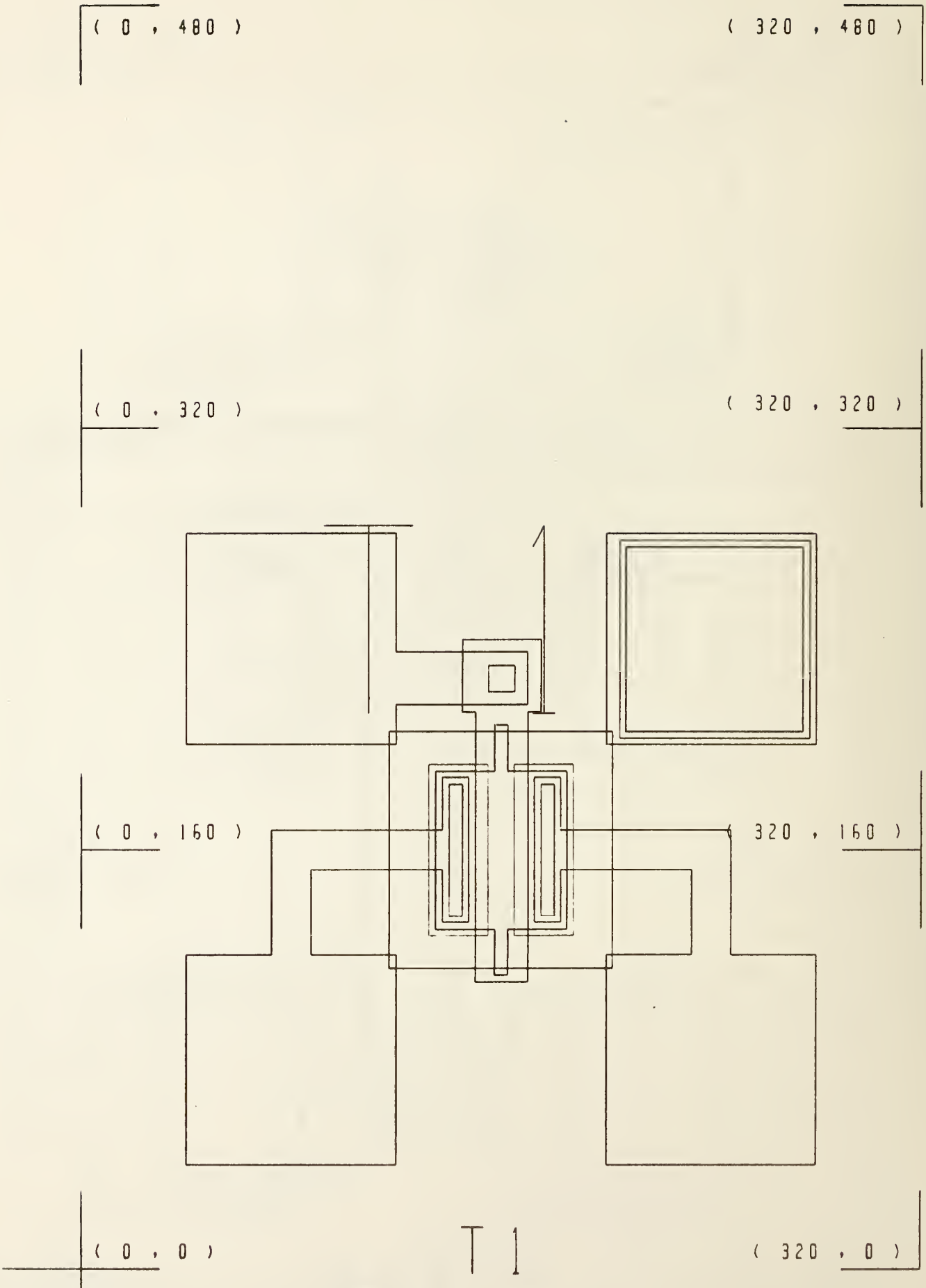


Figure 20. MOSFET T-1.

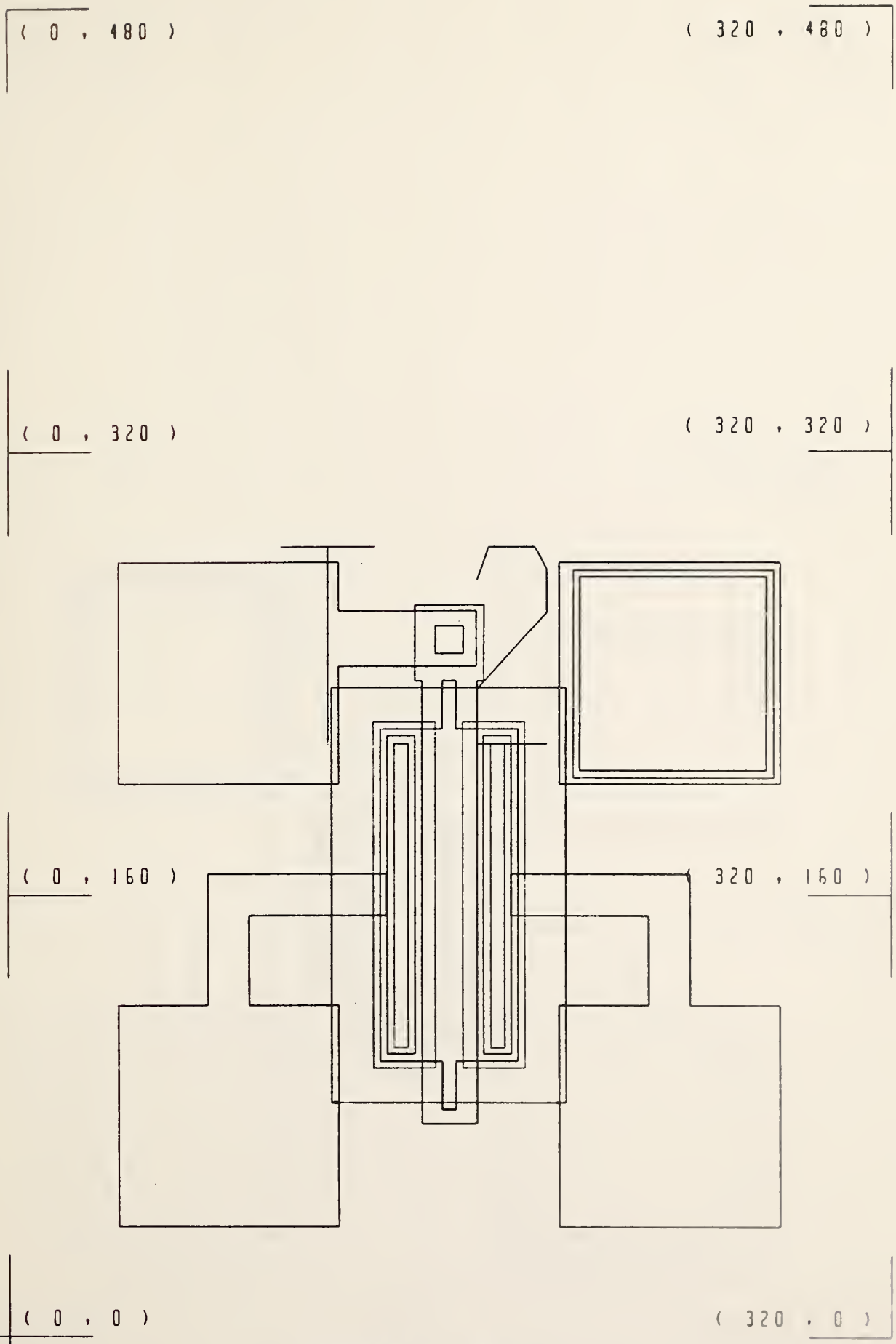


Figure 21. MOSFET T-2.

T 2

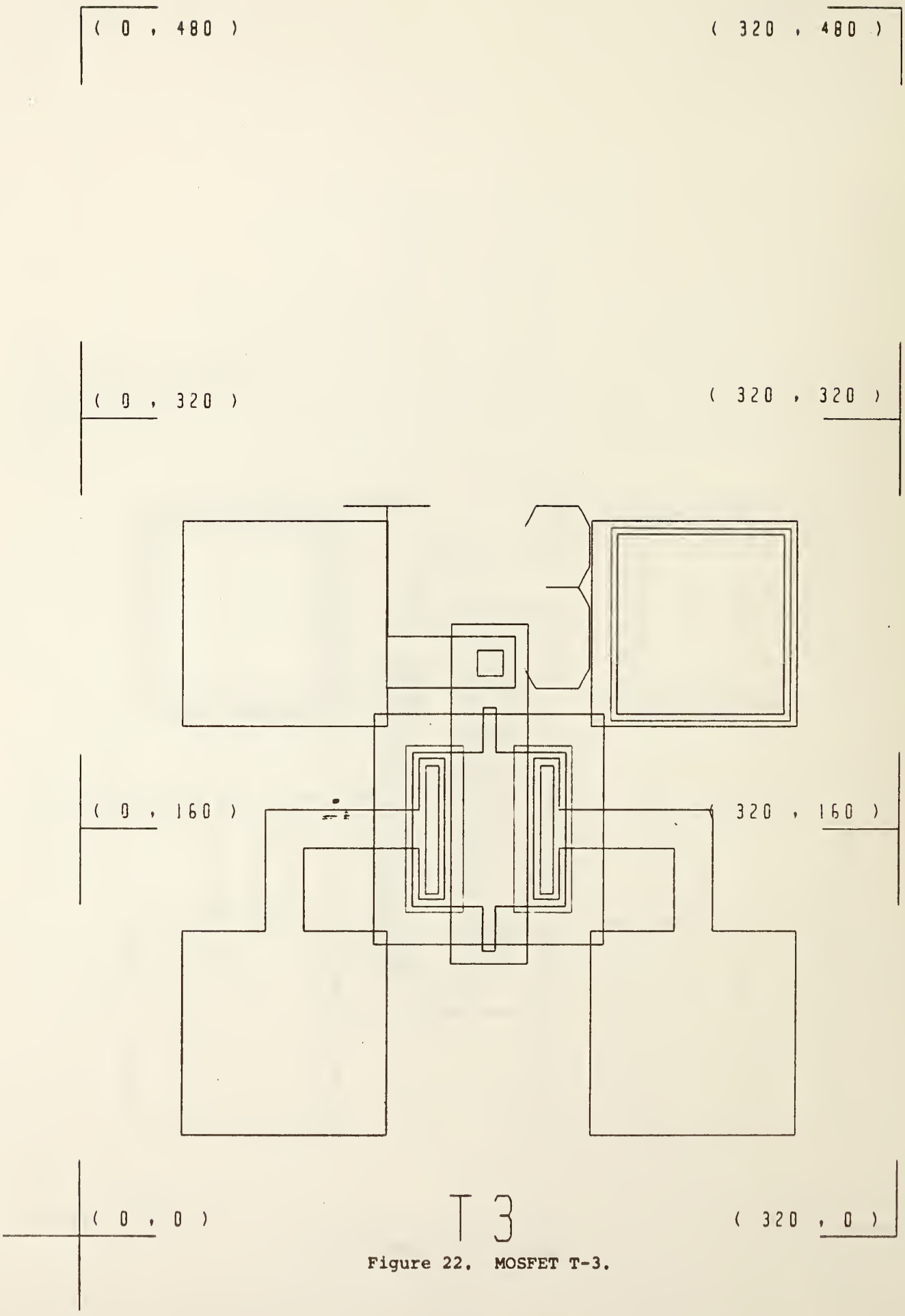


Figure 22. MOSFET T-3.

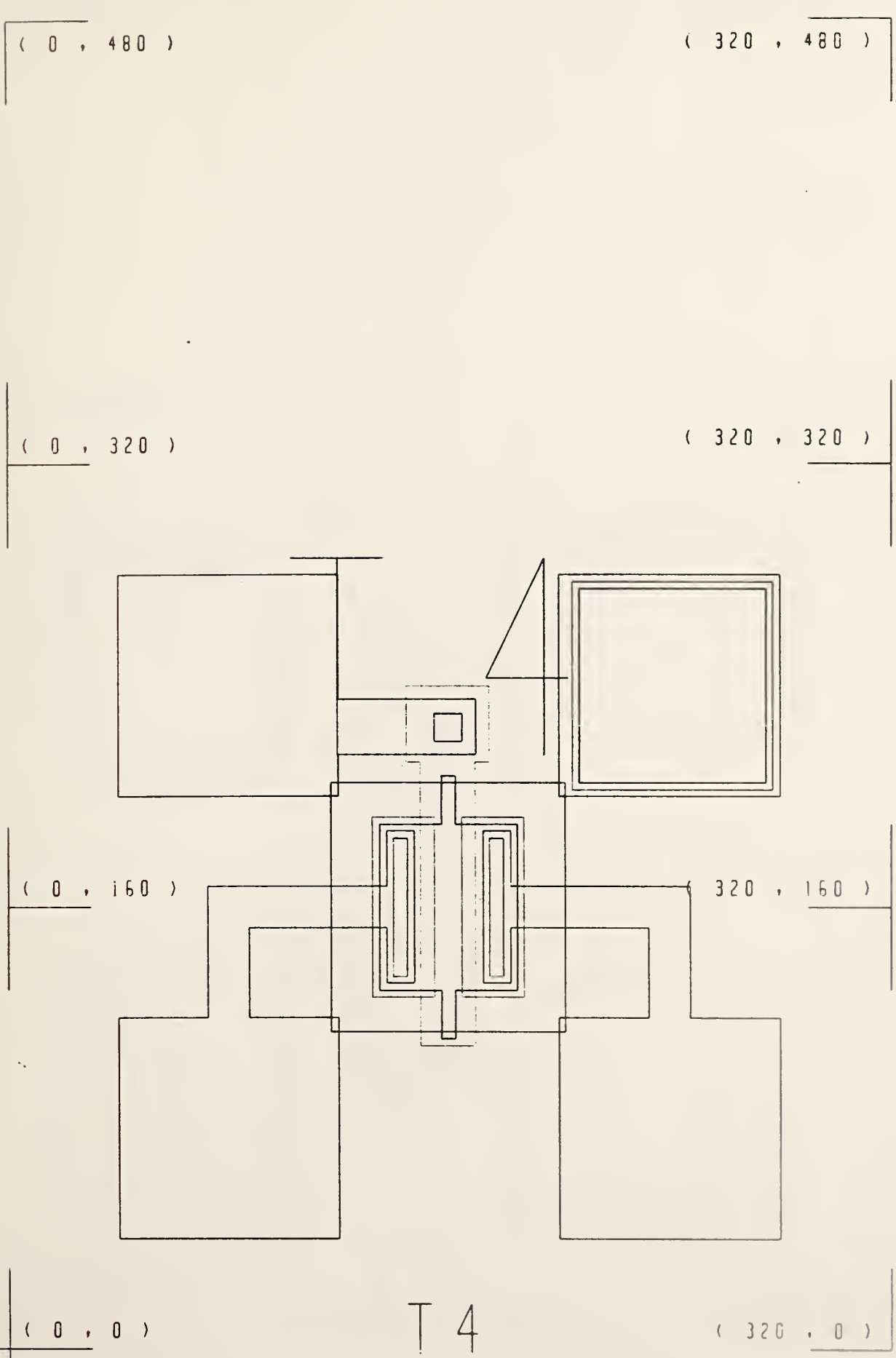


Figure 23. MOSFET T-4.

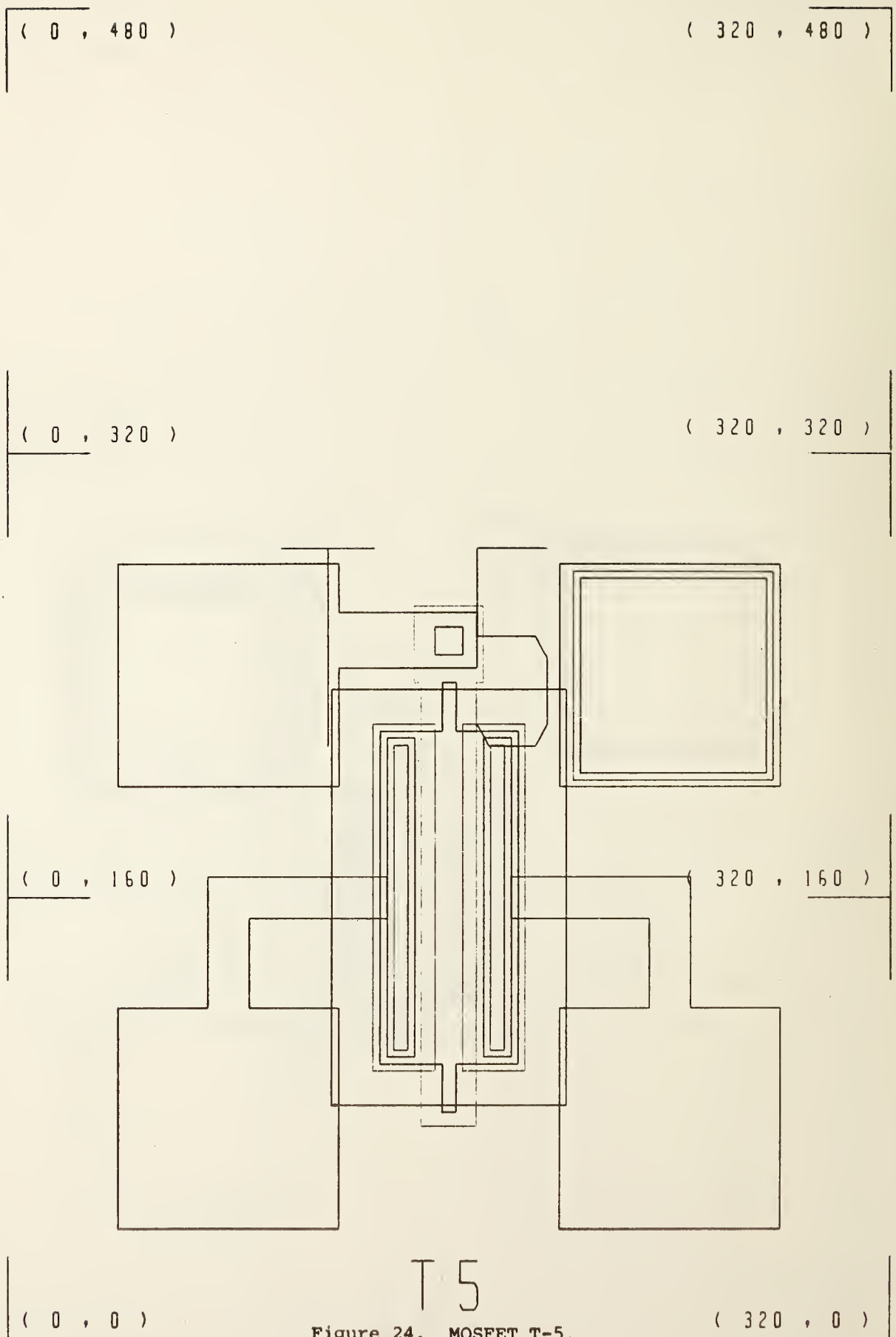


Figure 24. MOSFET T-5.

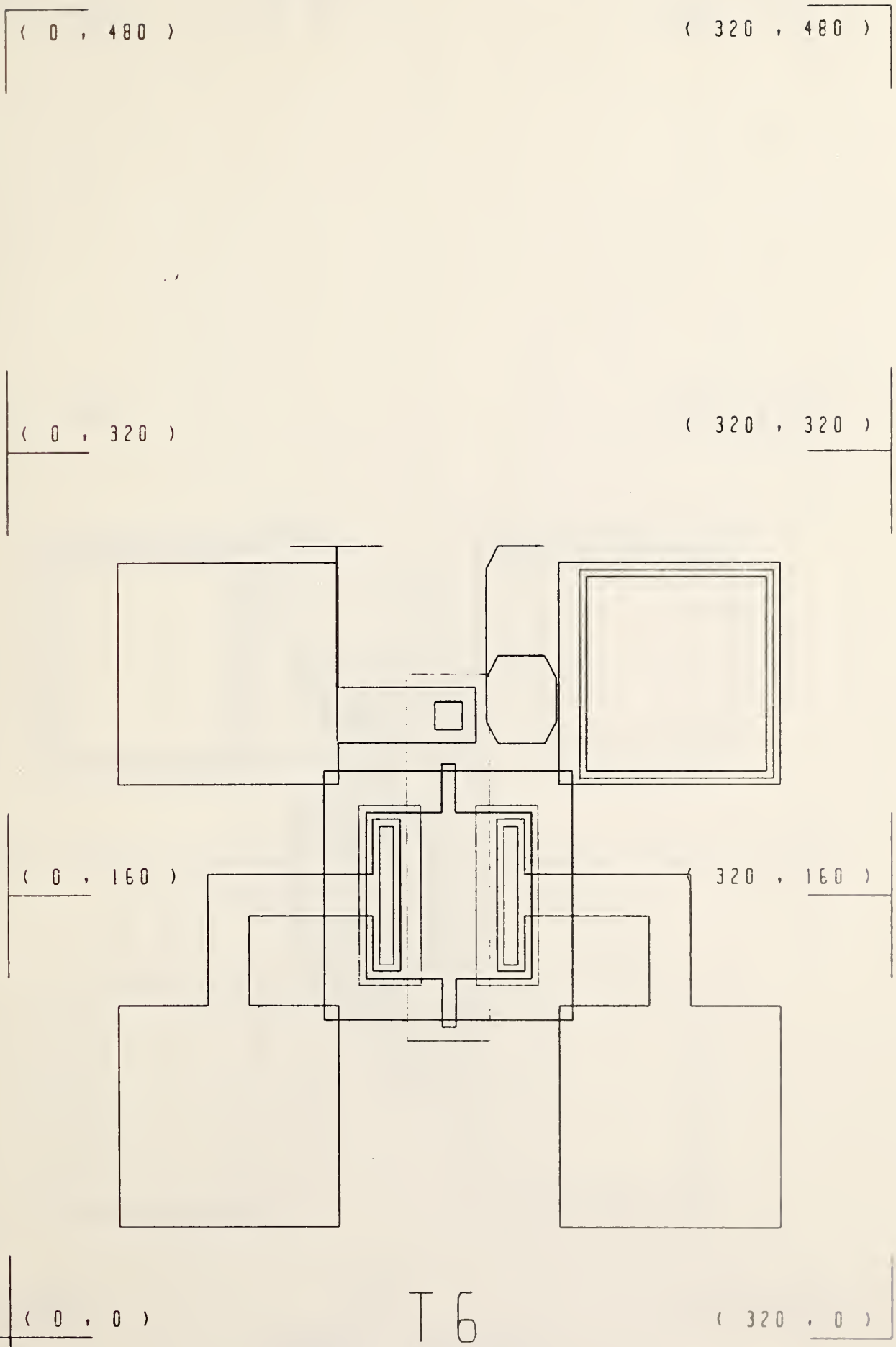


Figure 25. MOSFET T-6.

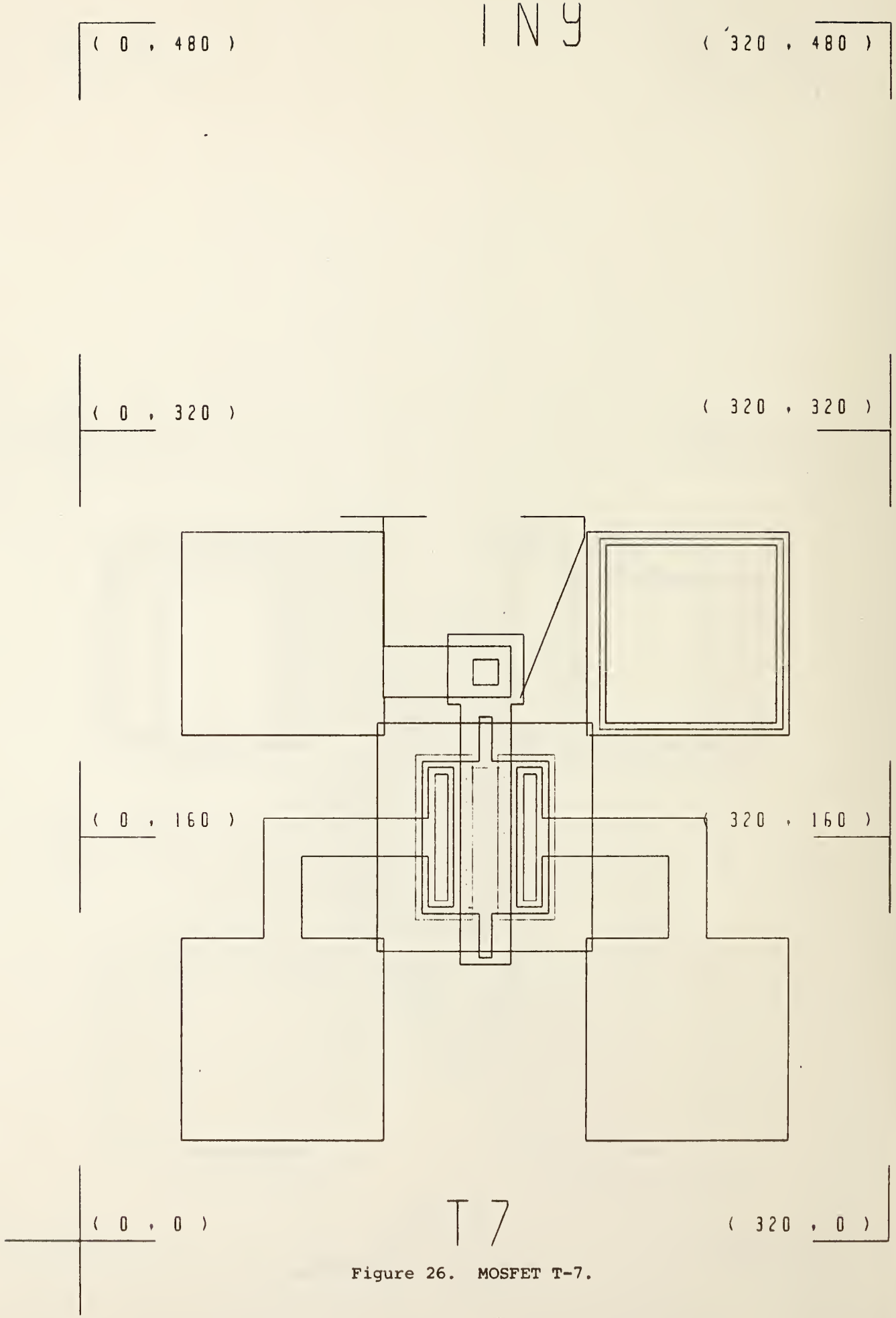


Figure 26. MOSFET T-7.

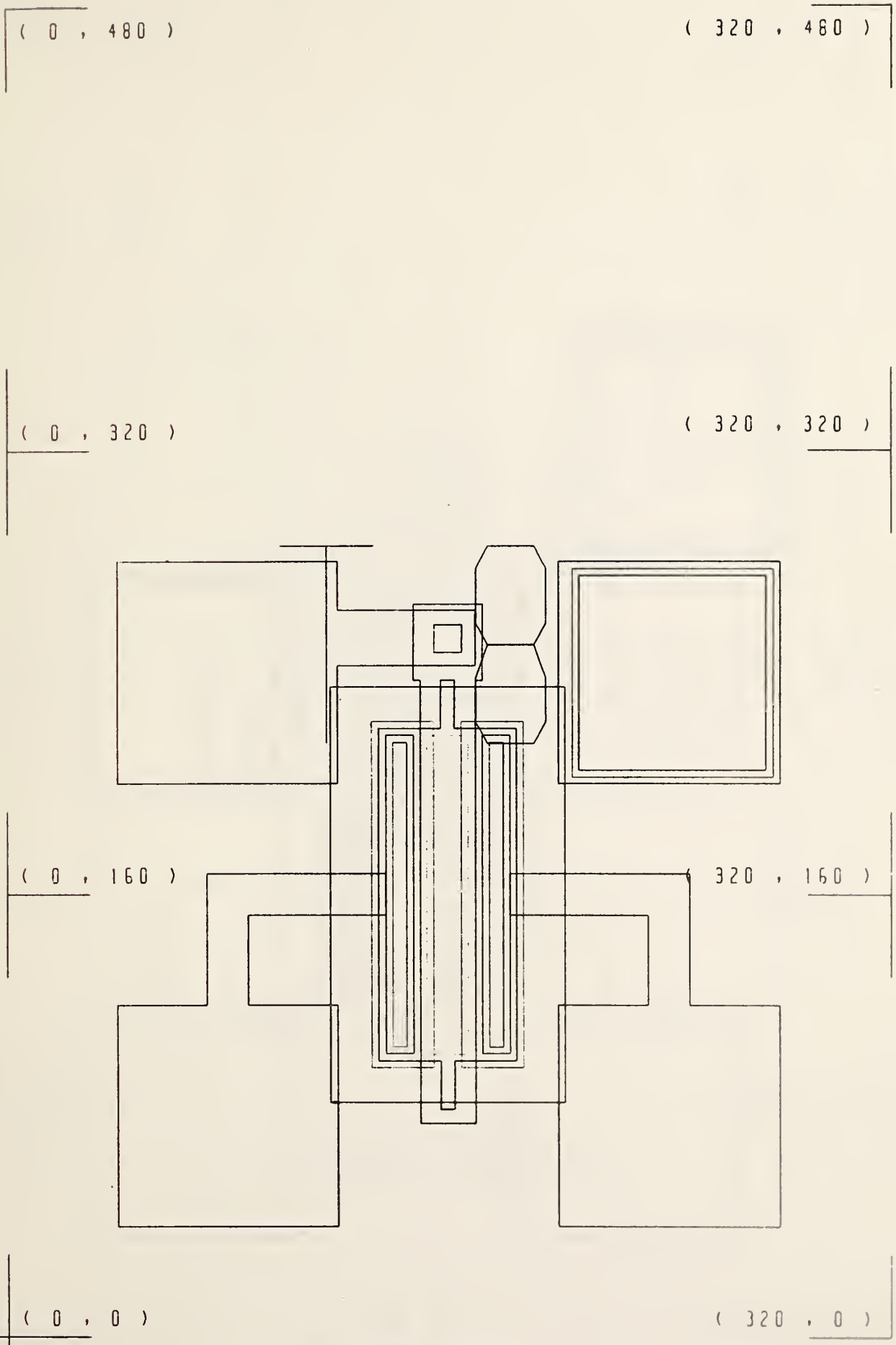


Figure 27. MOSFET T-8.

T 8

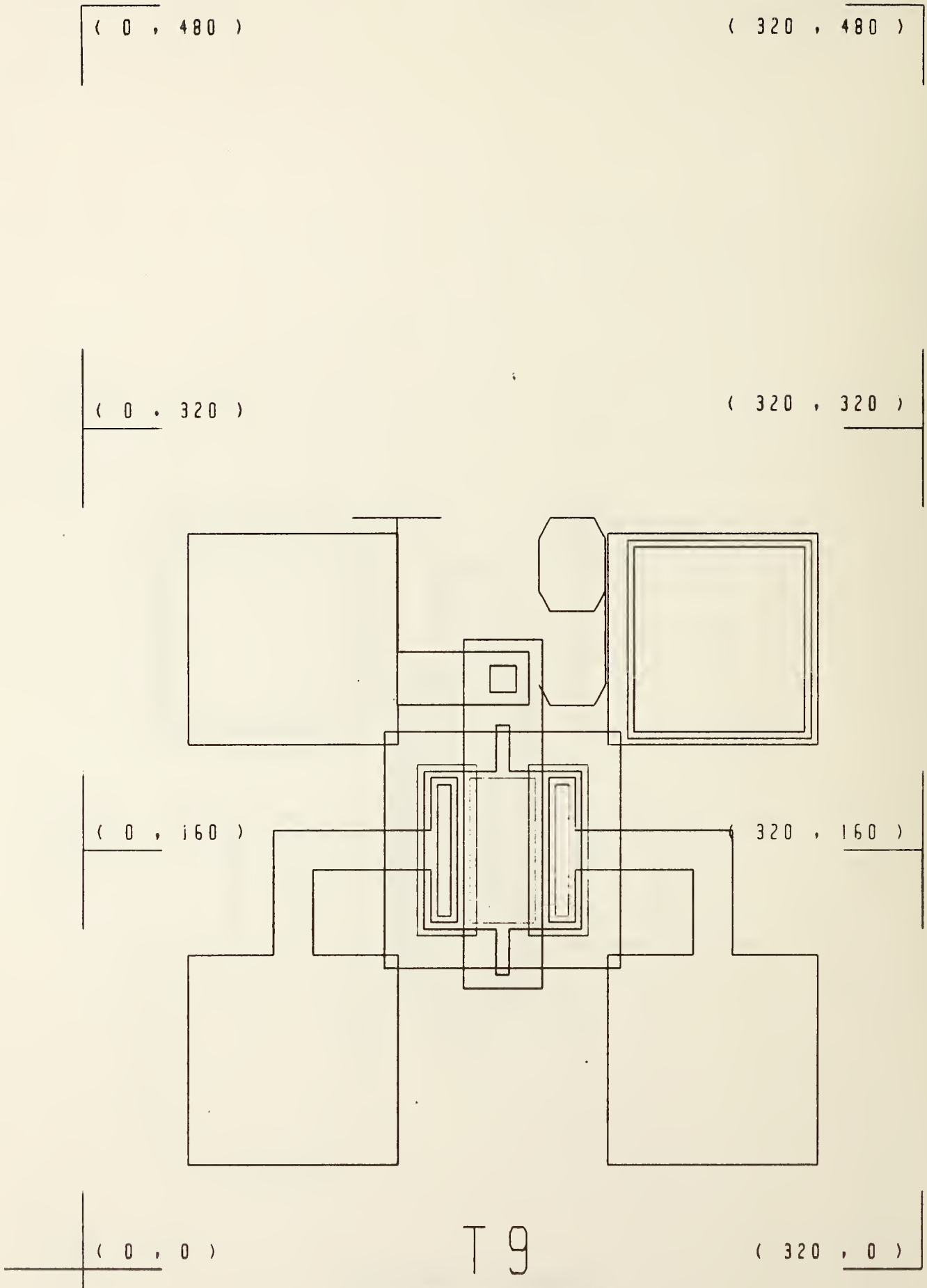


Figure 28. MOSFET T-9.

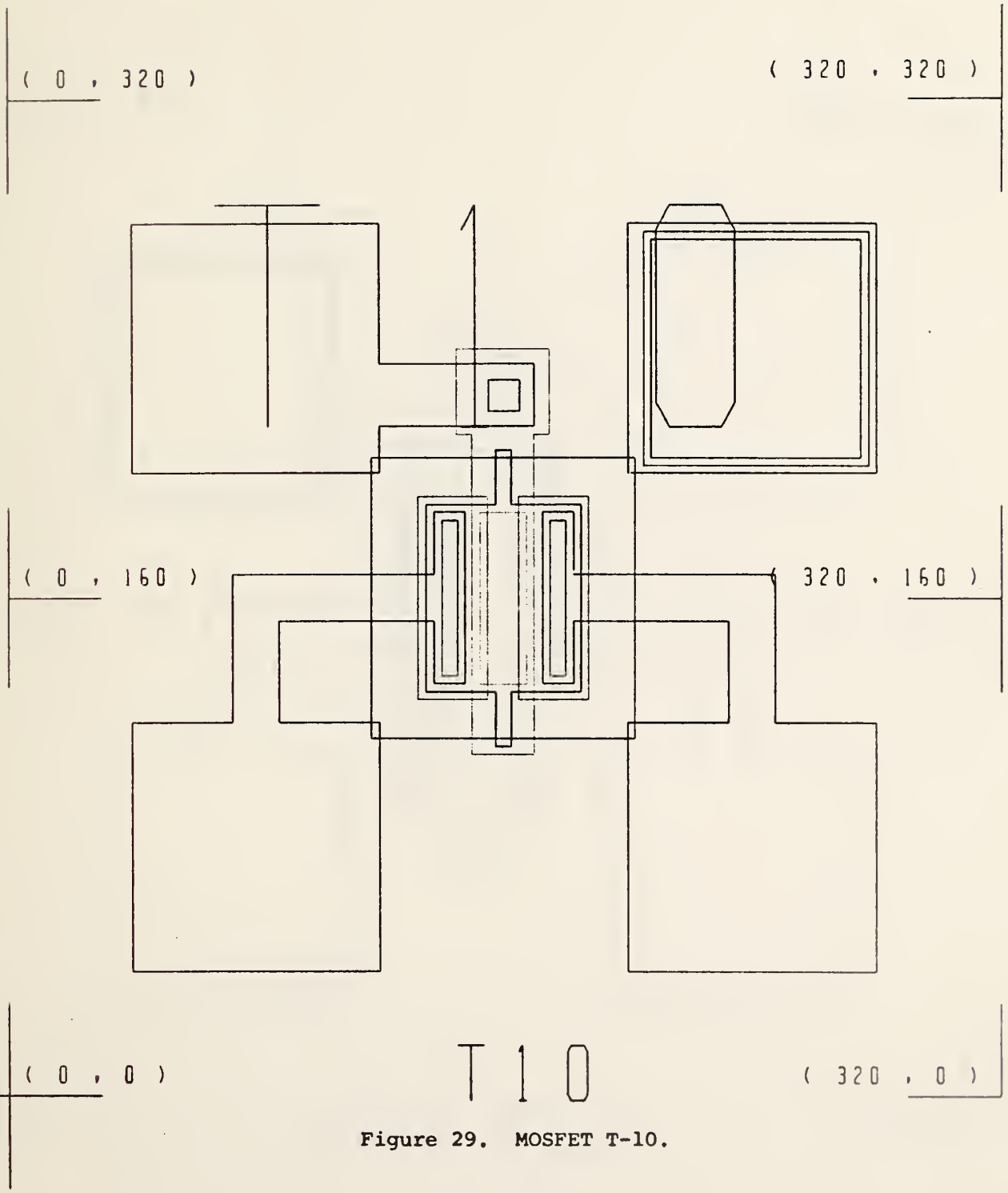


Figure 29. MOSFET T-10.

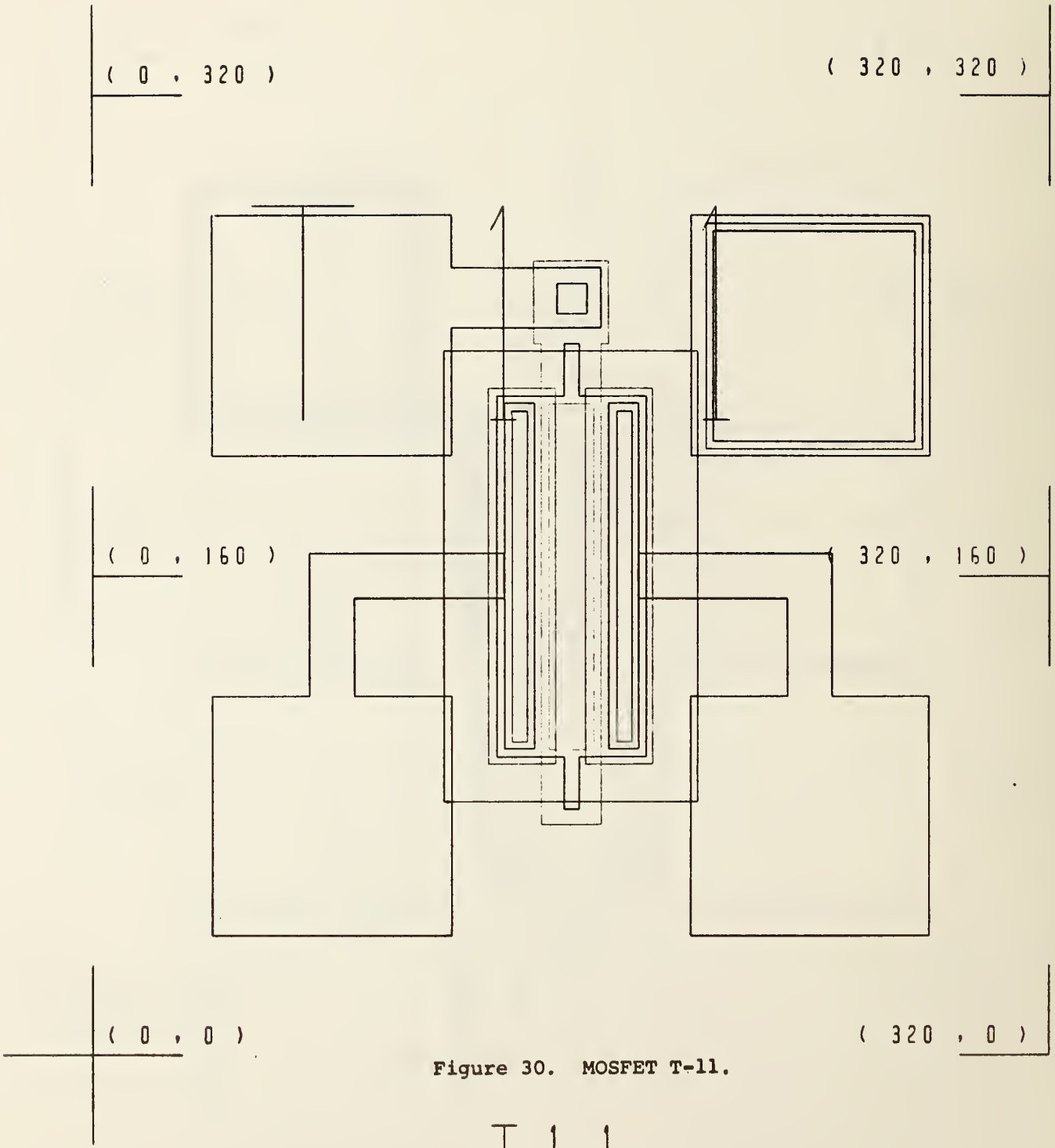


Figure 30. MOSFET T-11.

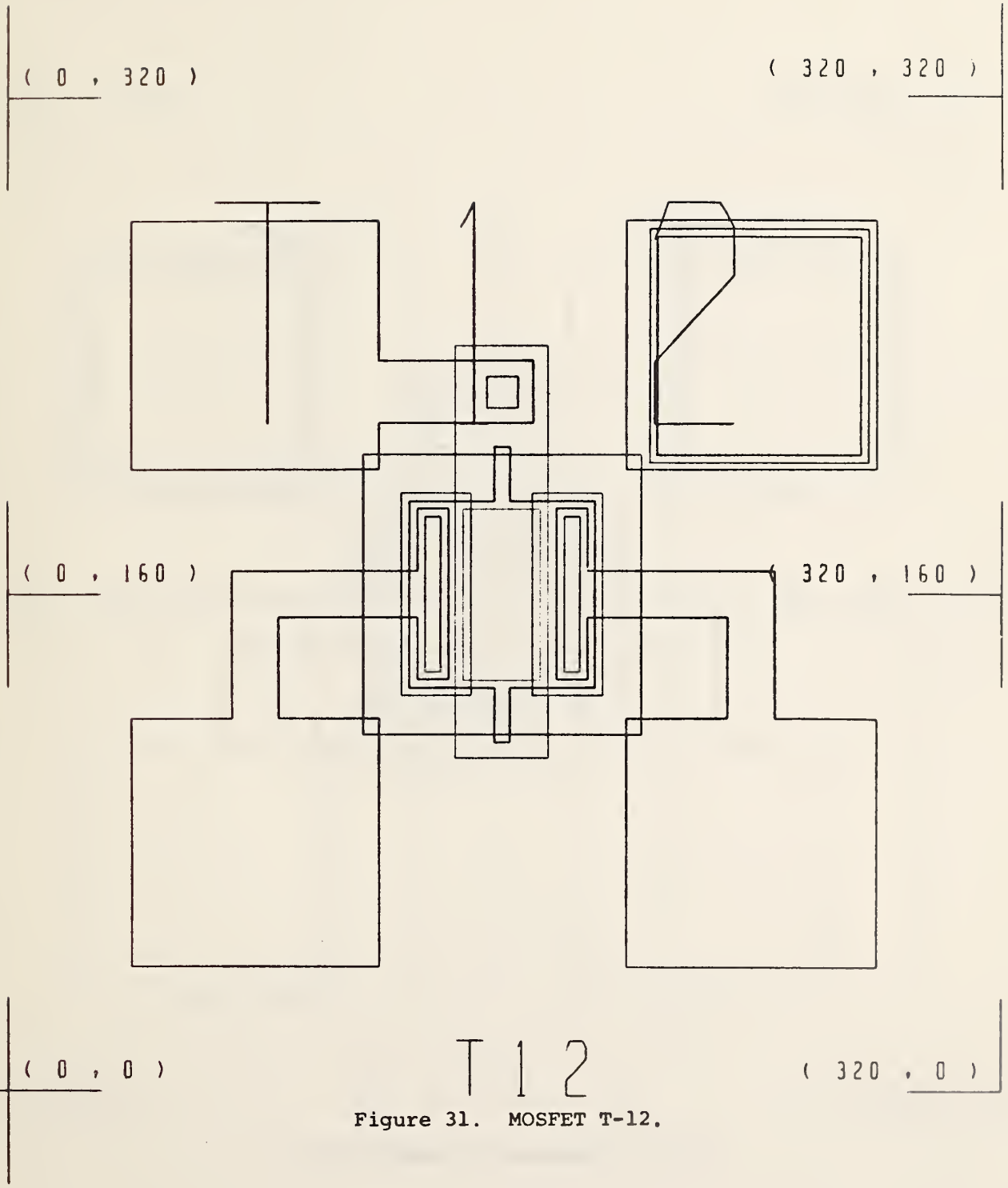


Figure 31. MOSFET T-12.

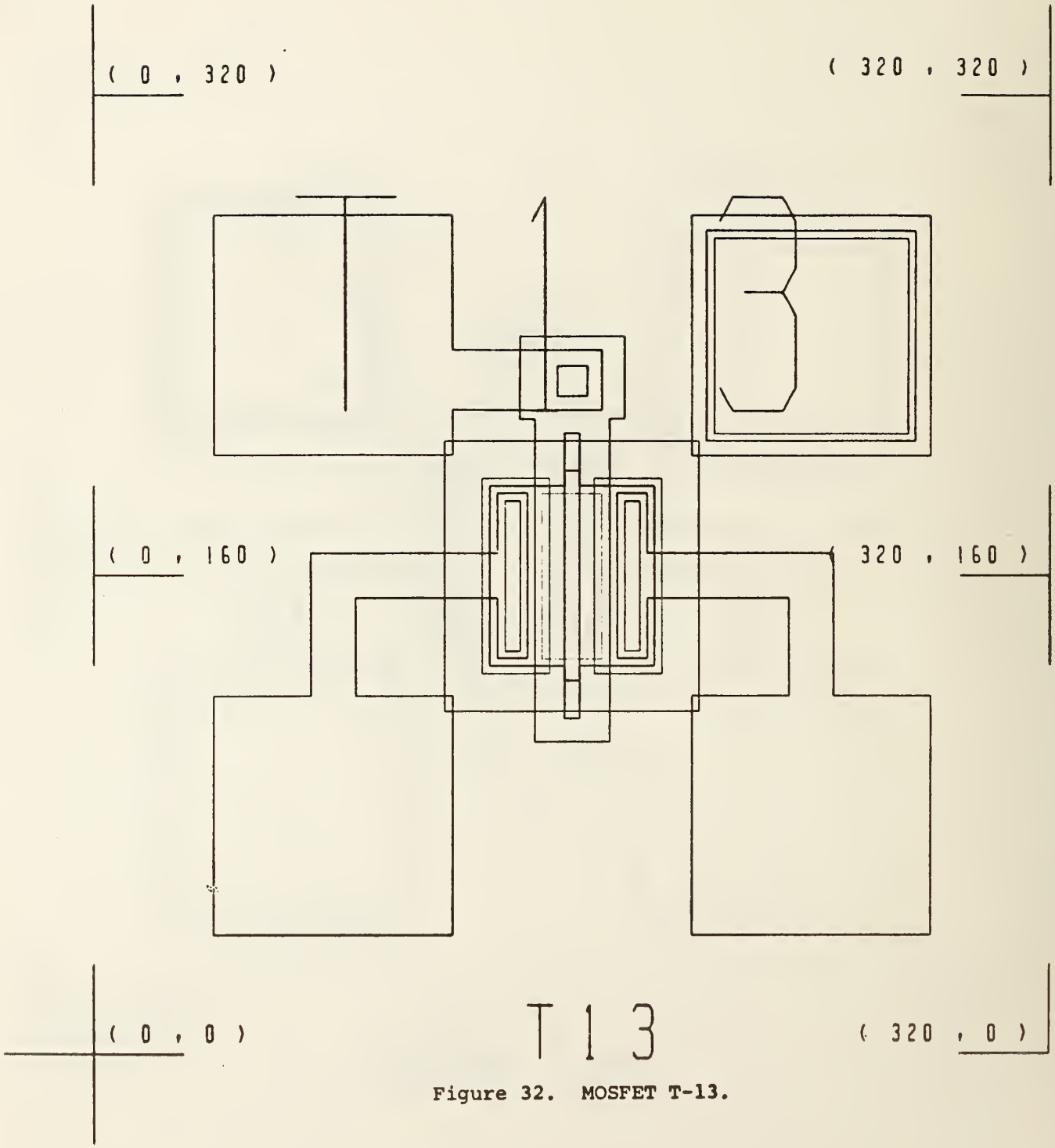


Figure 32. MOSFET T-13.

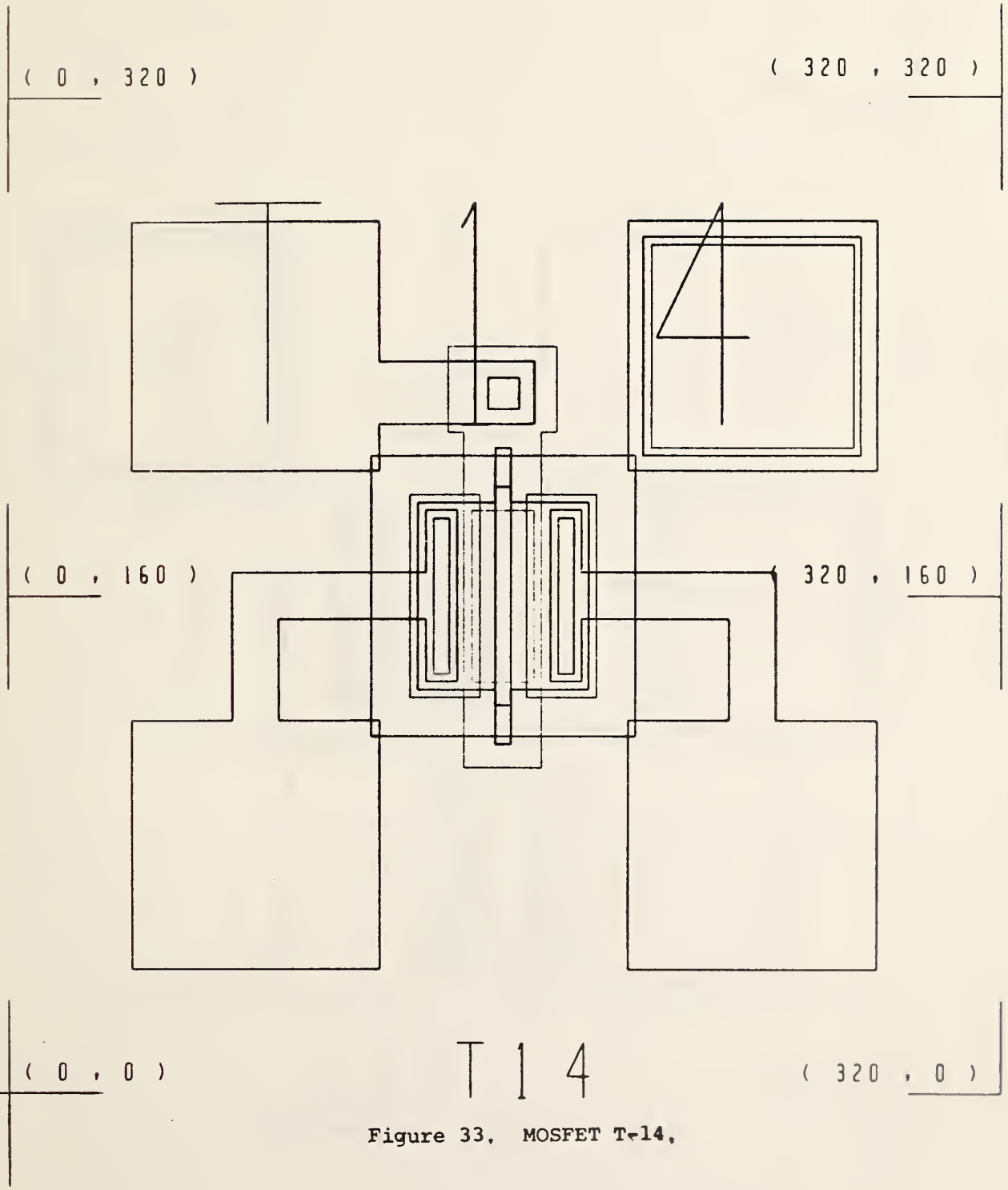


Figure 33. MOSFET T-14.

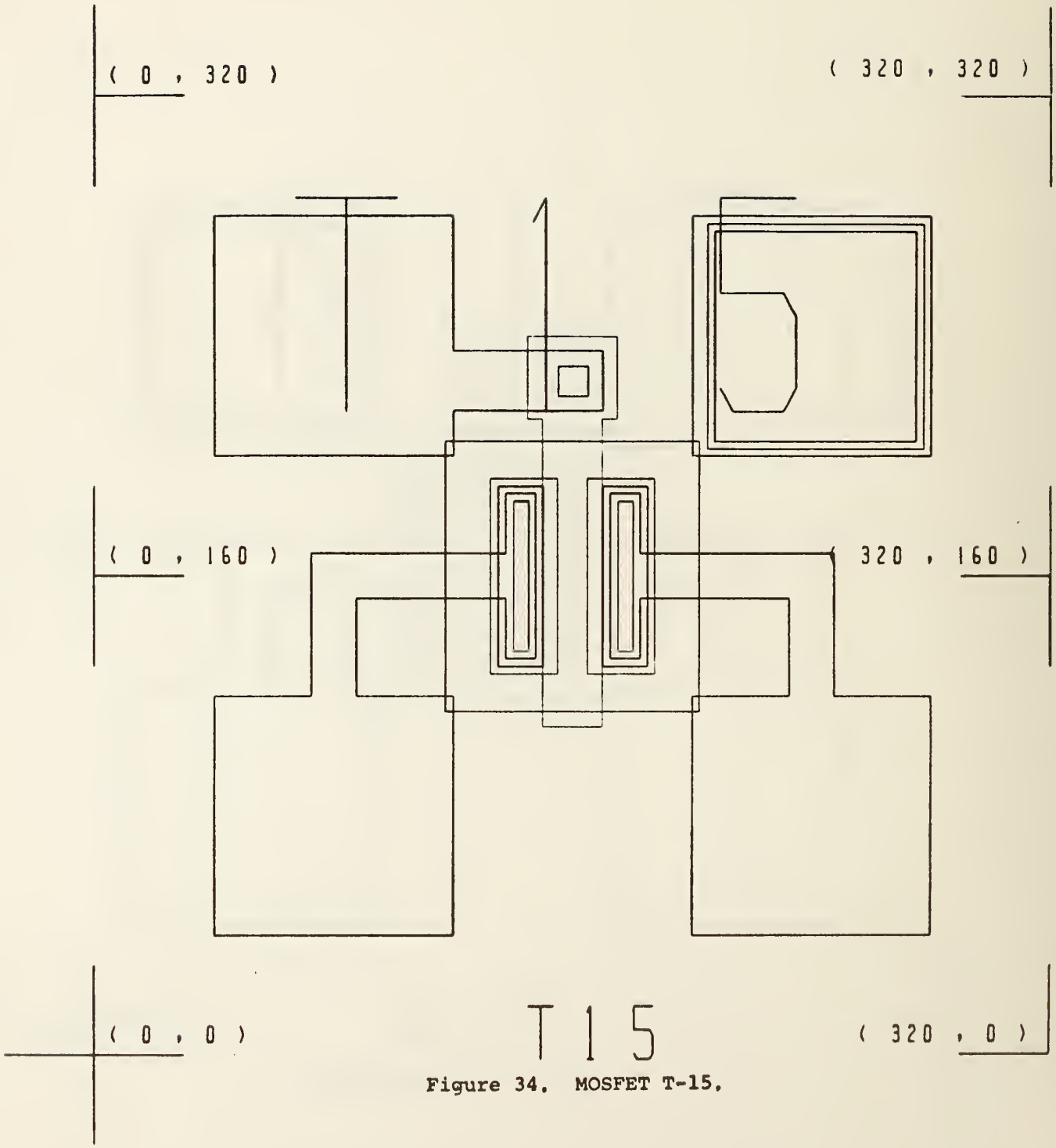


Figure 34. MOSFET T-15.

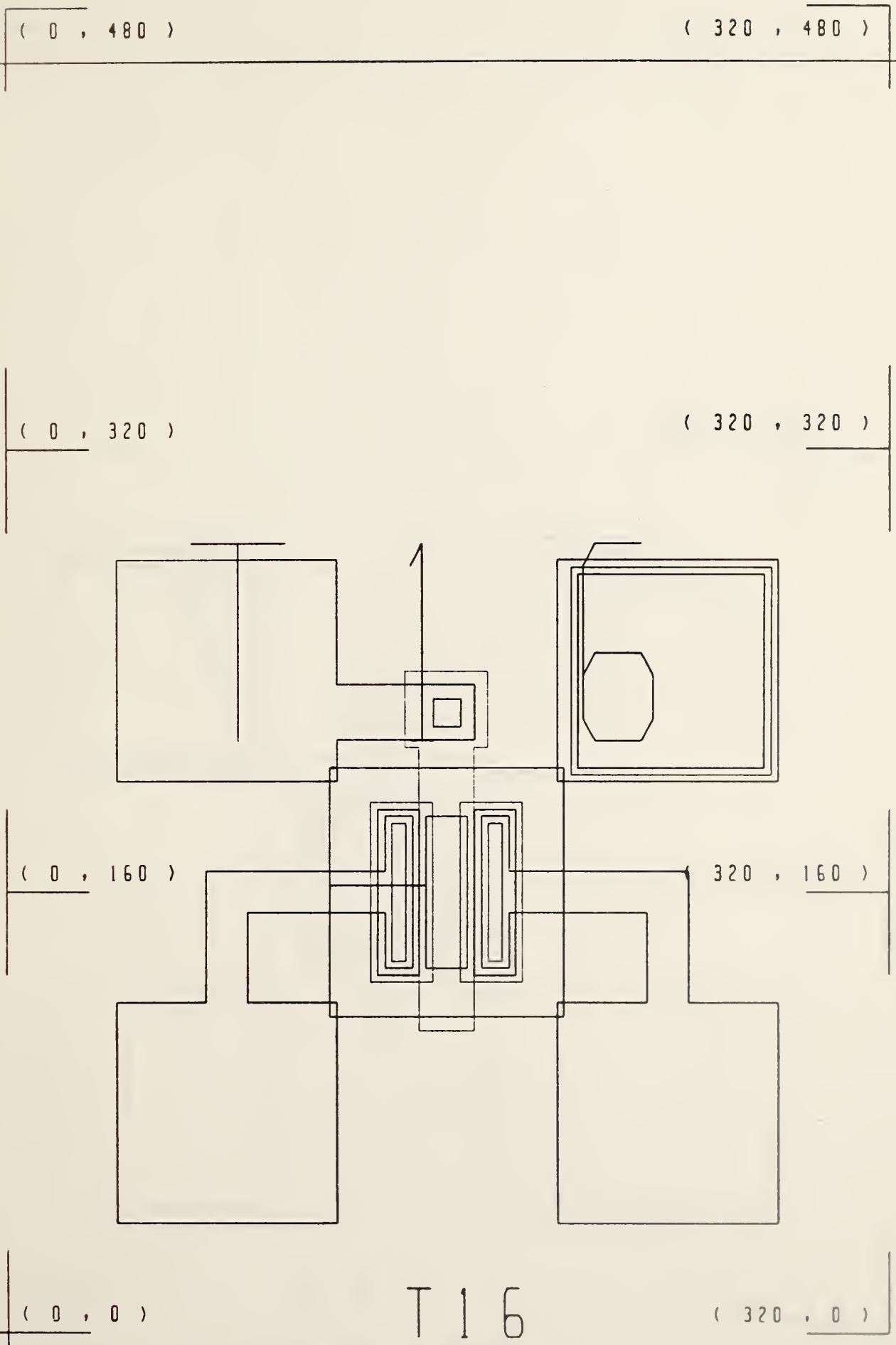


Figure 35. MOSFET T-16.

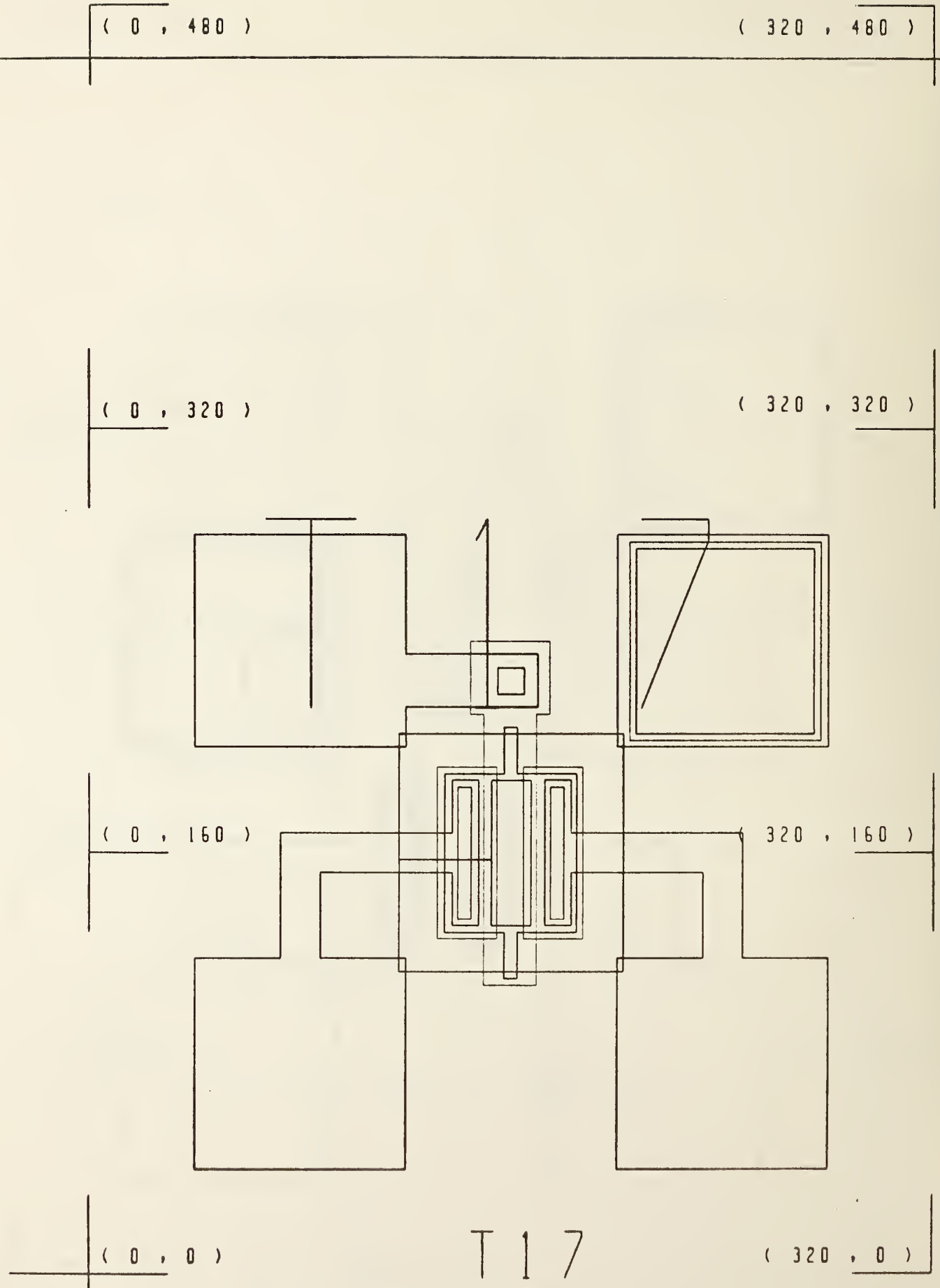


Figure 36. MOSFET T-17.

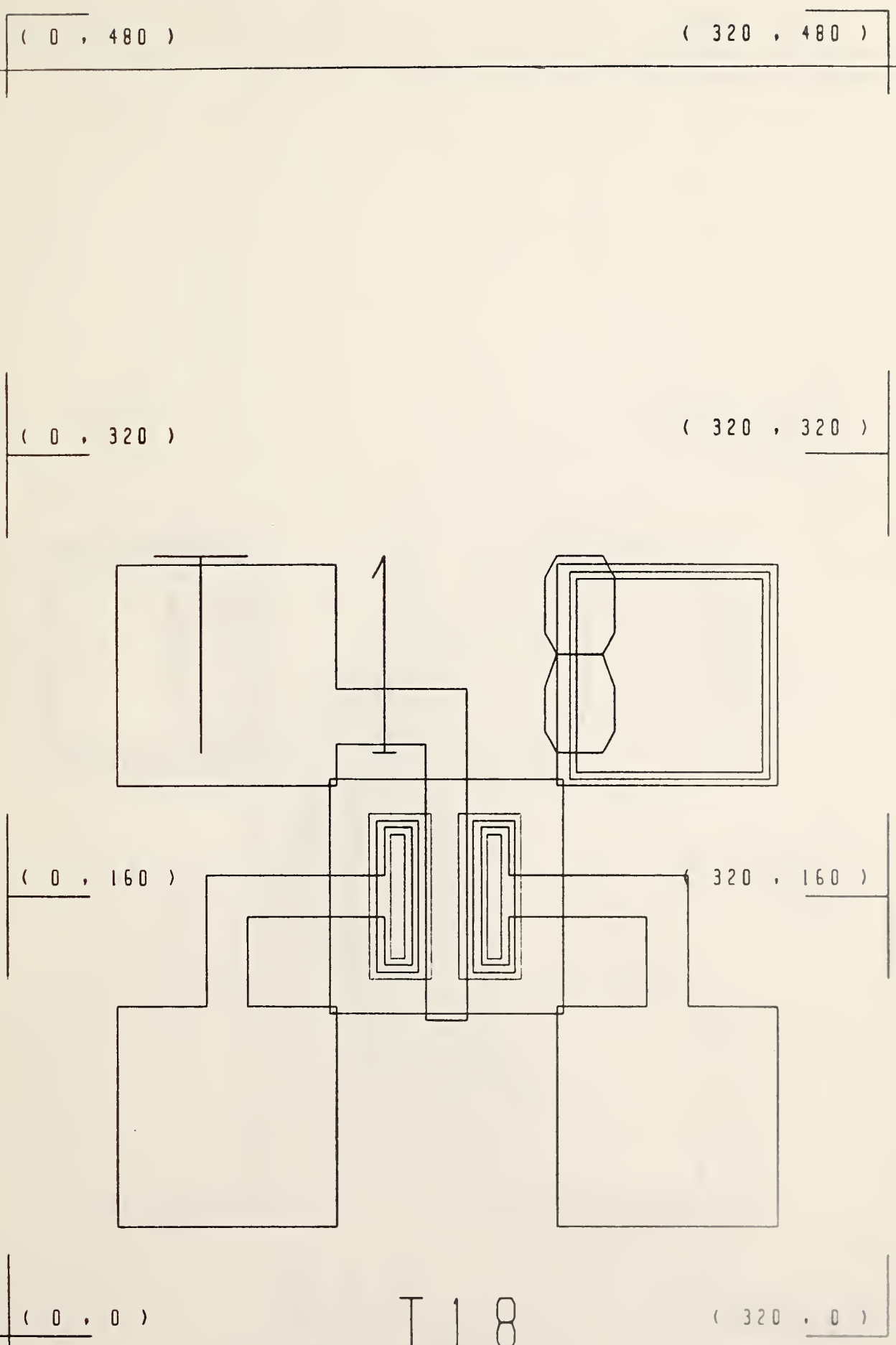


Figure 37. MOSFET T-18.

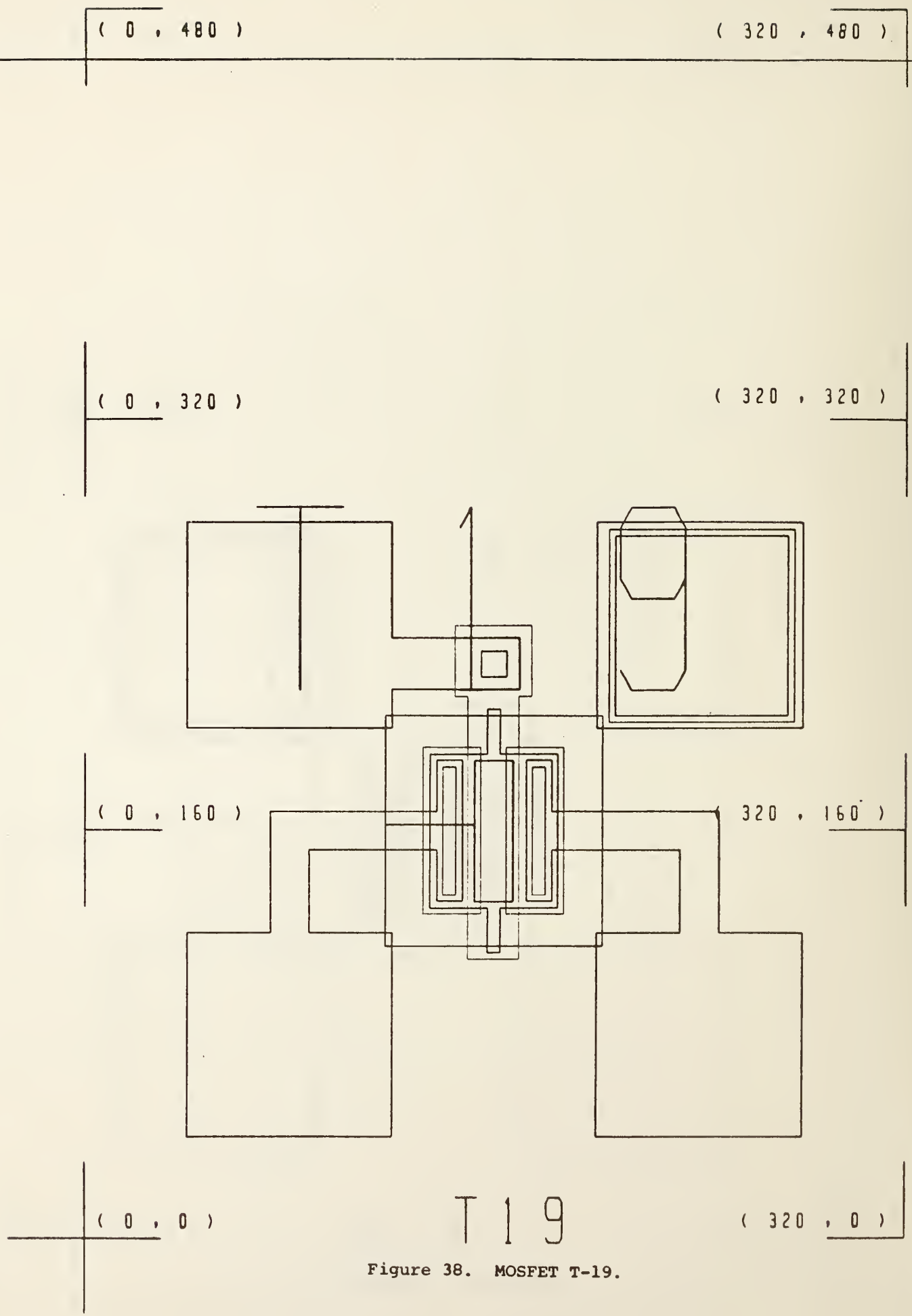
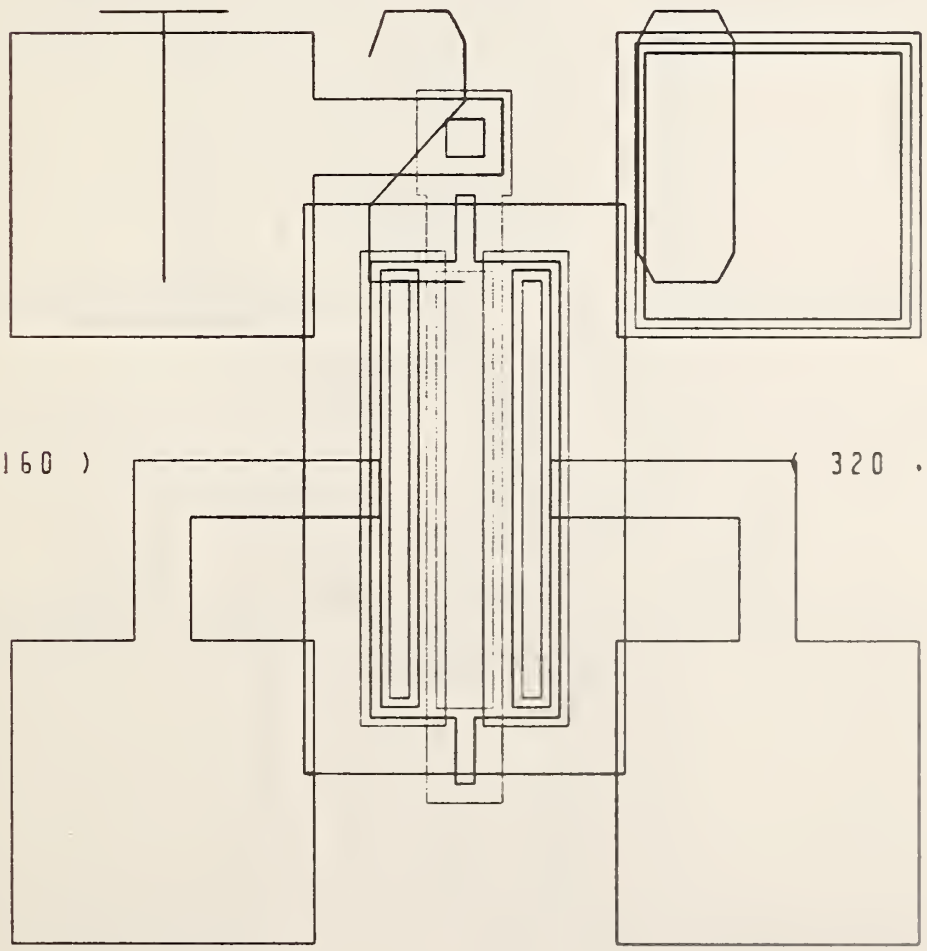


Figure 38. MOSFET T-19.

(0 , 480) (320 , 480)

(0 , 320) (320 , 320)



(0 , 160) (320 , 160)

(0 , 0) (320 , 0)

Figure 39. MOSFET T-20.

T 2 0

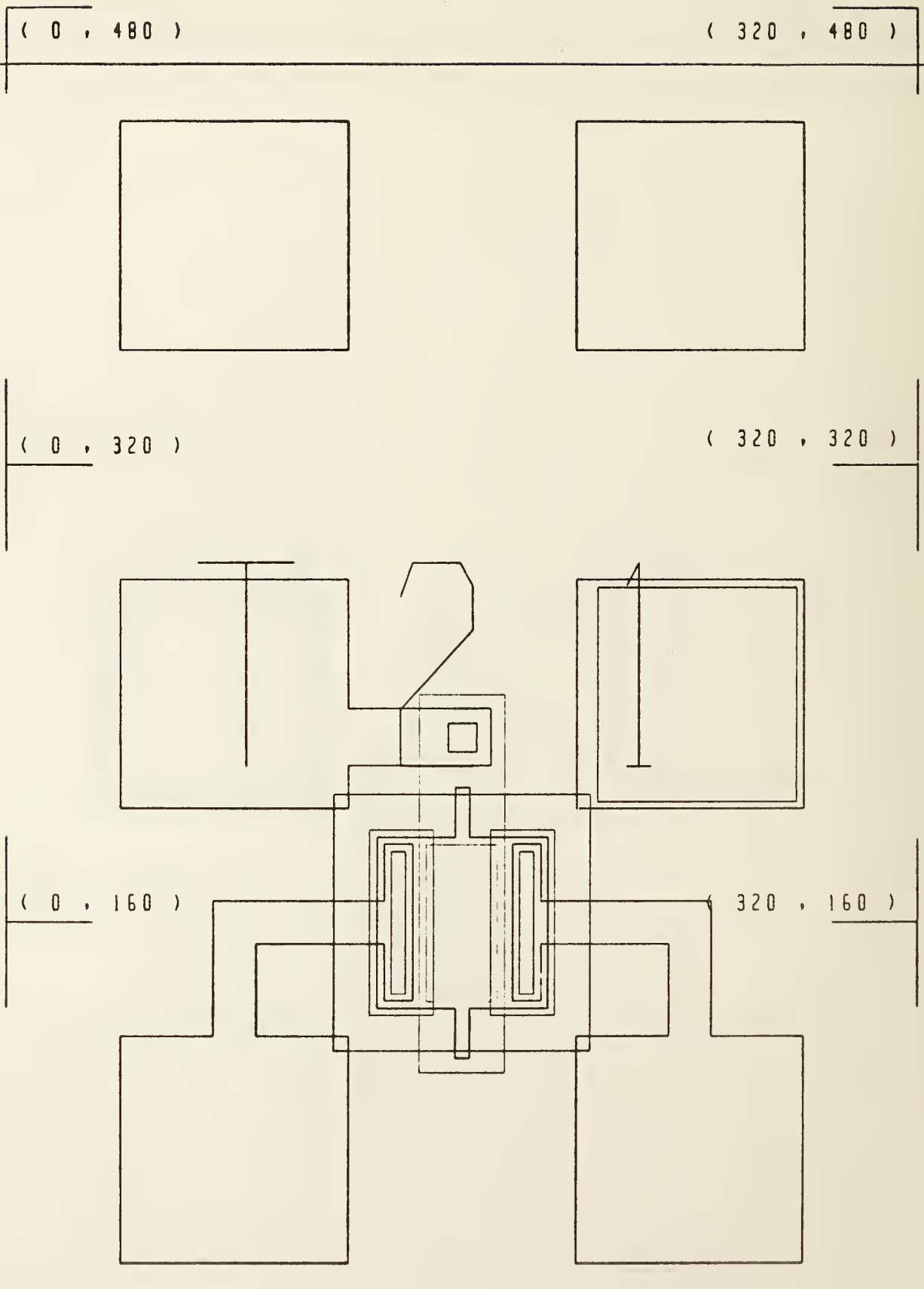


Figure 40. MOSFET T-21.

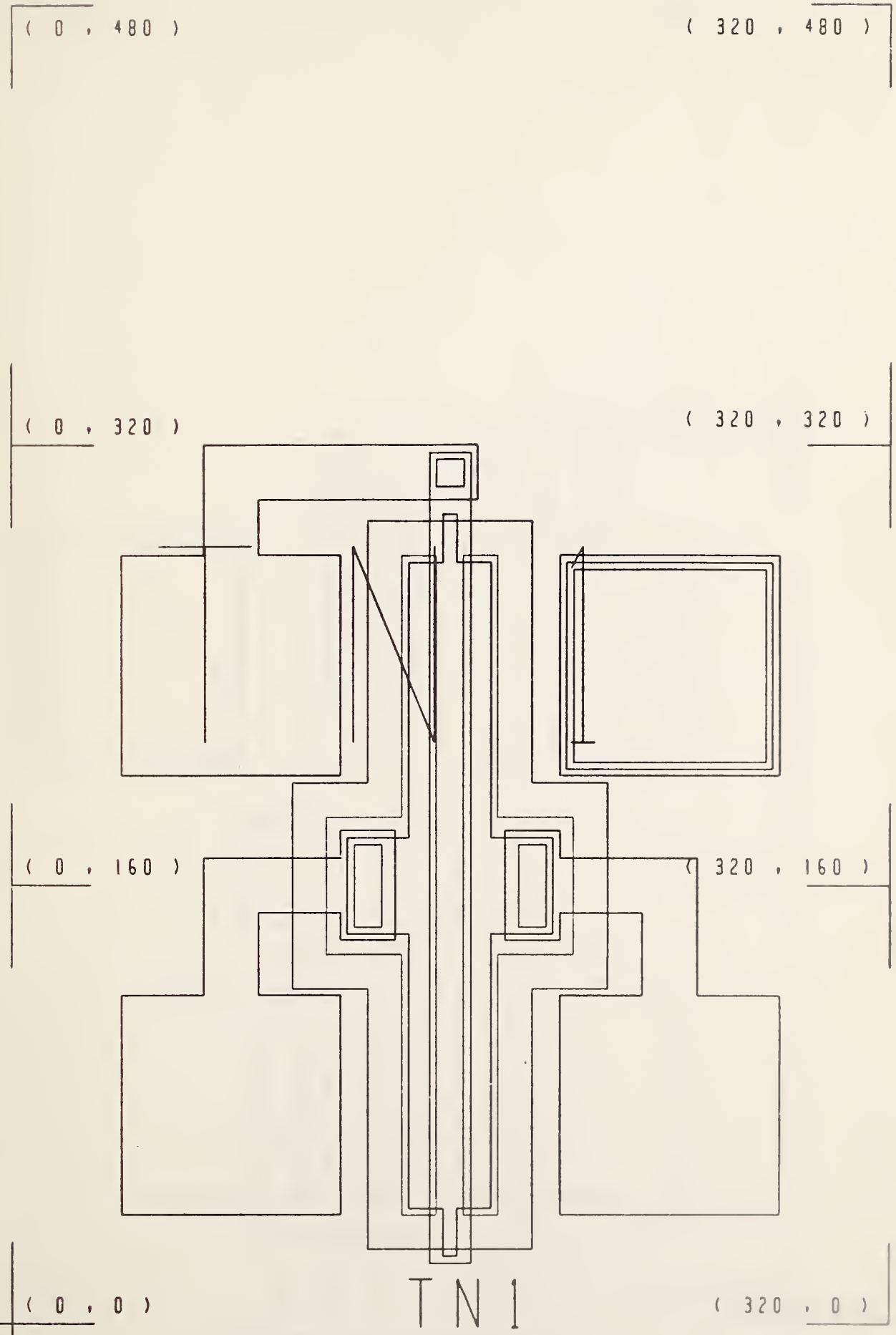


Figure 41. MOSFET TN-1.

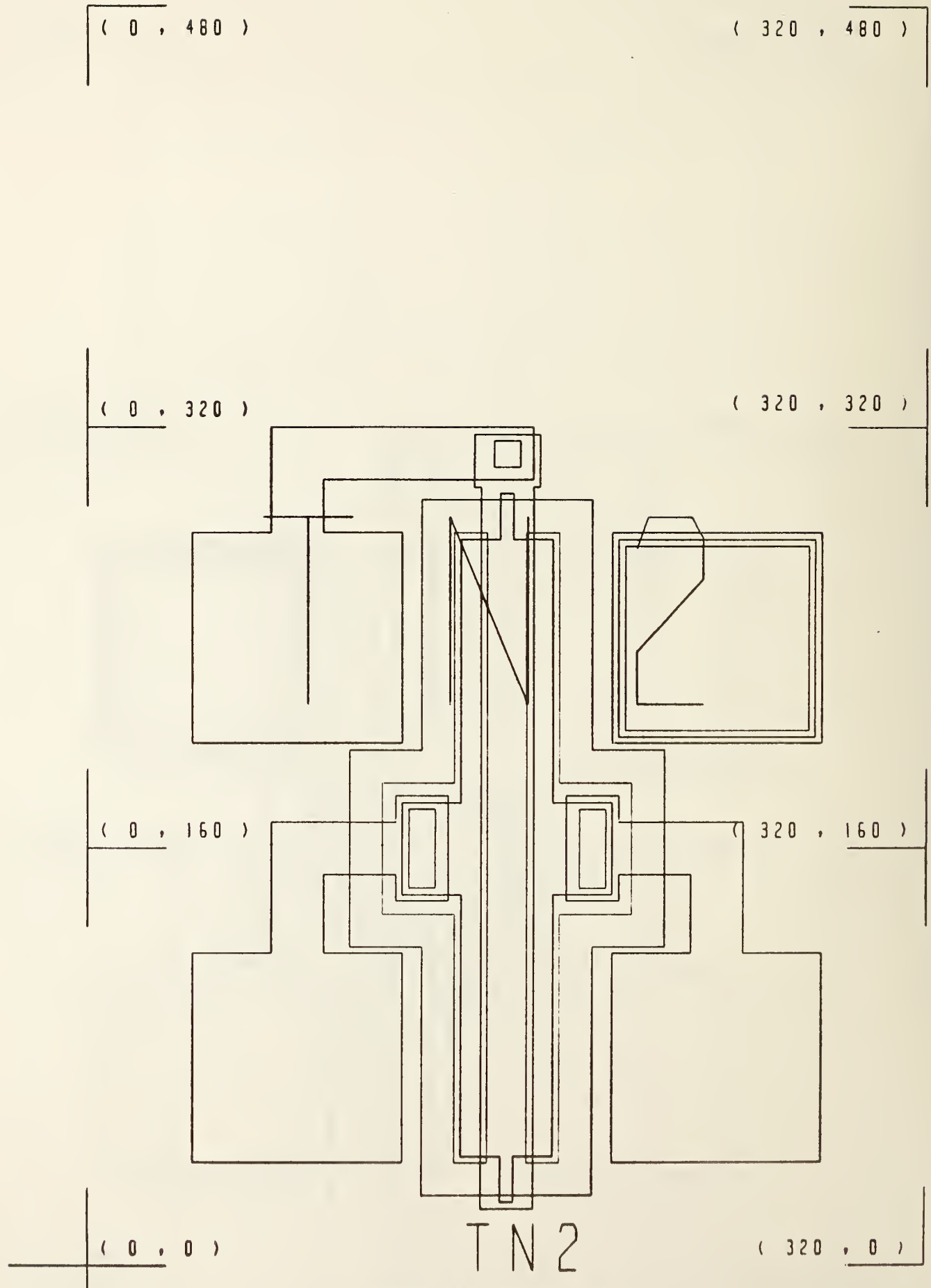


Figure 42. MOSFET TN-2.

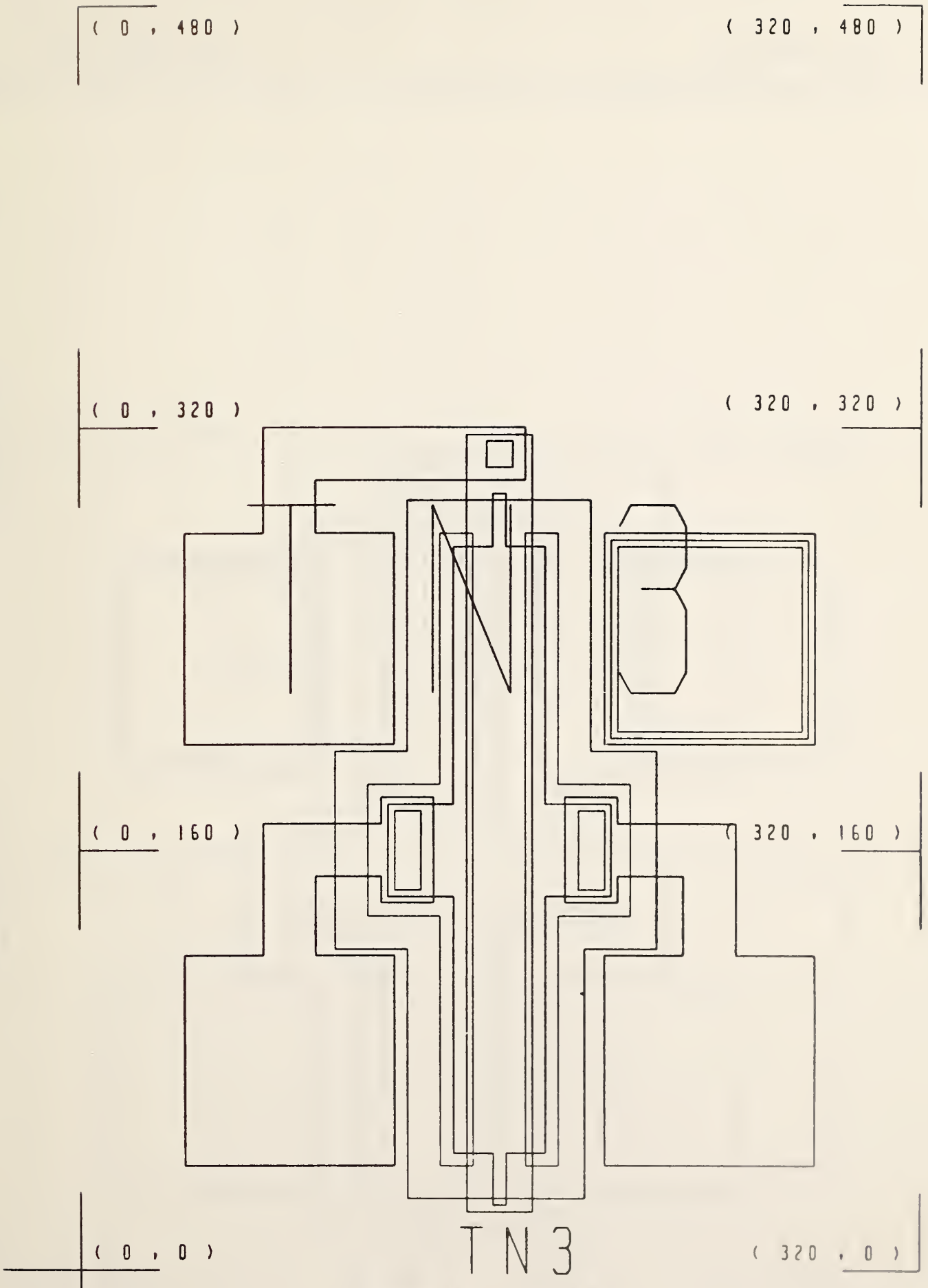


Figure 43. MOSFET TN-3.

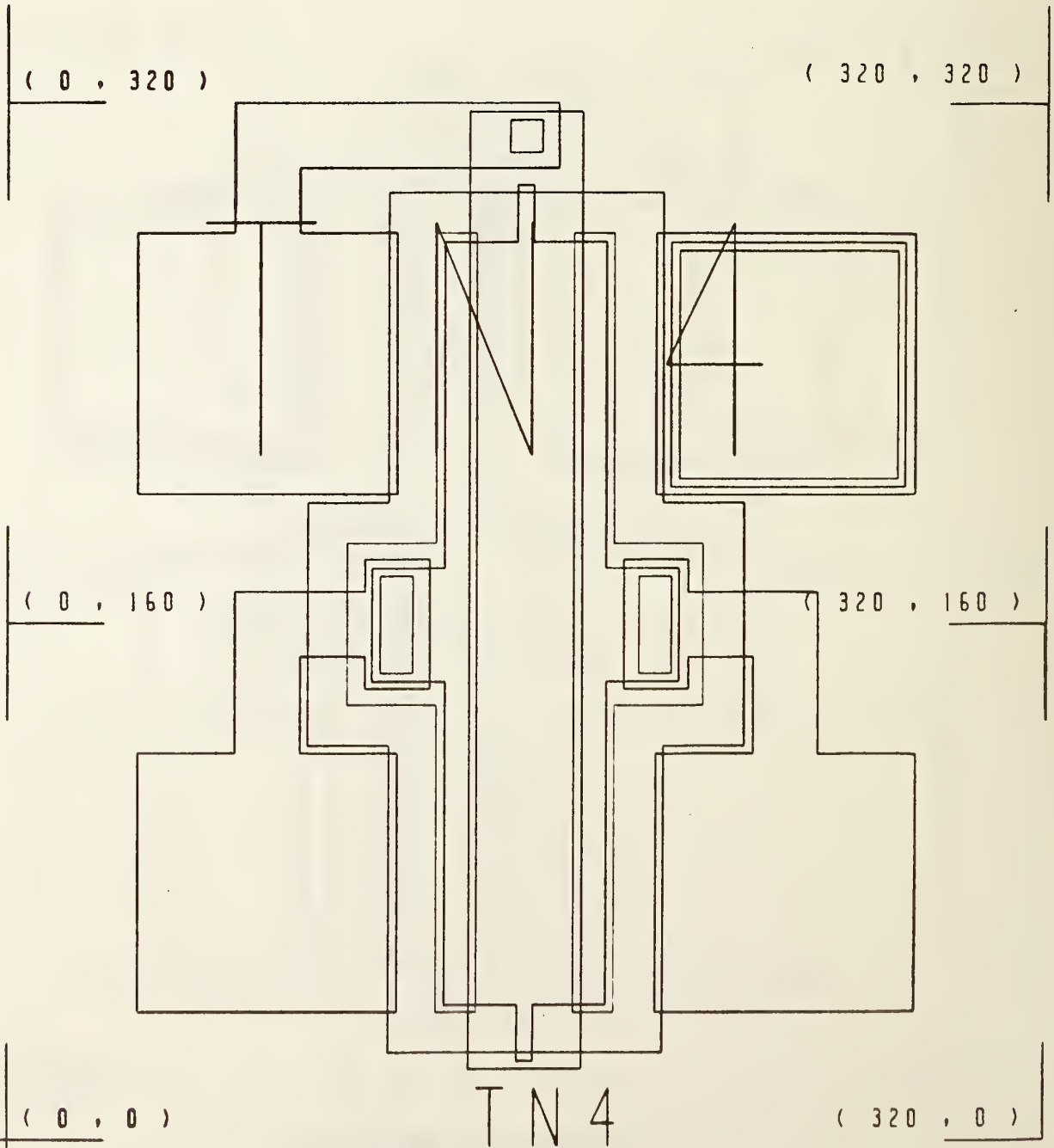


Figure 44. MOSFET TN-4.

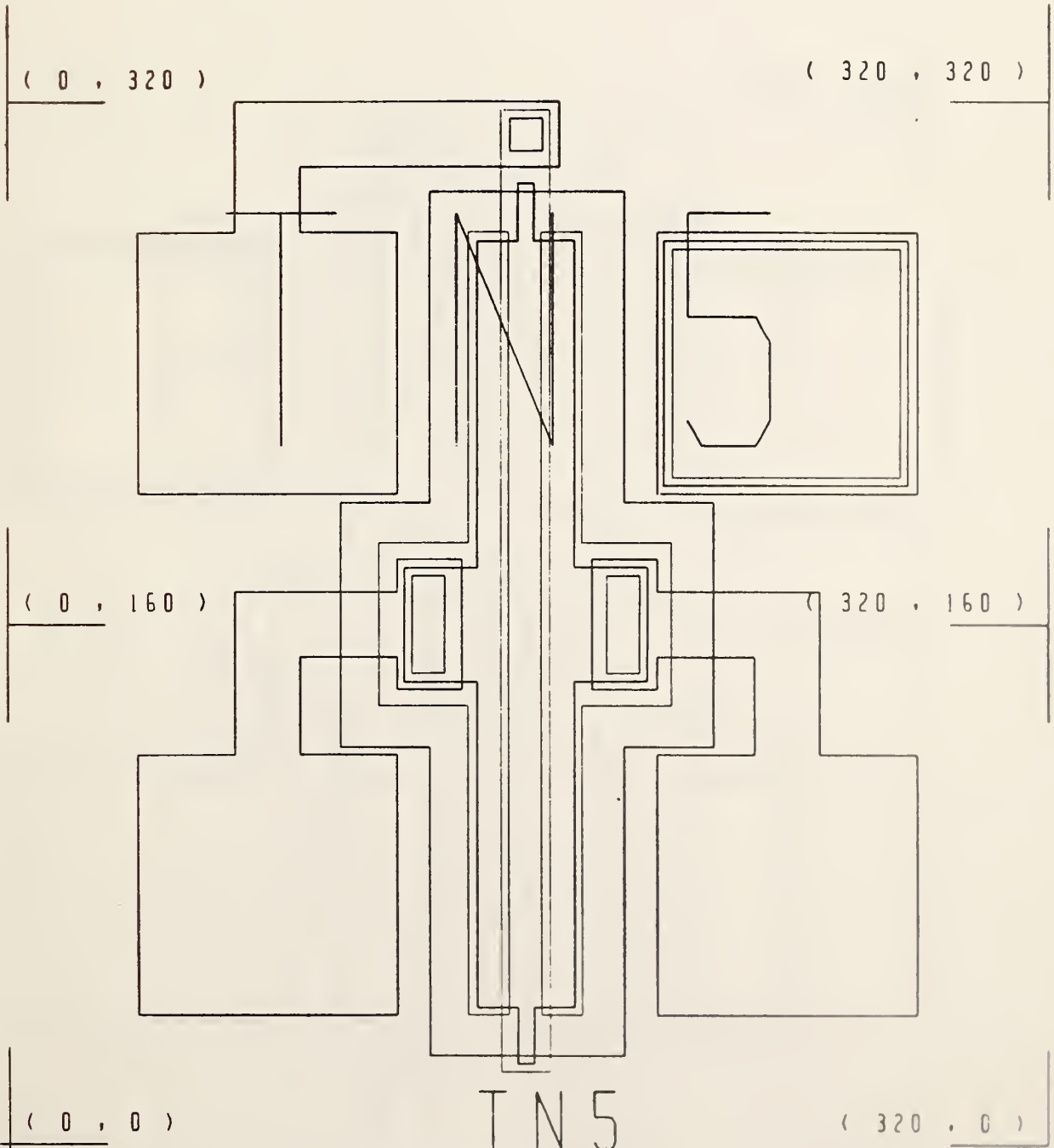


Figure 45. MOSFET TN-5.

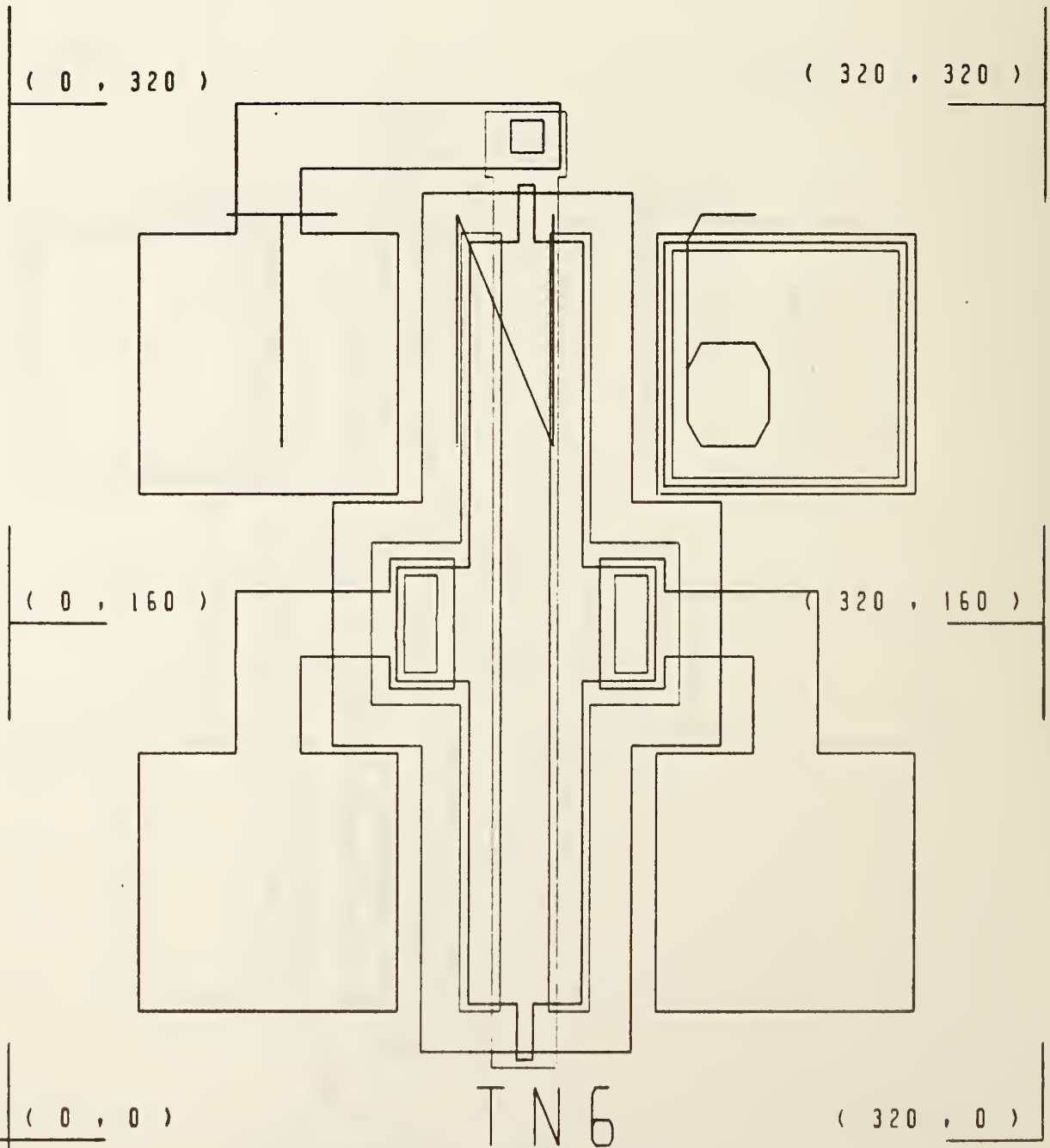


Figure 46. MOSFET TN-6.

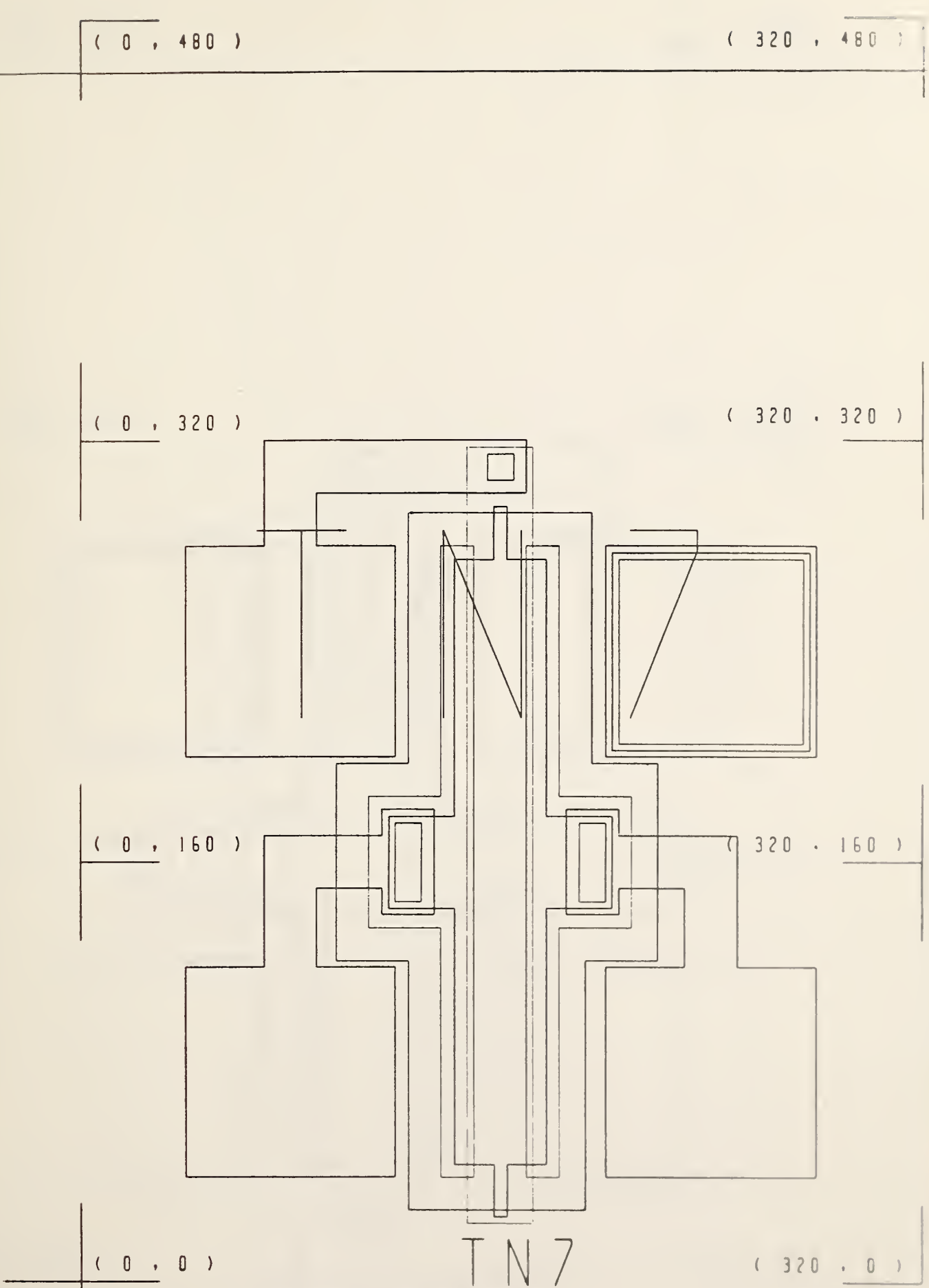


Figure 47. MOSFET TN-7.

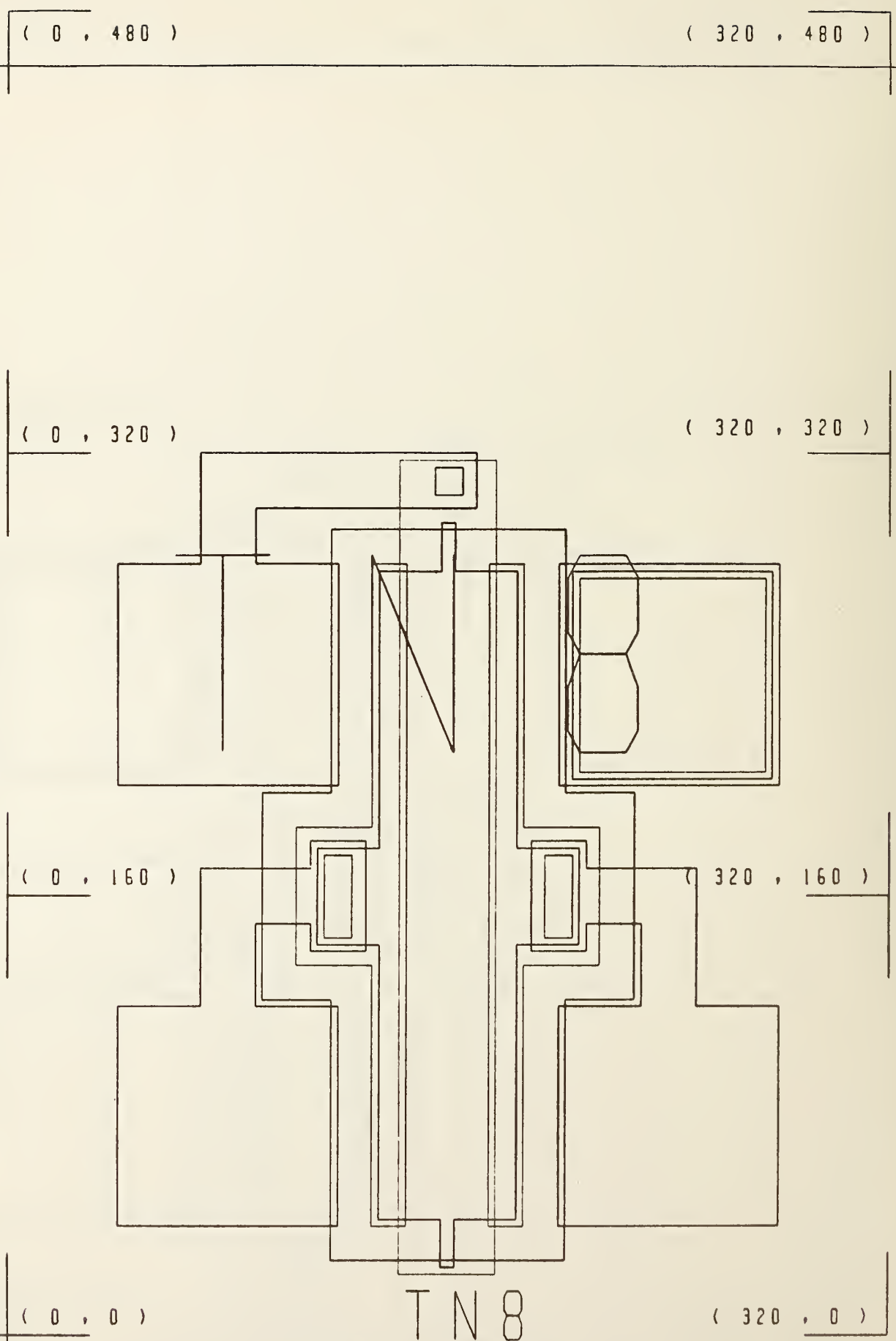


Figure 48. MOSFET TN-8.

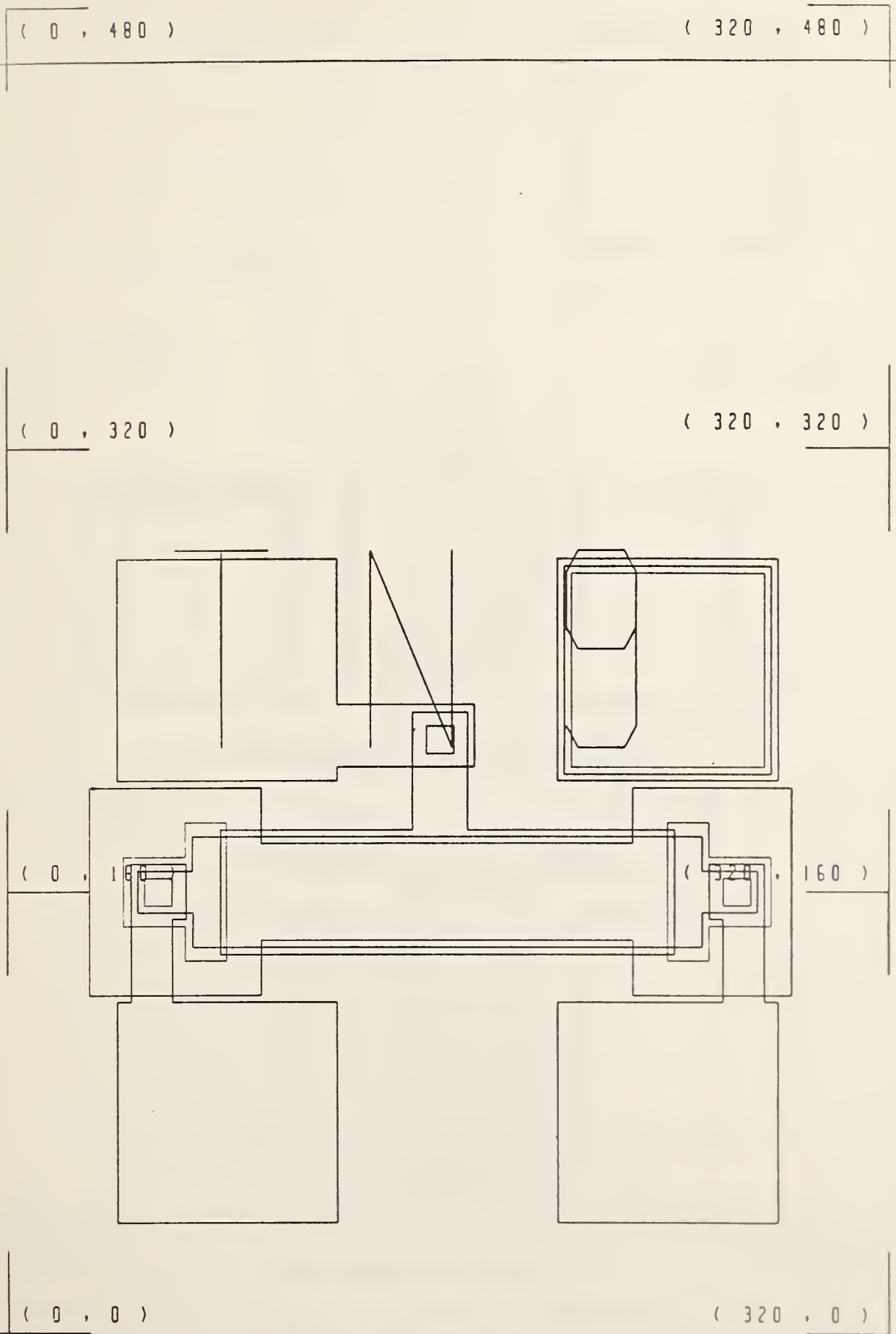


Figure 49. MOSFET TN-9.

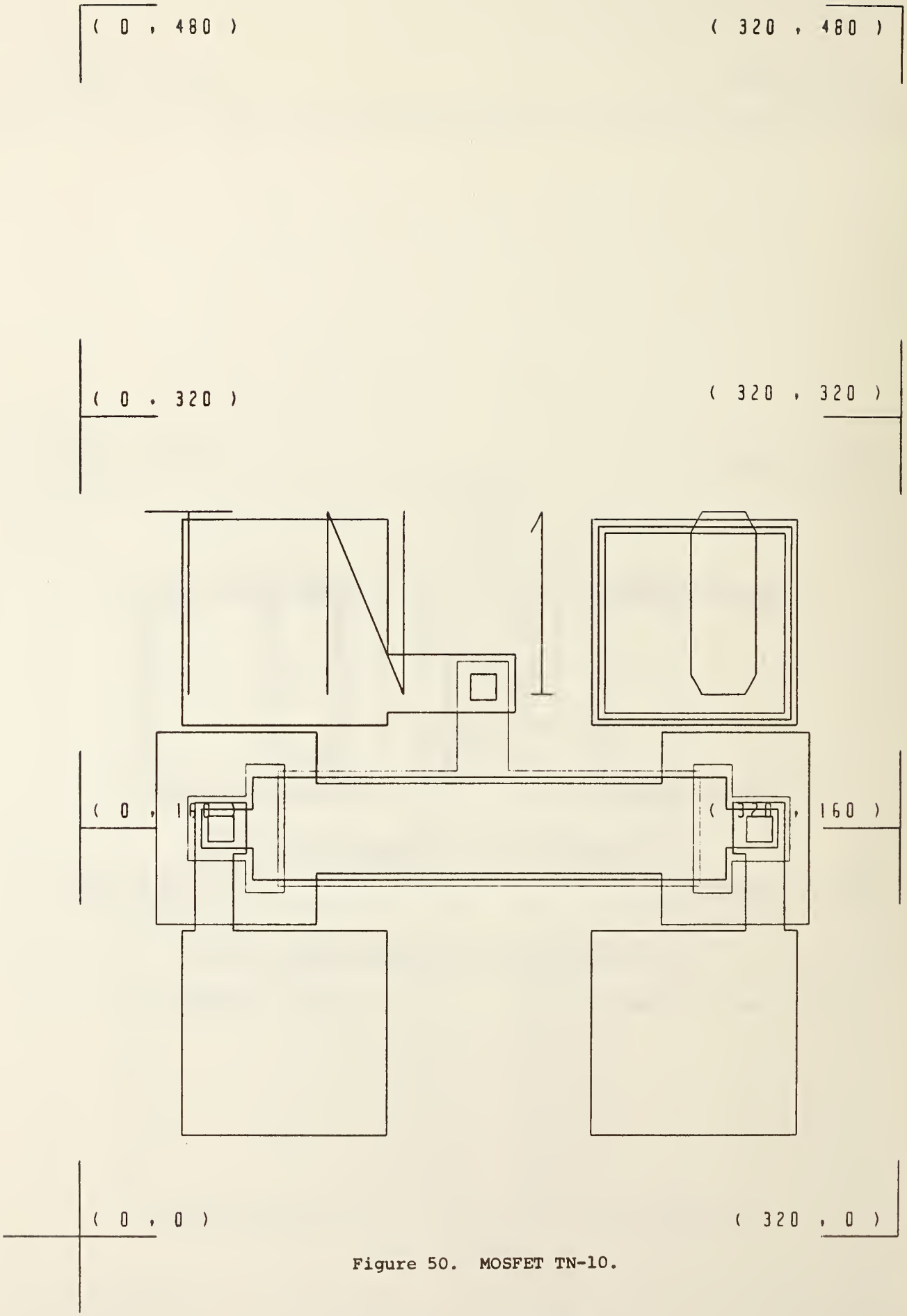


Figure 50. MOSFET TN-10.

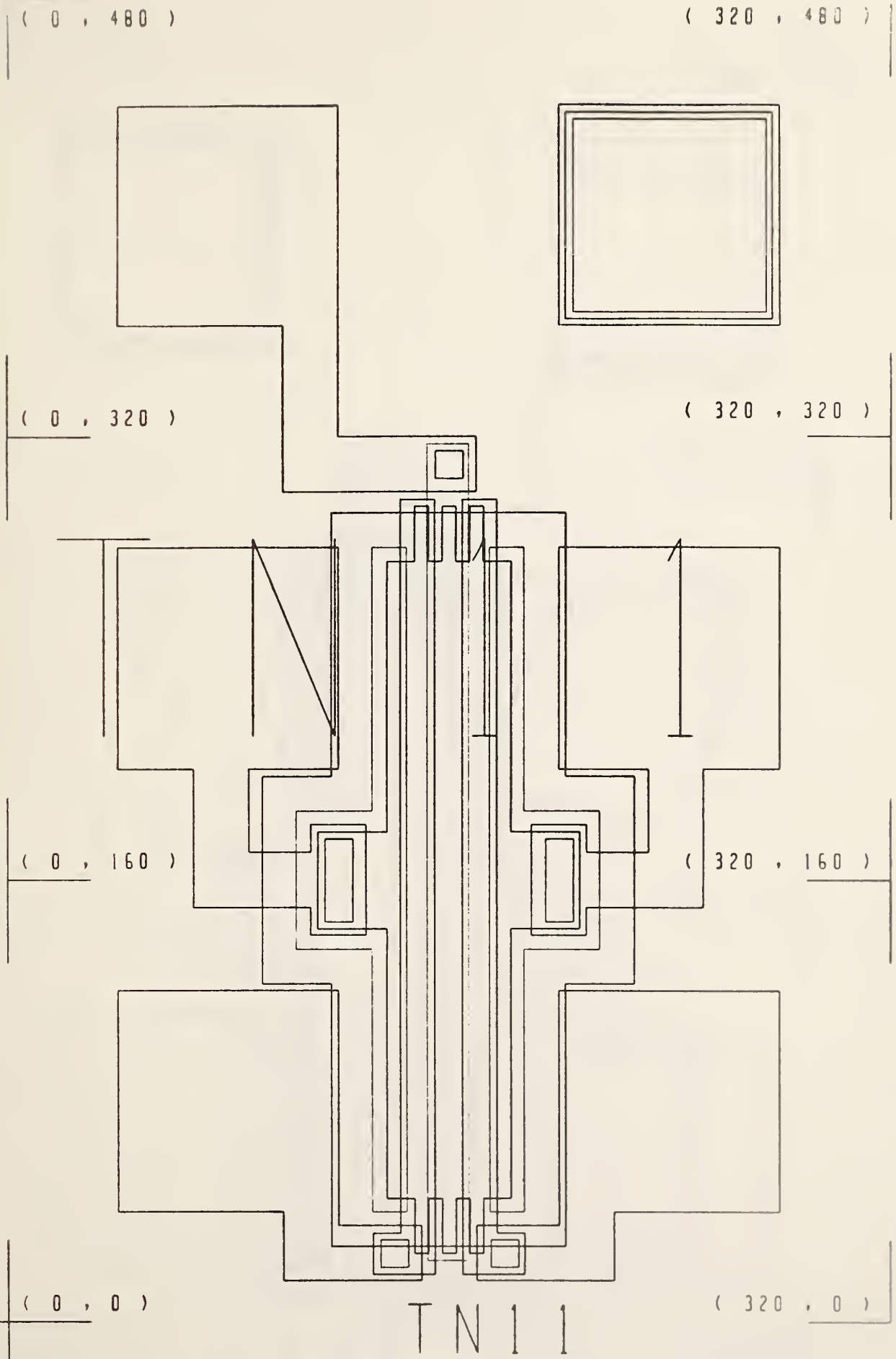


Figure 51. Triple-Gate MOSFET TN-11.

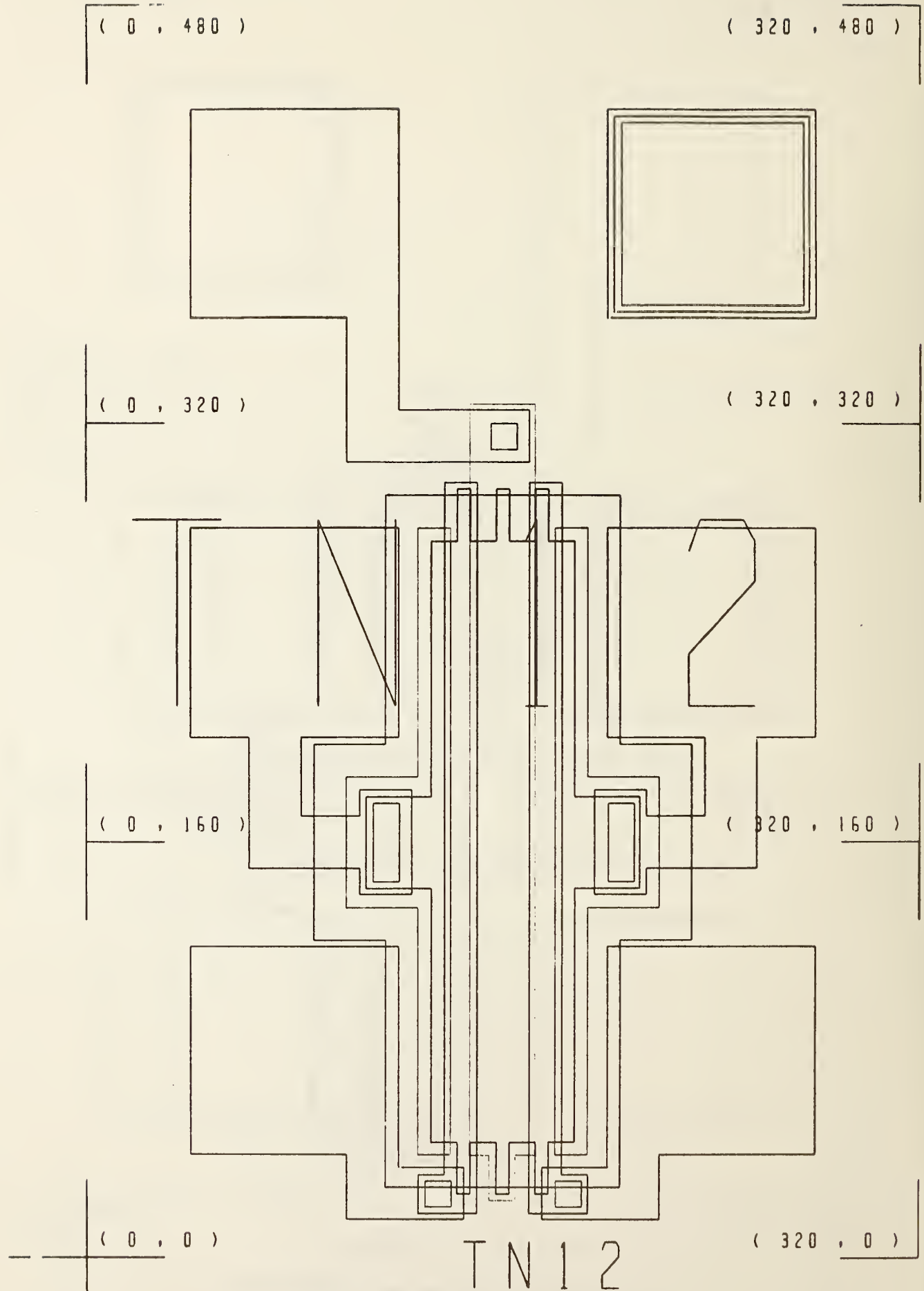


Figure 52. Triple-Gate MOSFET TN-12.

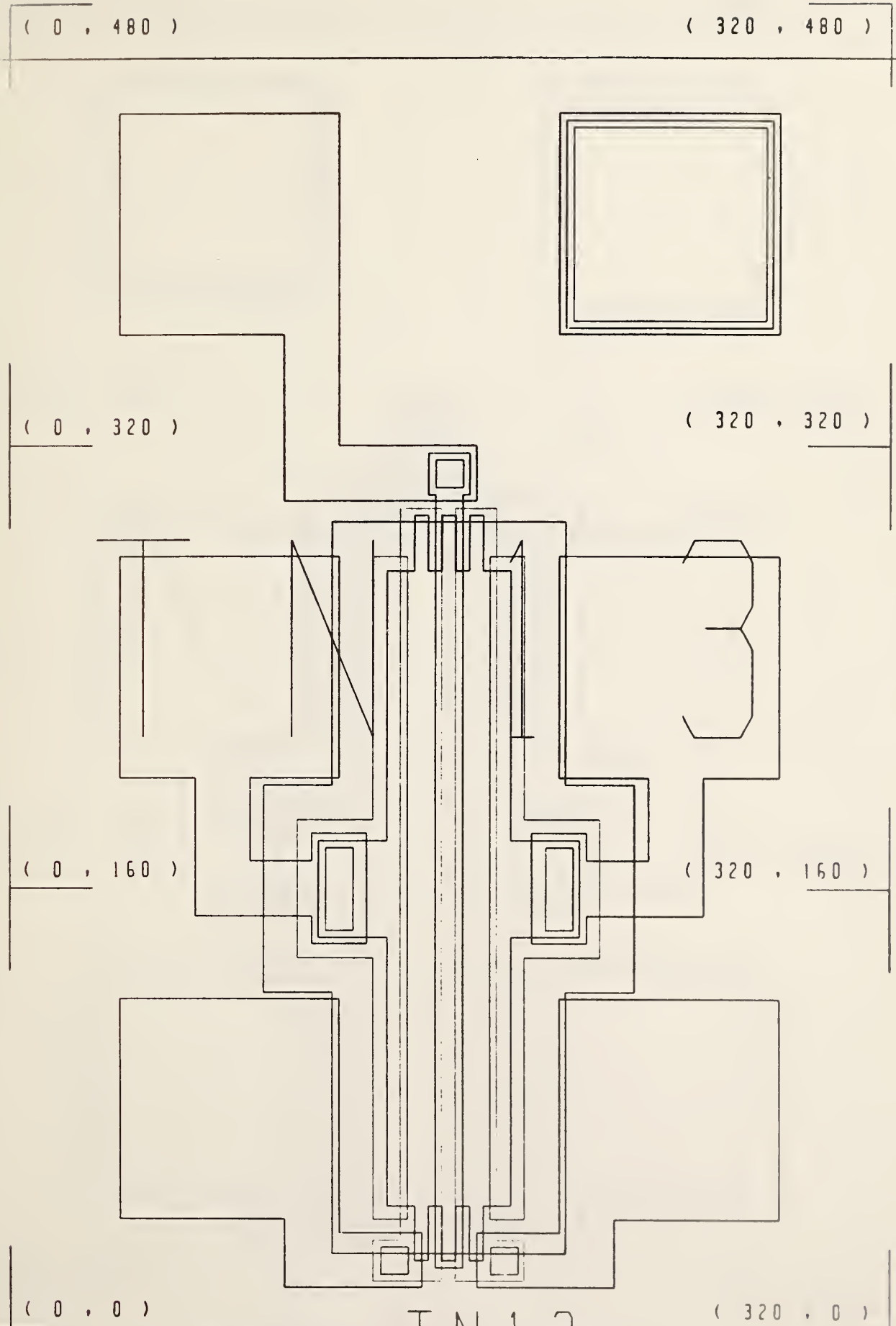


Figure 53. Triple-Gate MOSFET TN-13.

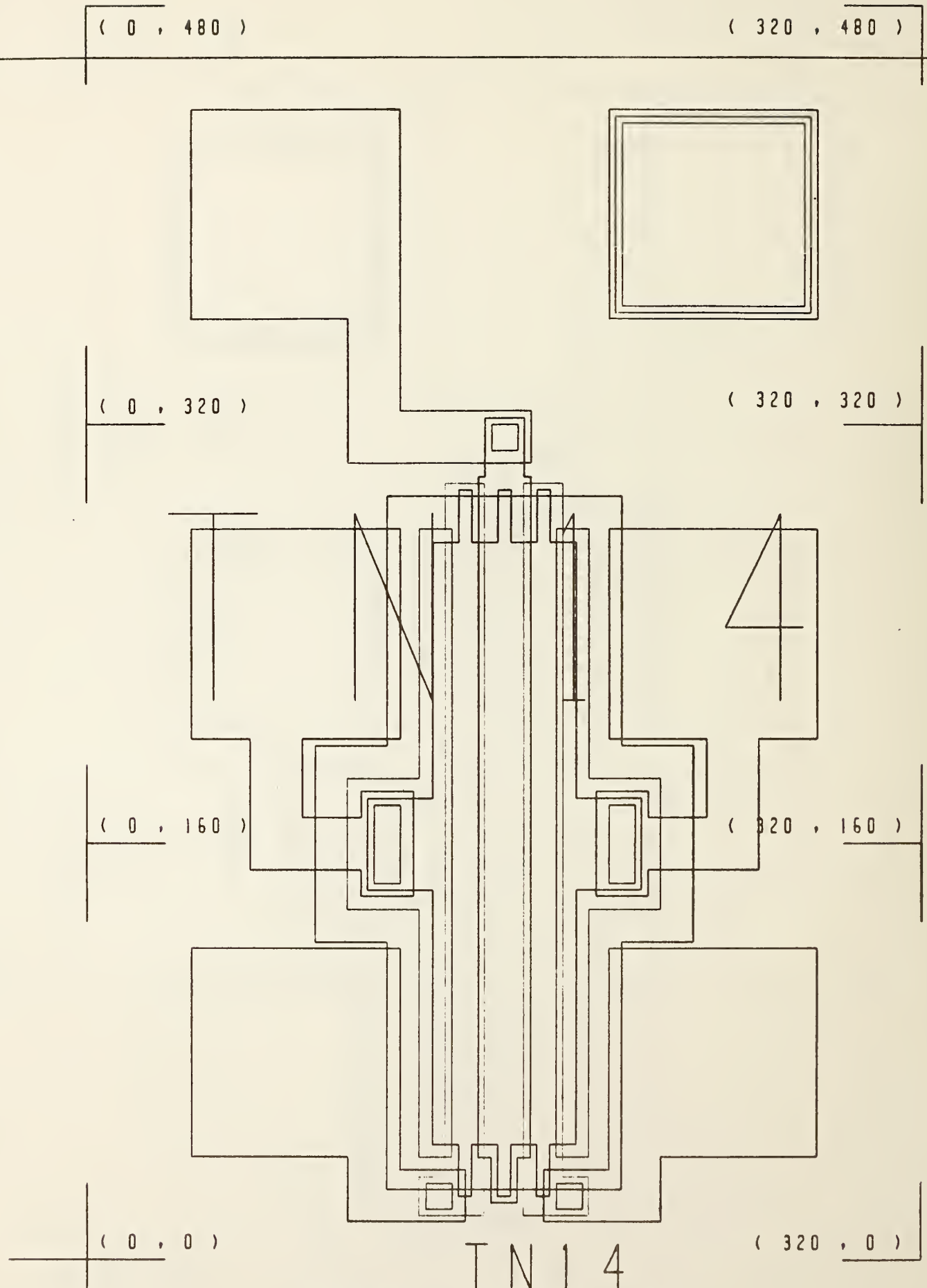


Figure 54. Triple-Gate MOSFET TN-14.

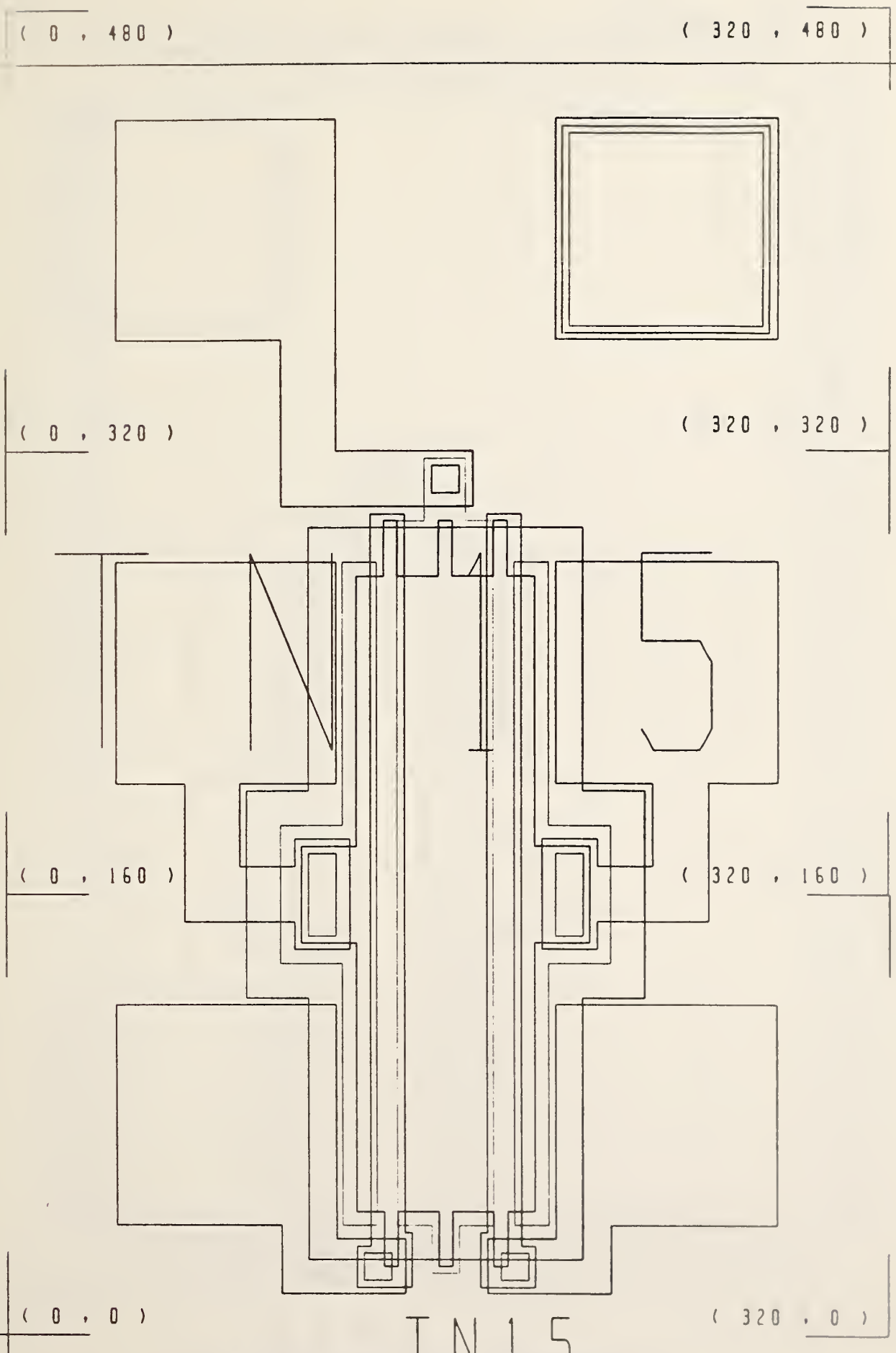


Figure 55. Triple-Gate MOSFET TN-15.

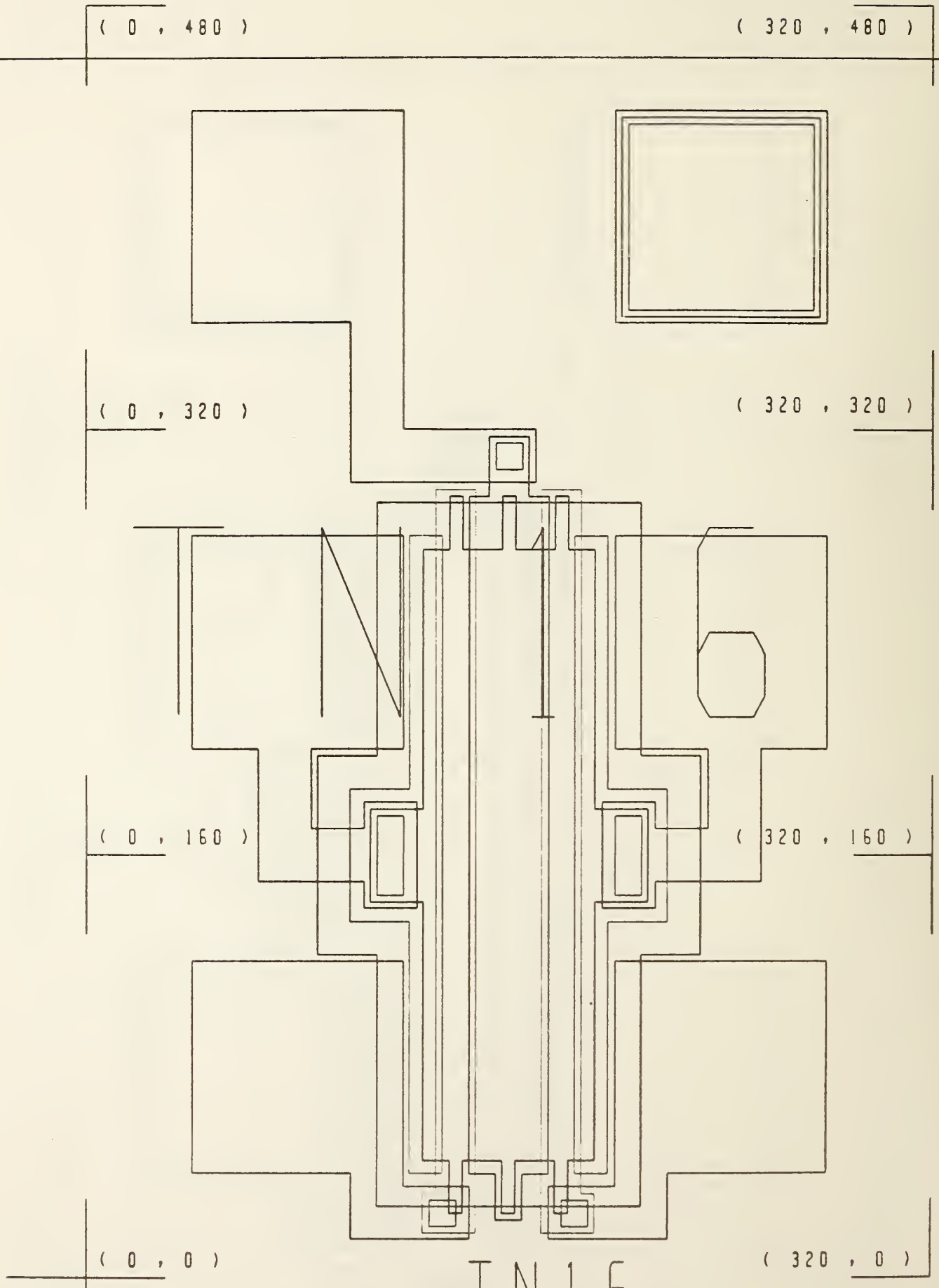


Figure 56. Triple-Gate MOSFET TN-16.

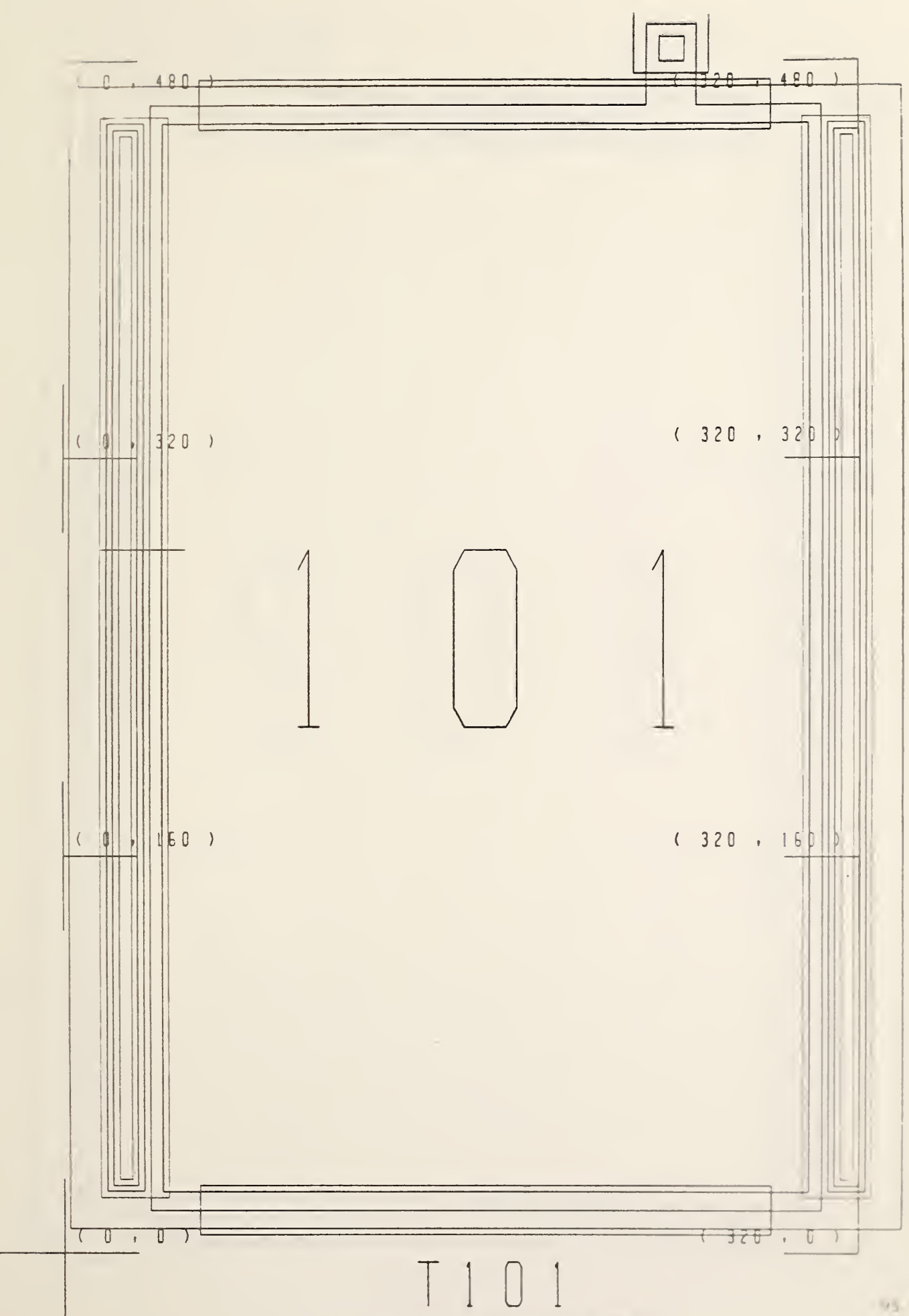


Figure 57. Capacitor/Transistor T-101.

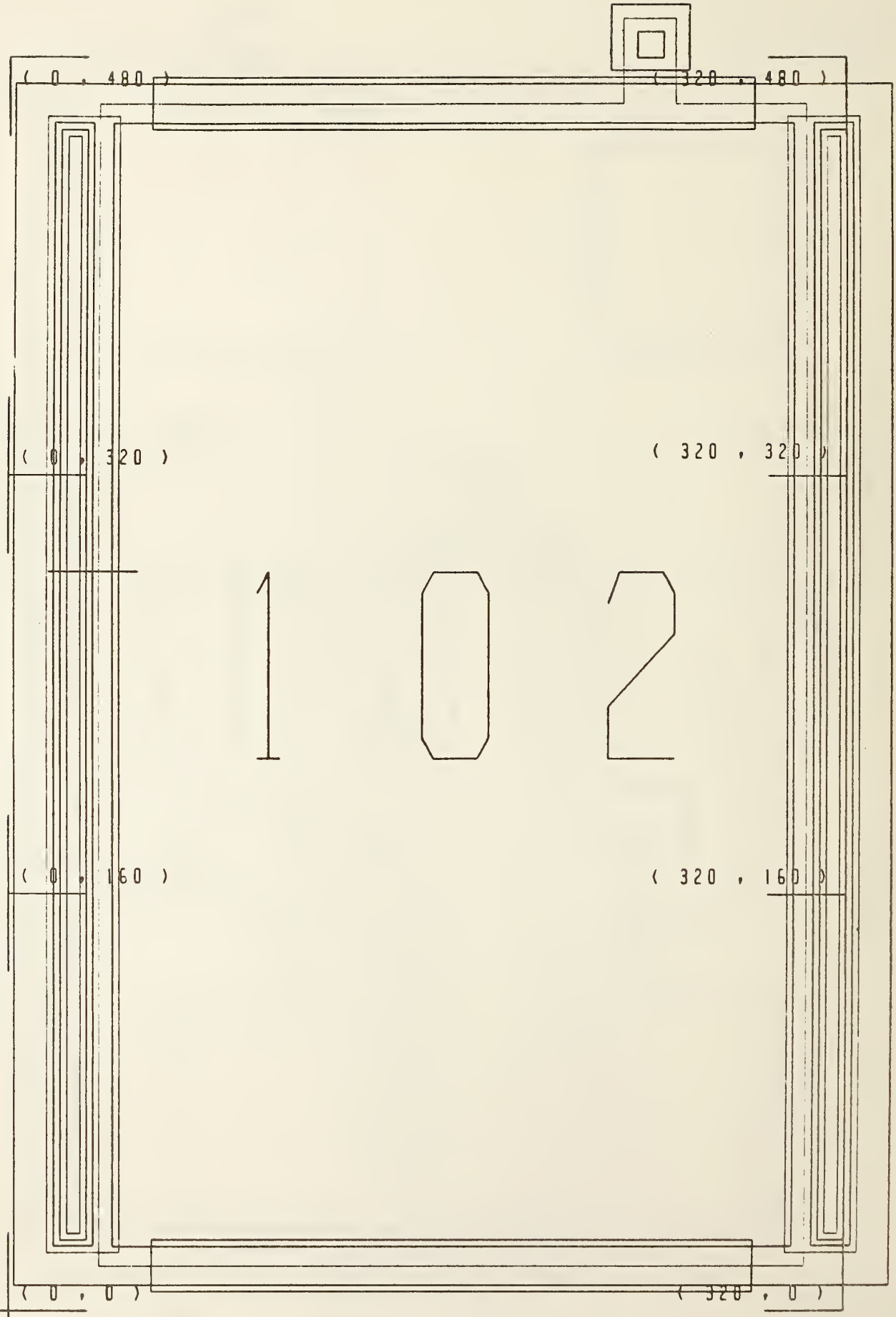


Figure 58. Capacitor/Transistor T-102.

Figure 59. Capacitor/Transistor T-103.

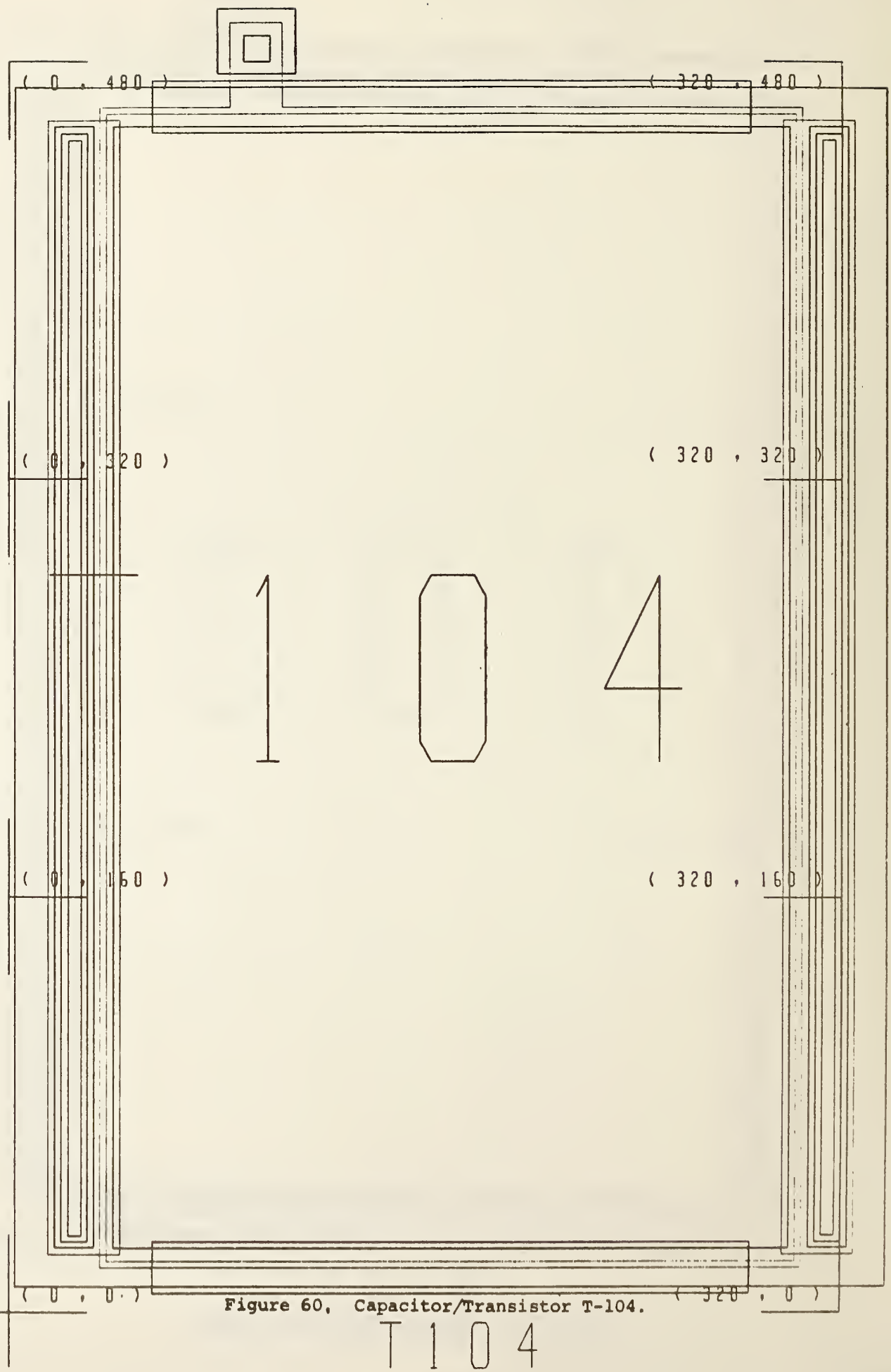


Figure 60, Capacitor/Transistor T-104.

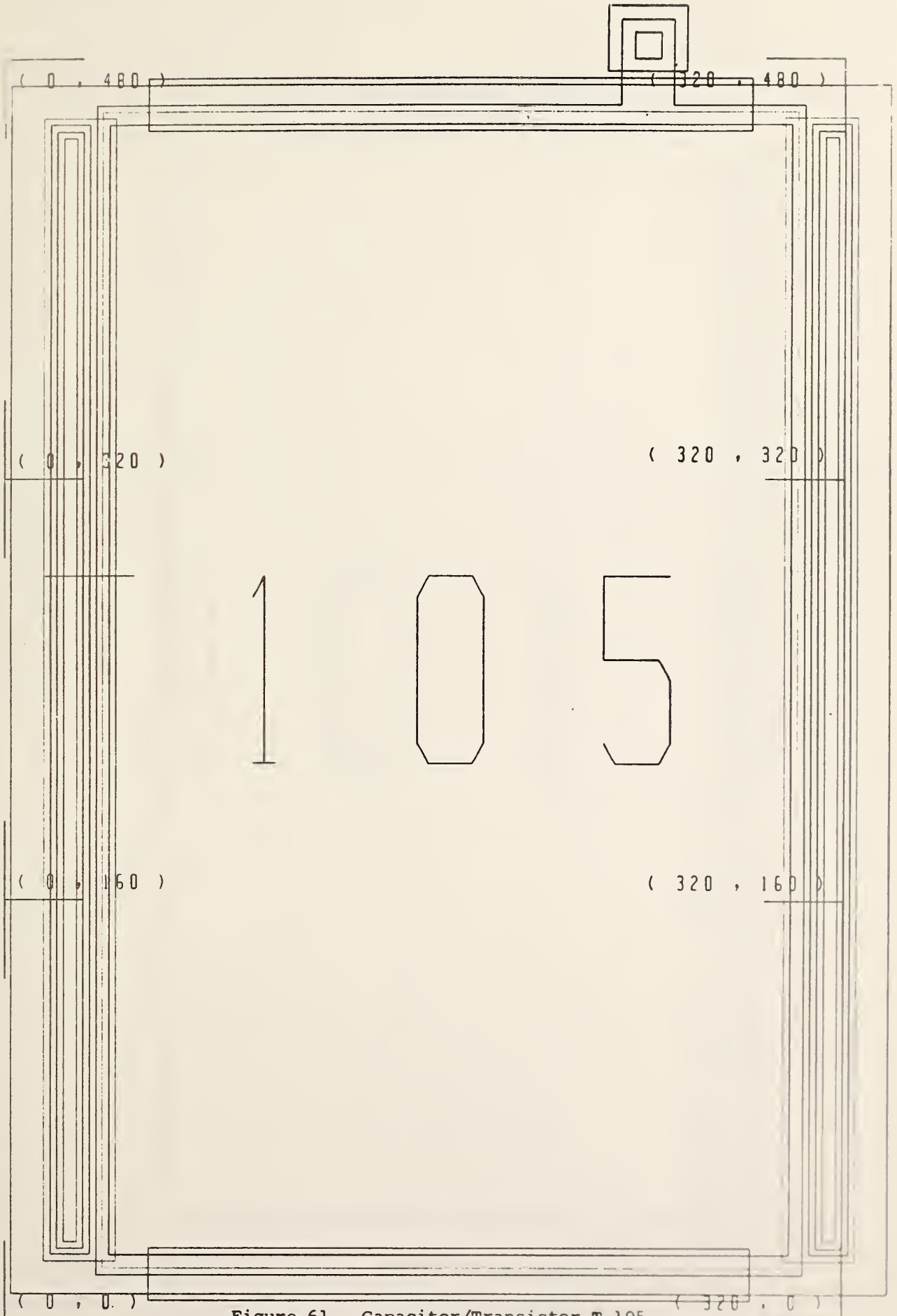


Figure 61. Capacitor/Transistor T-105.

T105

Figure 62. Capacitor/Transistor T-106.

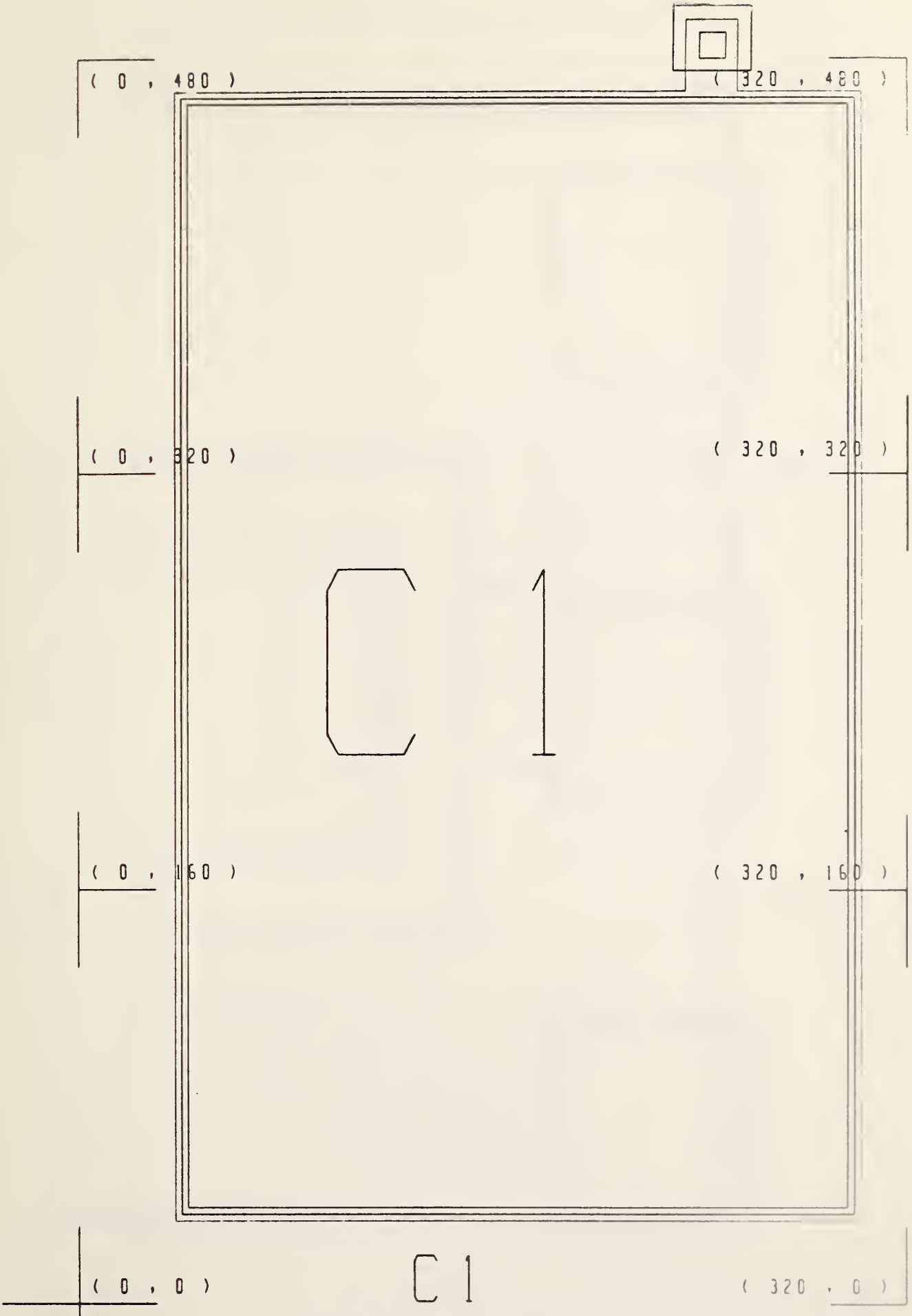


Figure 63. Capacitor C-1.

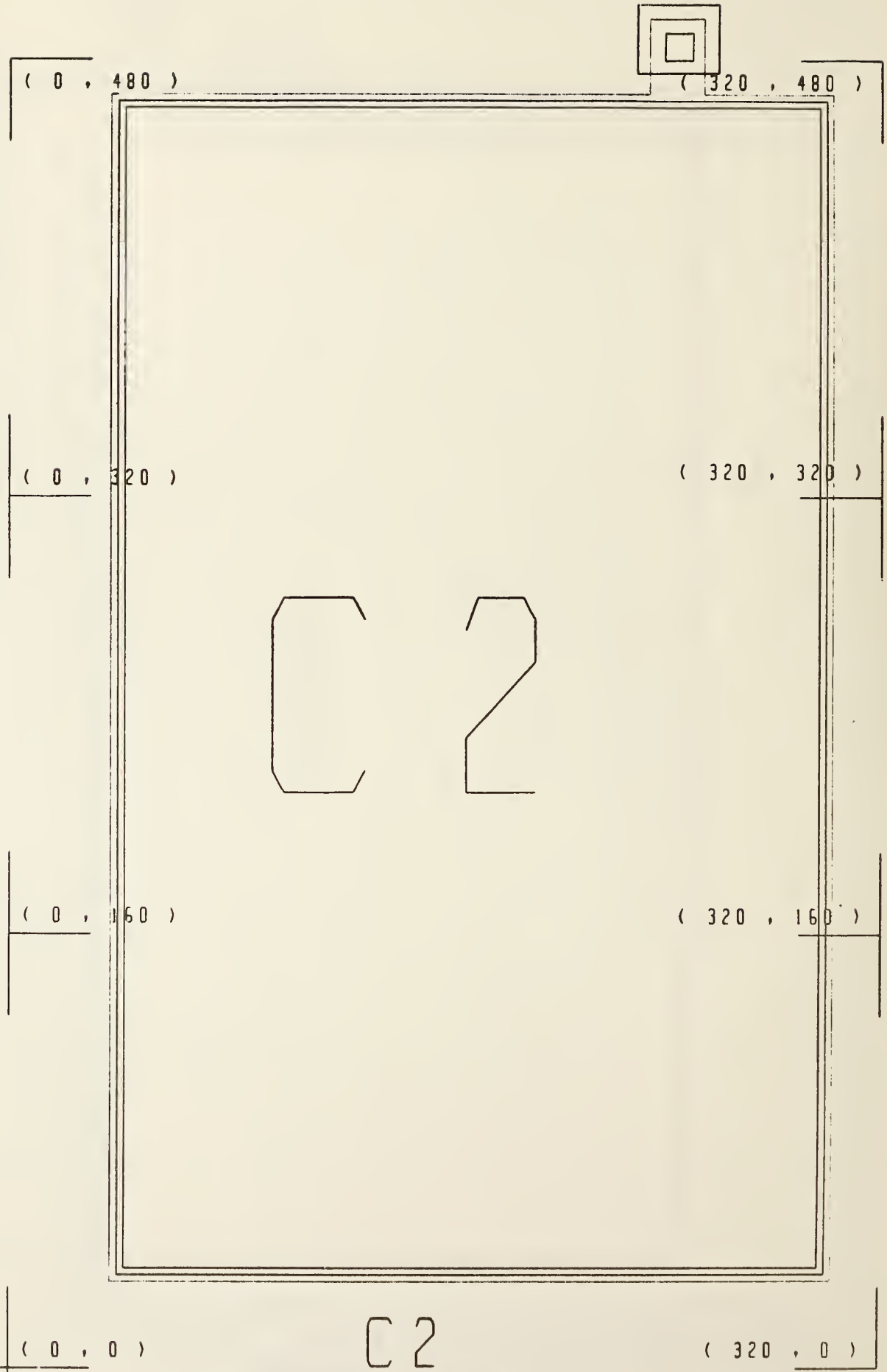


Figure 64. Capacitor C-2.

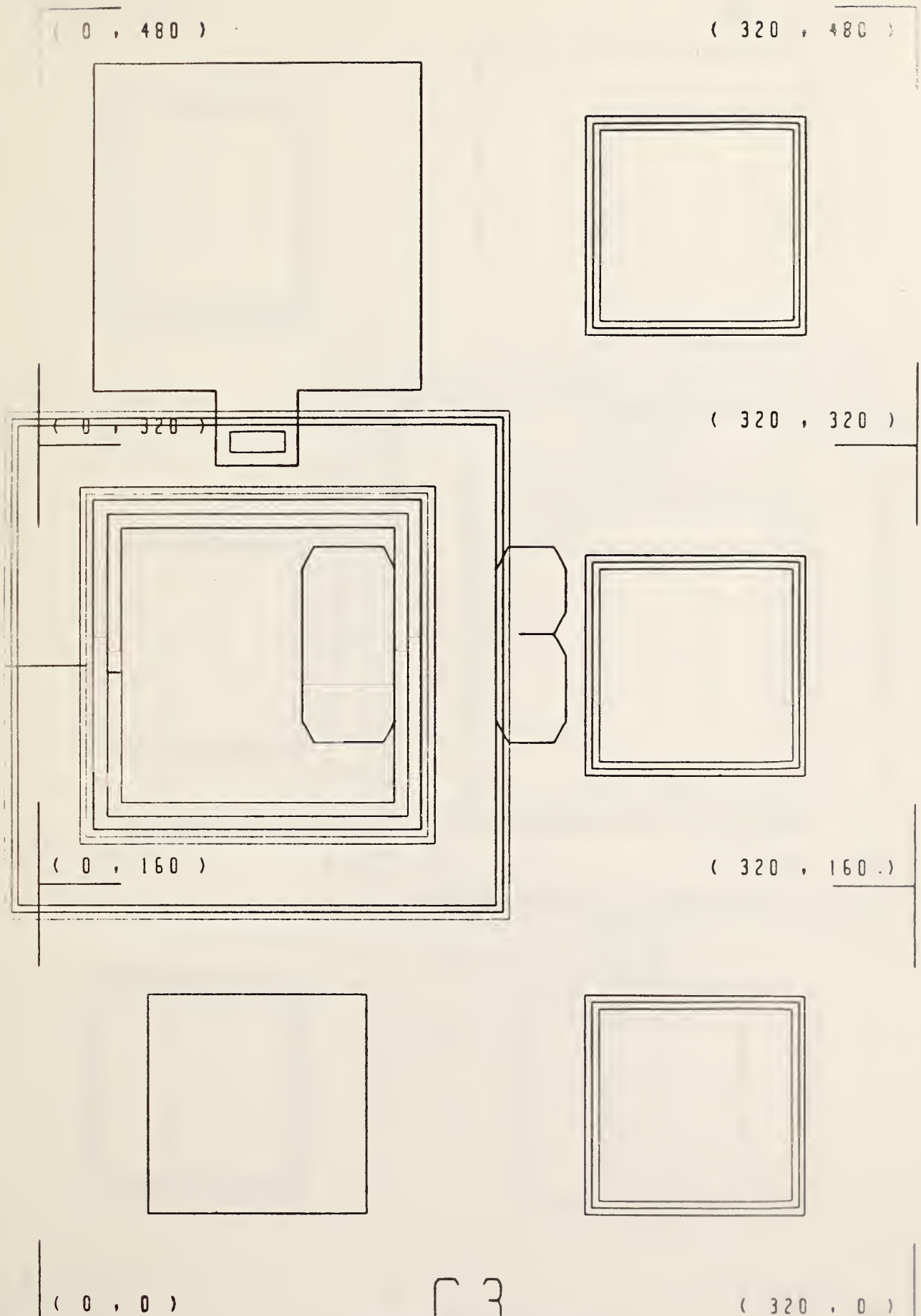


Figure 65. Capacitor C-3.

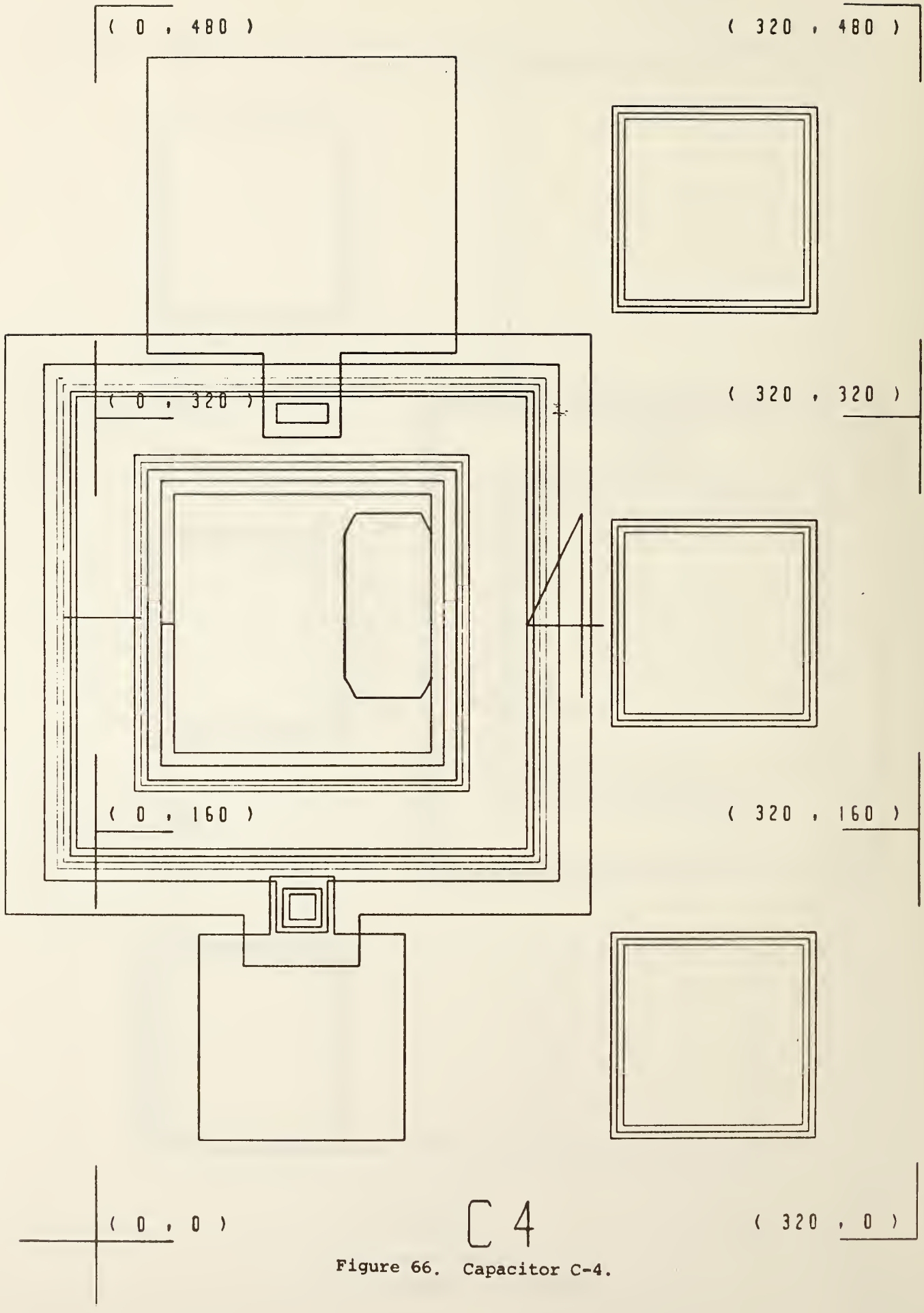


Figure 66. Capacitor C-4.

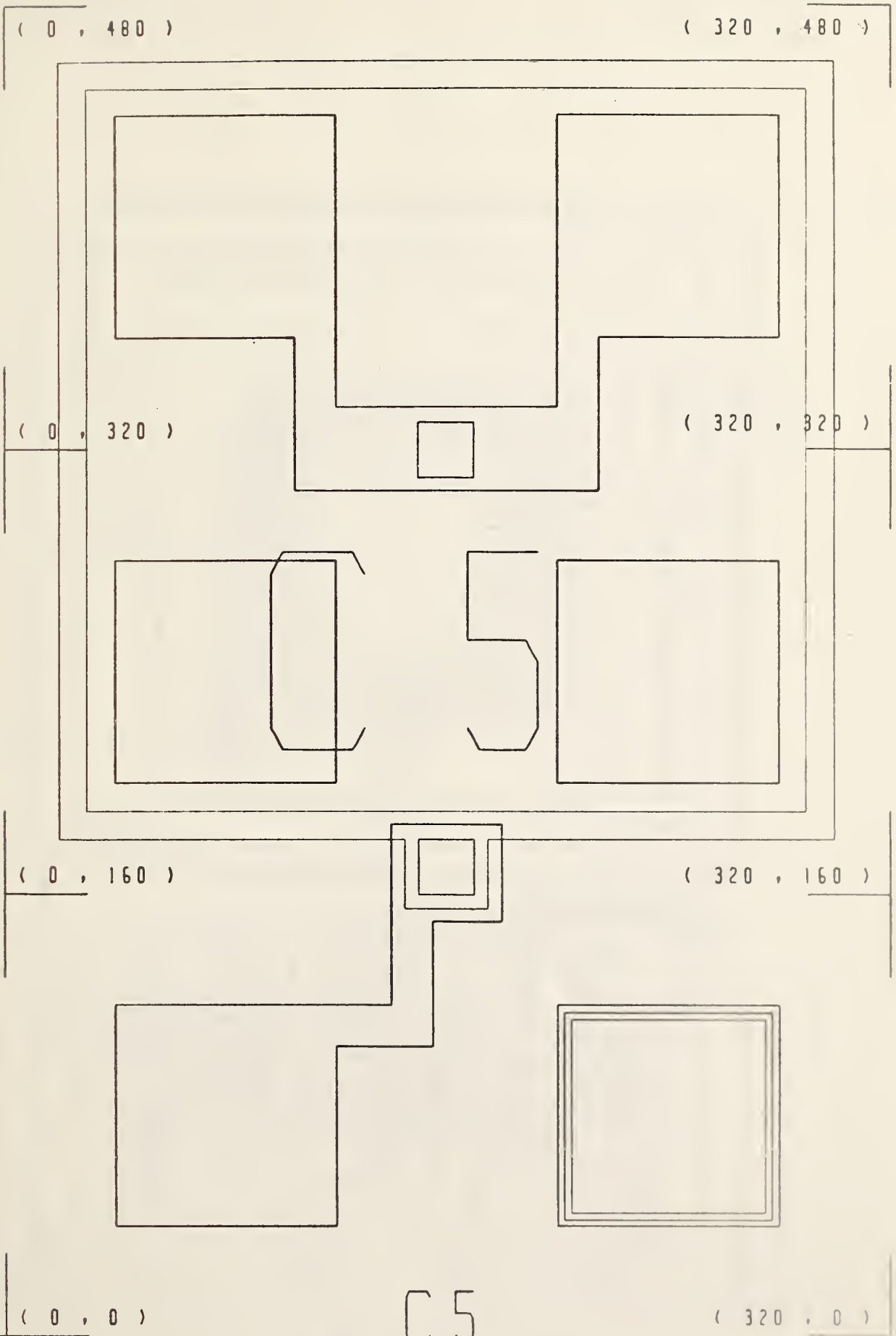


Figure 67. Capacitor C-5.

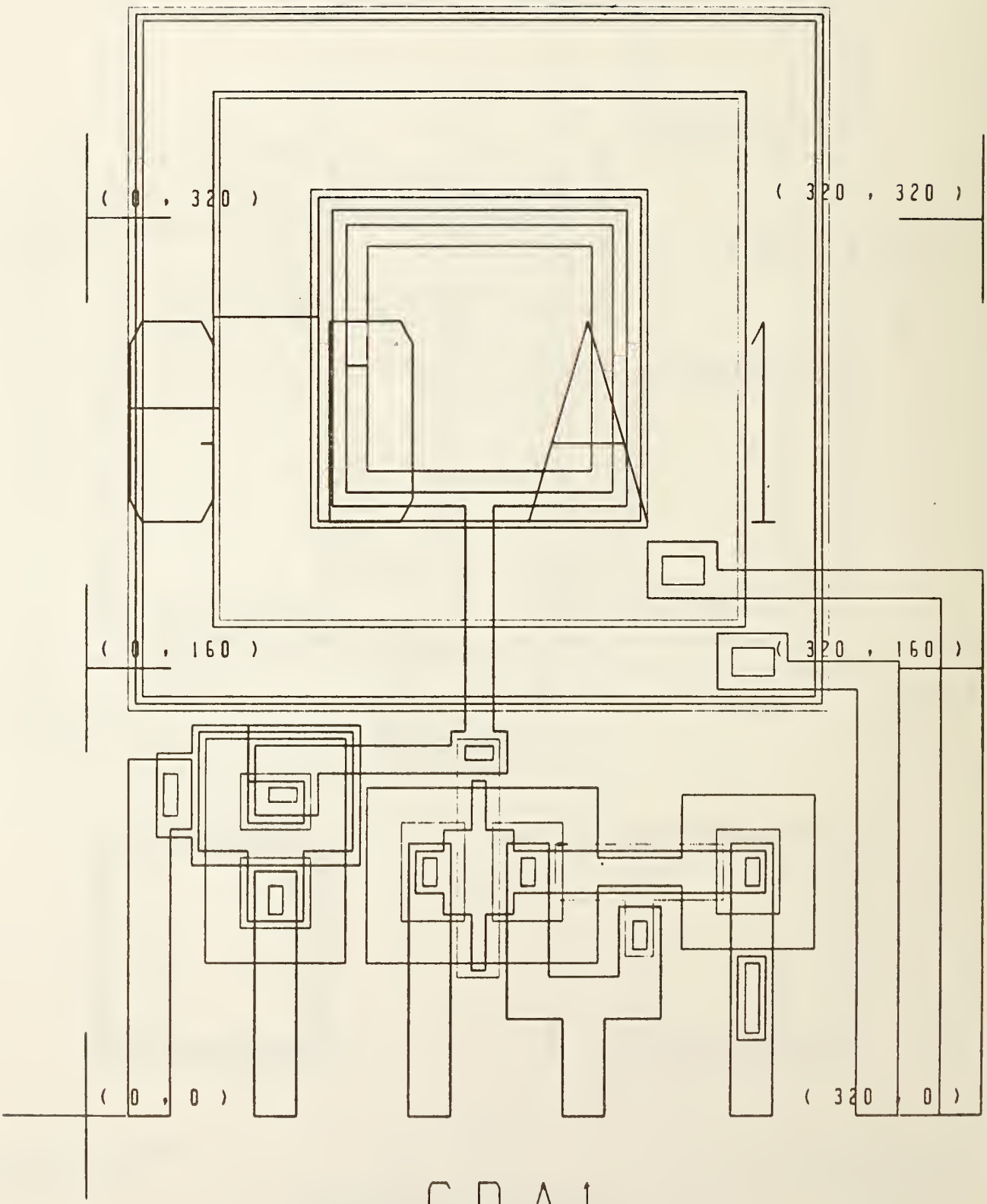


Figure 68. Gated-diode Electrometer GDA-1.

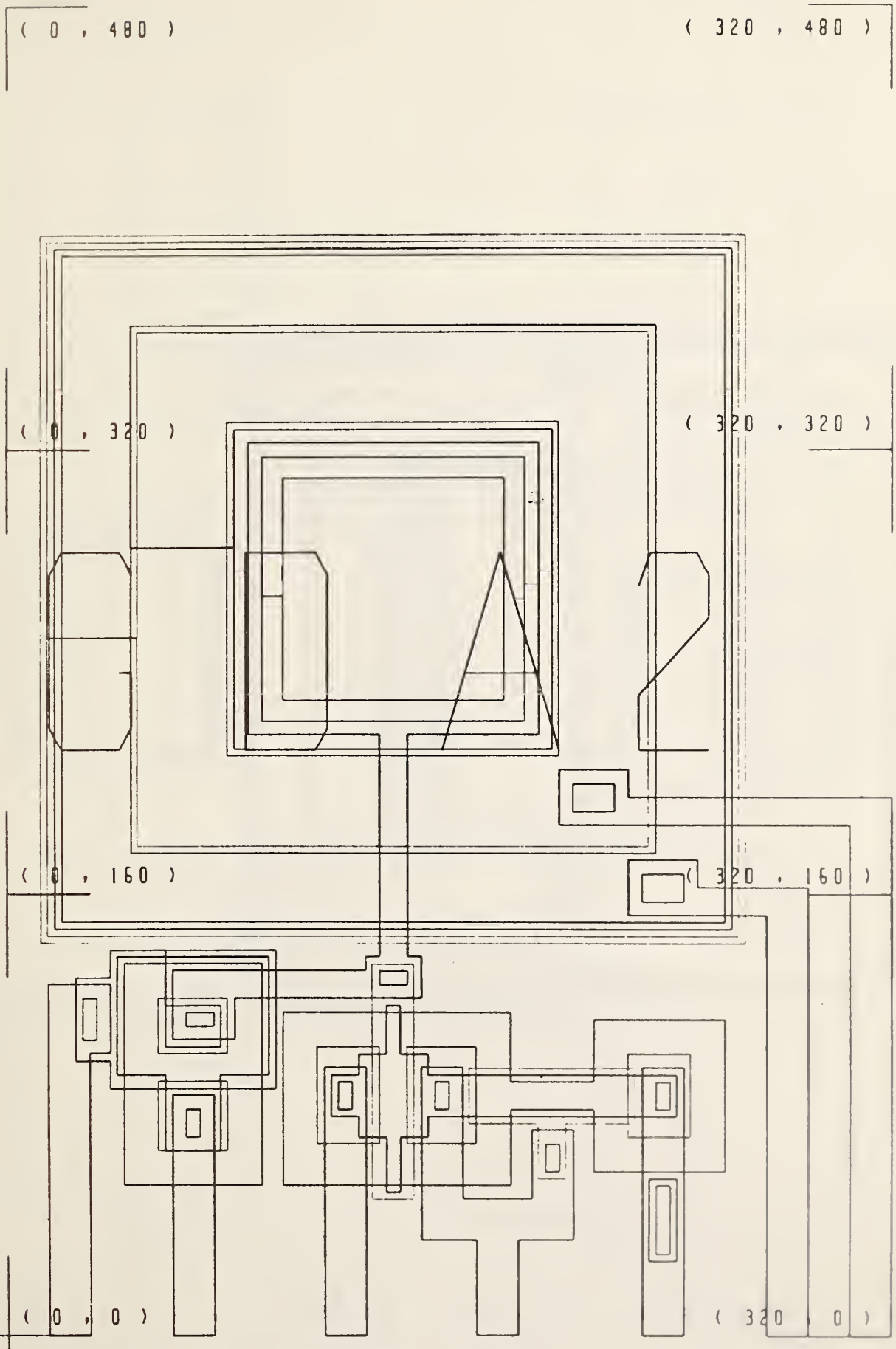


Figure 69. Gated-diode Electrometer GDA-2.

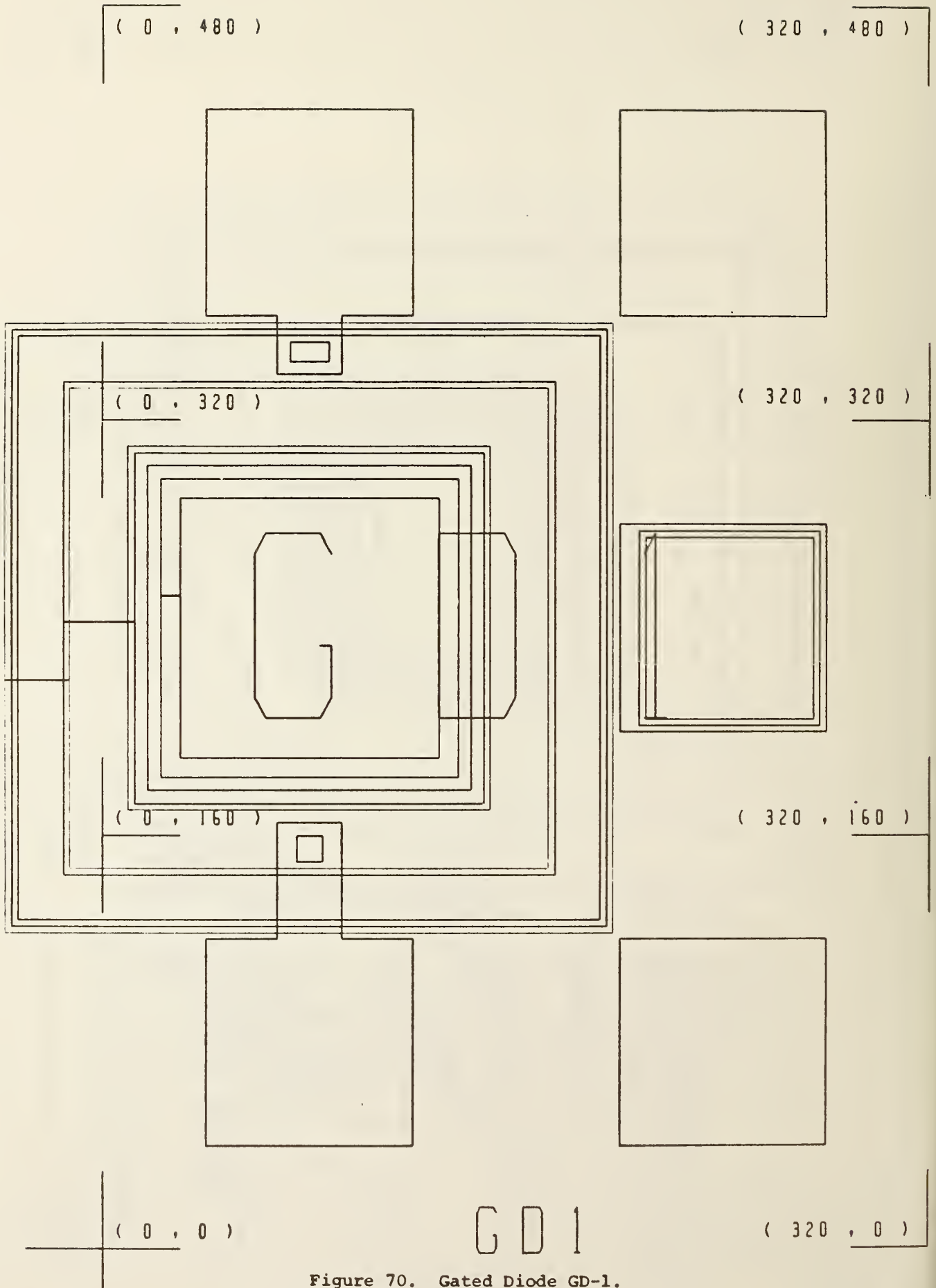


Figure 70. Gated Diode GD-1.

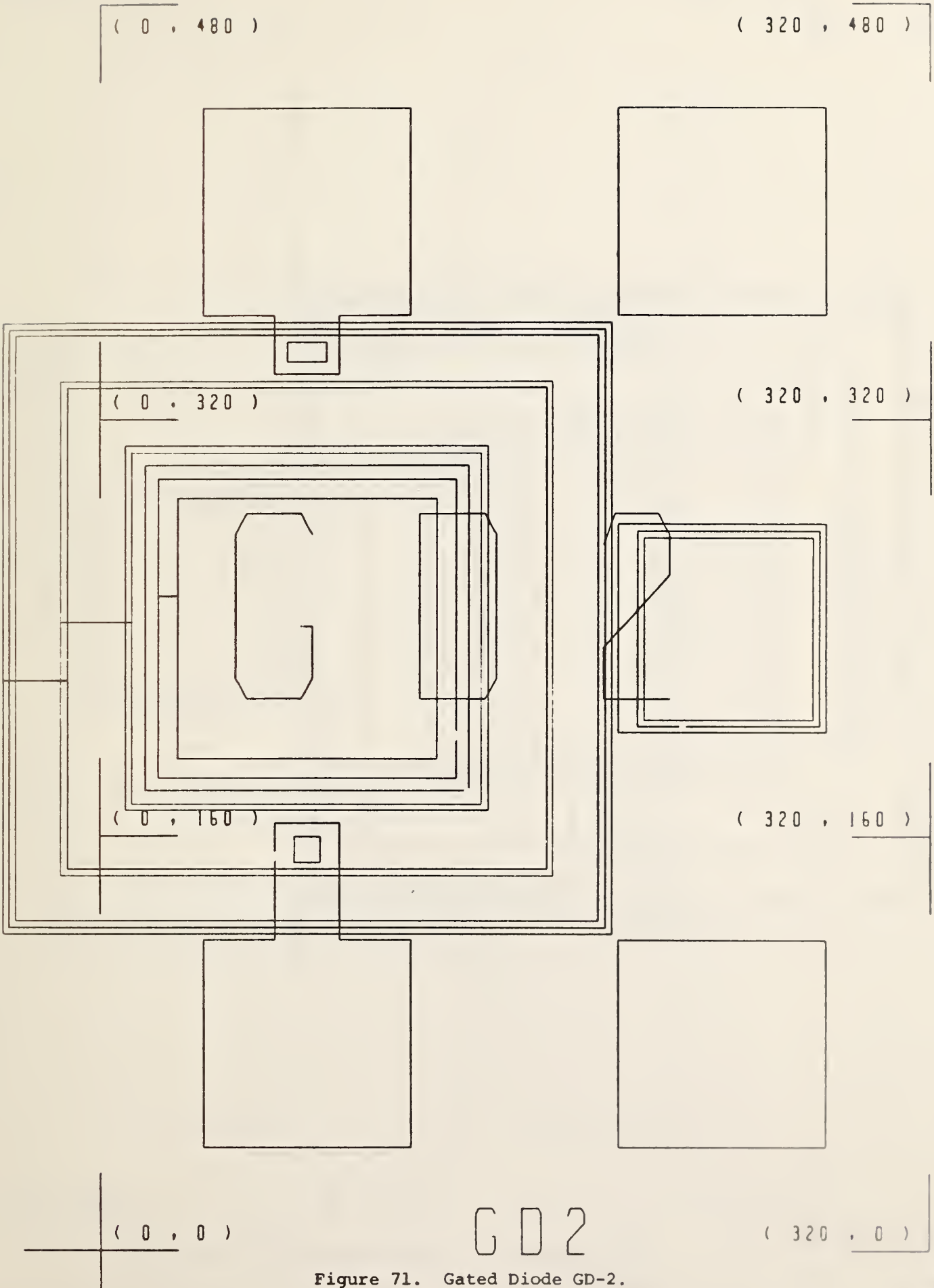


Figure 71. Gated Diode GD-2.

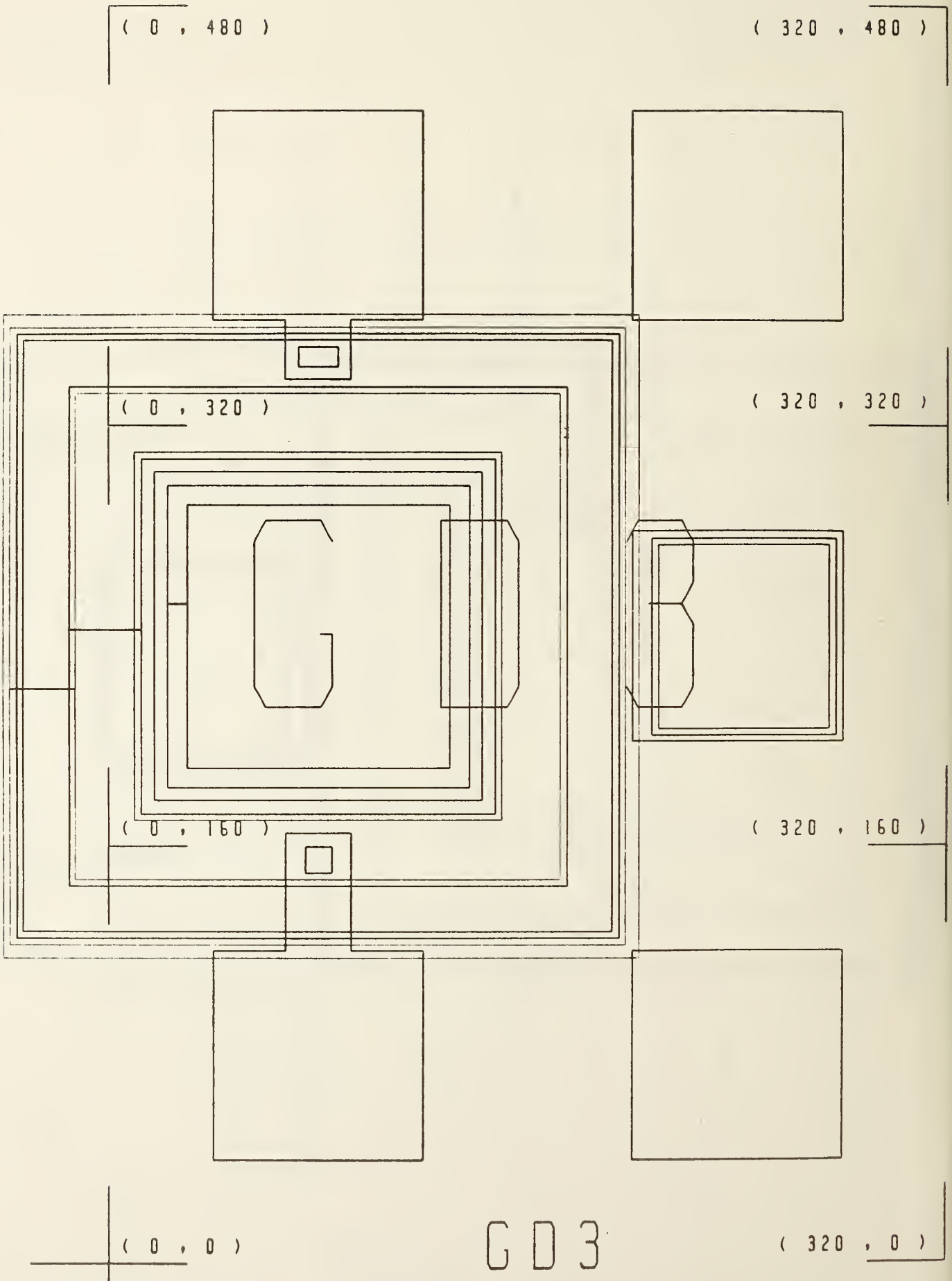


Figure 72. Gated Diode GD-3.

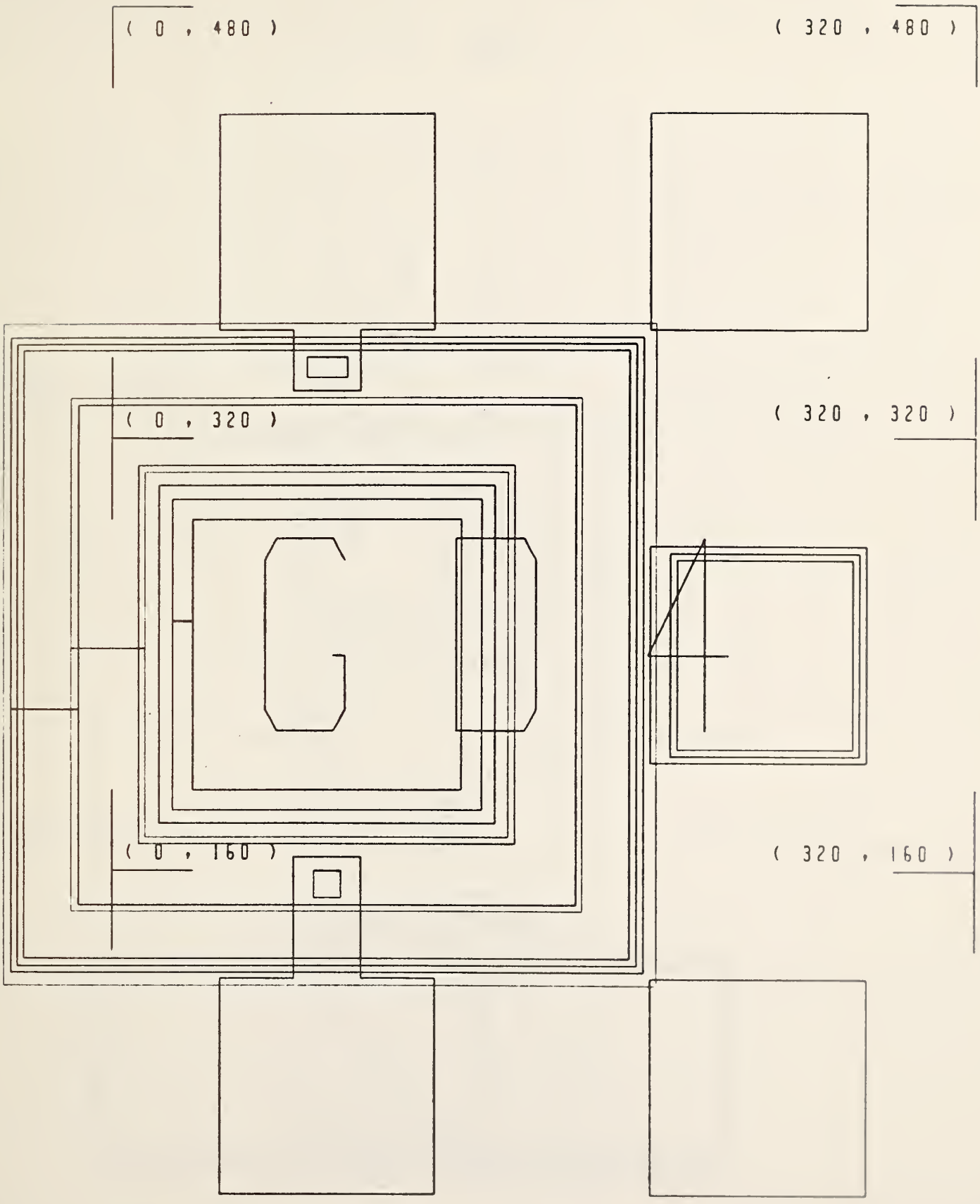


Figure 73. Gated Diode GD-4.

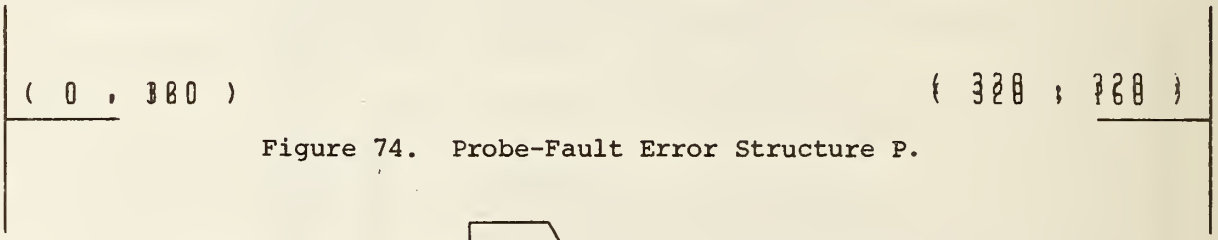
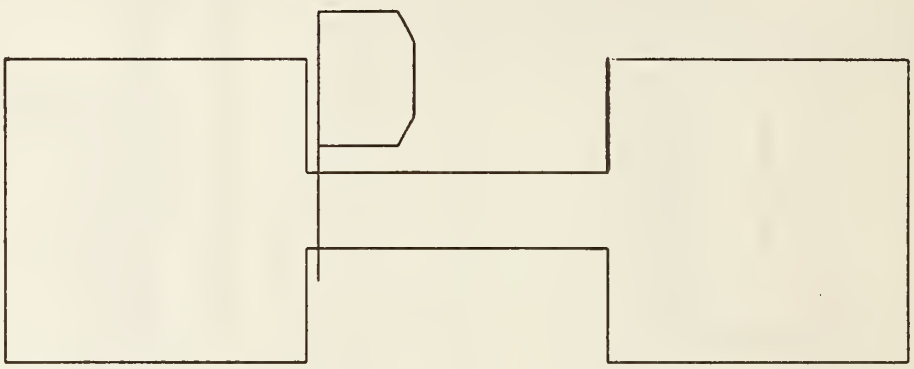


Figure 74. Probe-Fault Error Structure P.



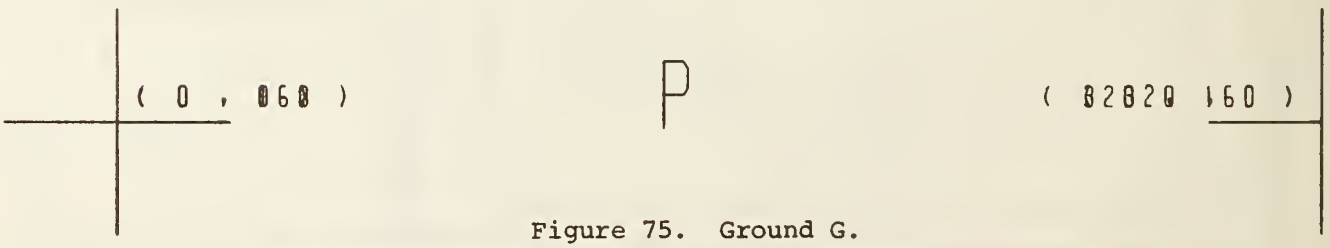
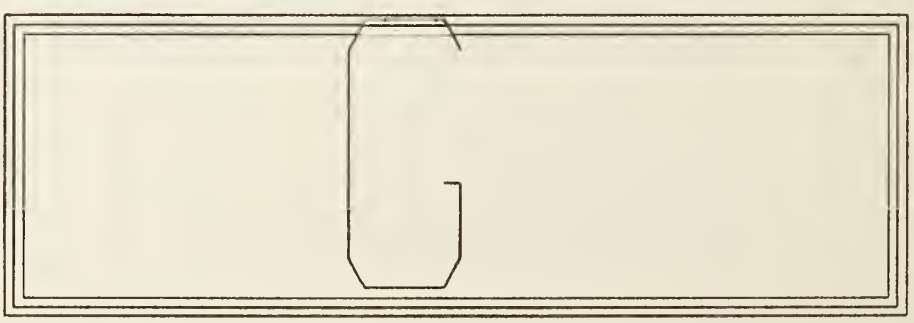


Figure 75. Ground G.



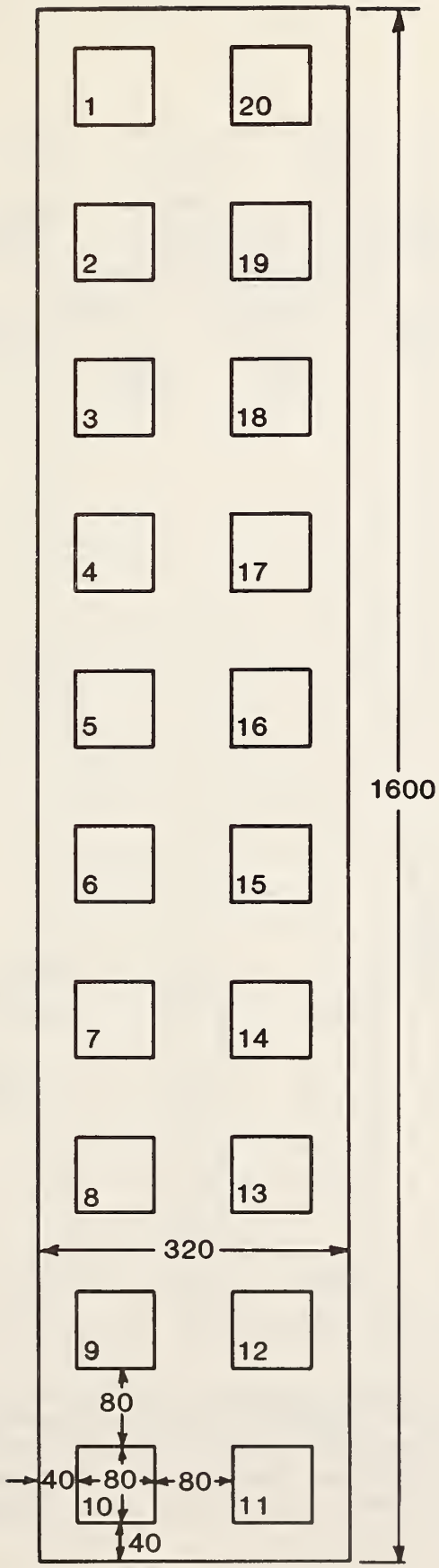


Figure 76. Cell probe pad array used for TERRY-2. Dimensions shown are in micrometers. Probe pads are numbered as shown at the lower left in each pad.

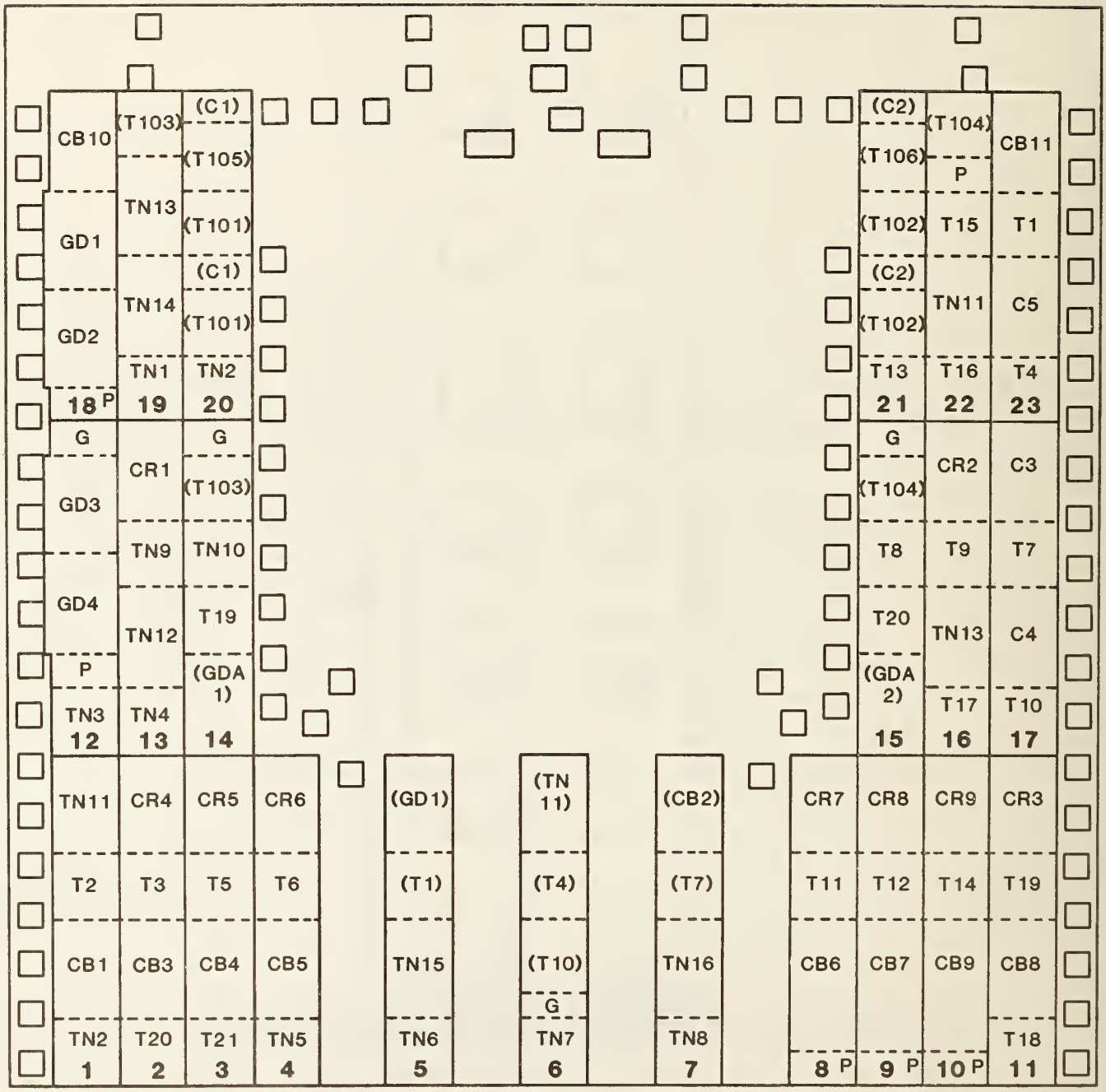


Figure 77. Schematic of TERRY-2 showing the locations of each probe pad cell. The bold numbers are the cell numbers. The test structure designations are also shown within the cells. Device designations in parentheses indicate that although they are addressed by probe pads in those locations, the devices are actually located outside the cells.

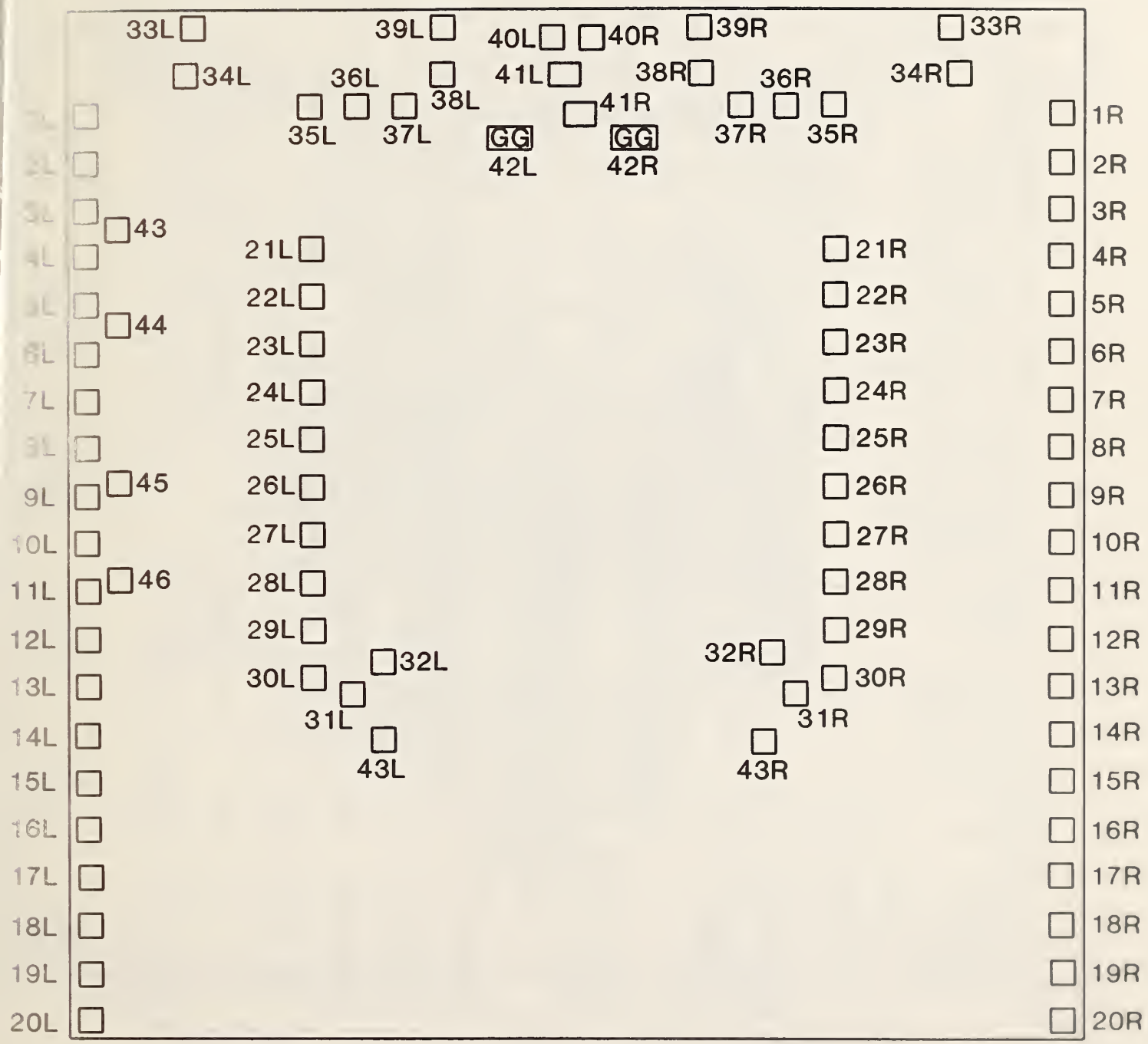


Figure 78. Schematic of TERRY-2 showing the locations and identifications of bonding pads.

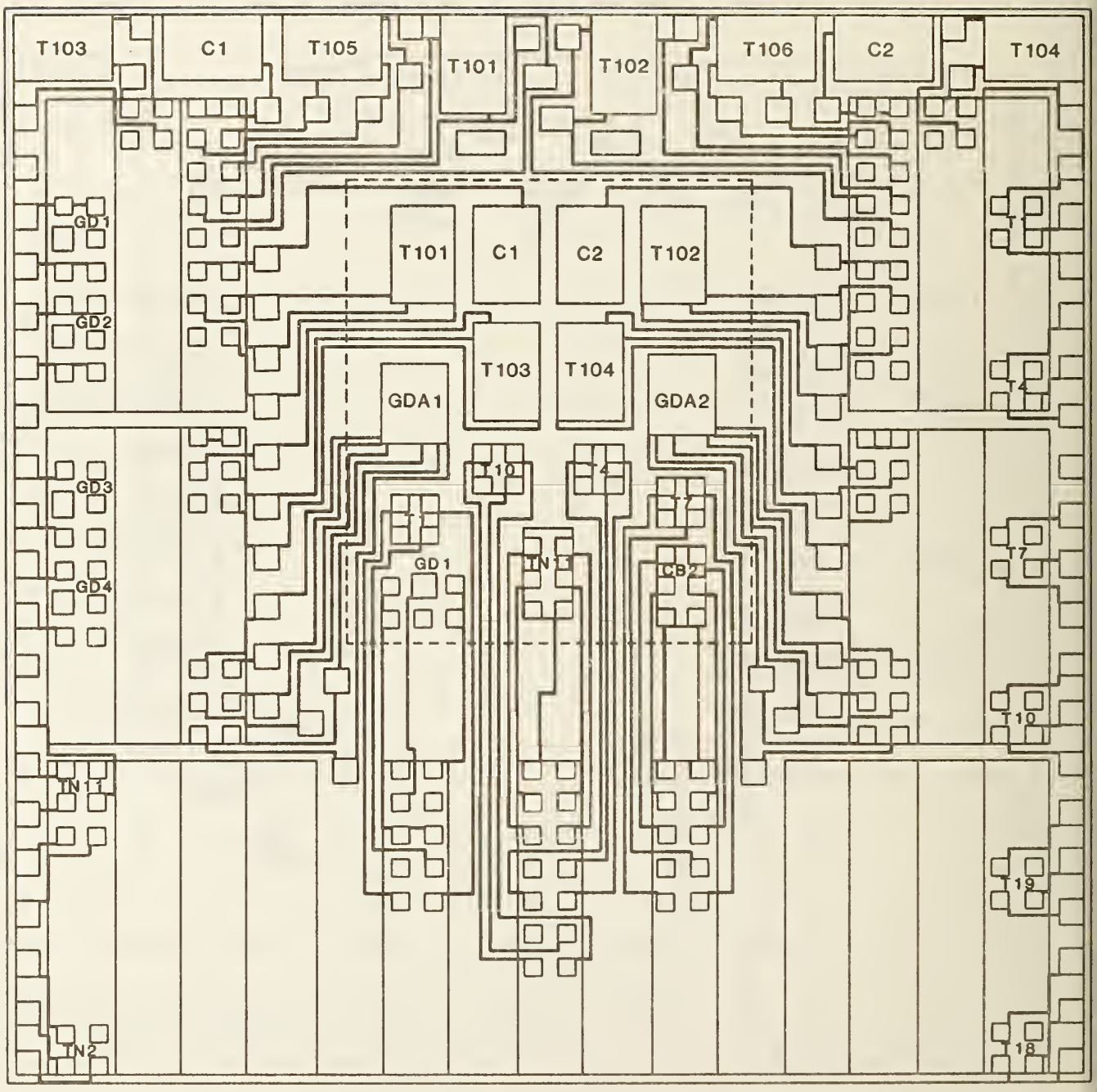


Figure 79. Schematic of TERRY-2 showing interconnections between test structures, probe pads, and bonding pads.

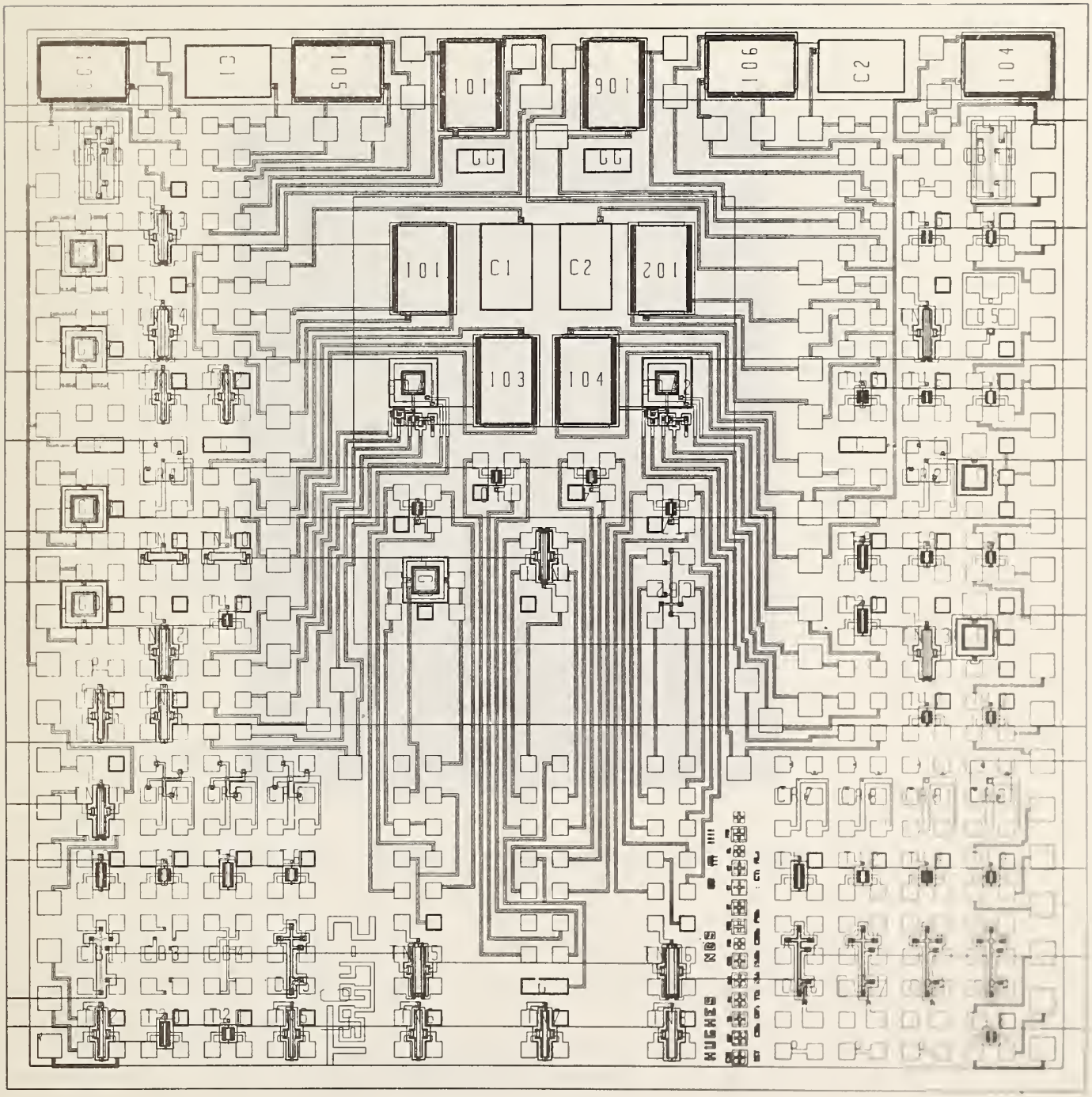


Figure 80a. TERRY-2 test chip layout schematic produced by the CAD system used to digitize the chip.

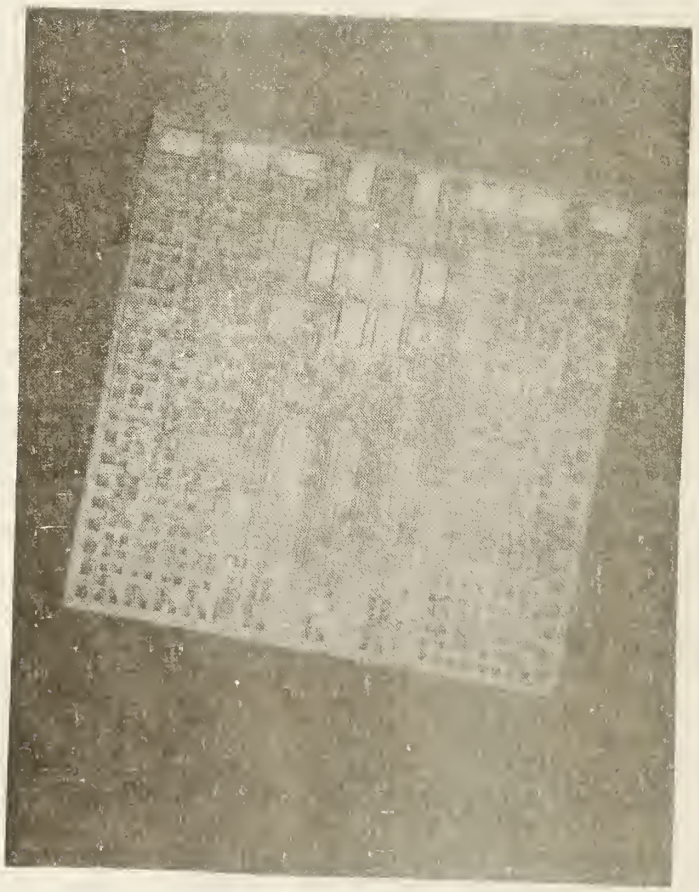


Figure 80b. Photograph of a TERRY-2 test chip.

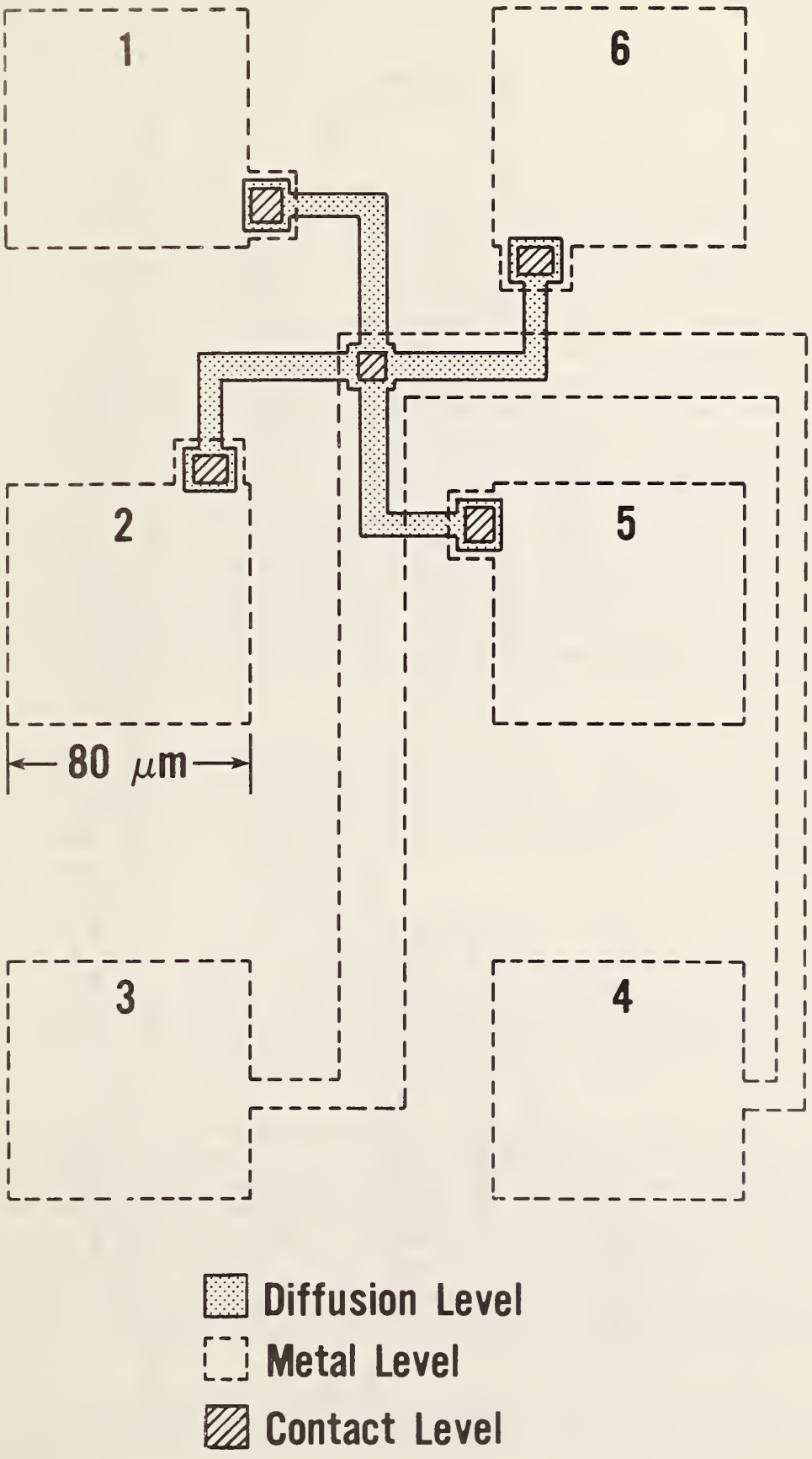


Figure 81. Schematic of a six-terminal metal-to-diffusion contact resistor (from Proctor *et al.*, 1983).

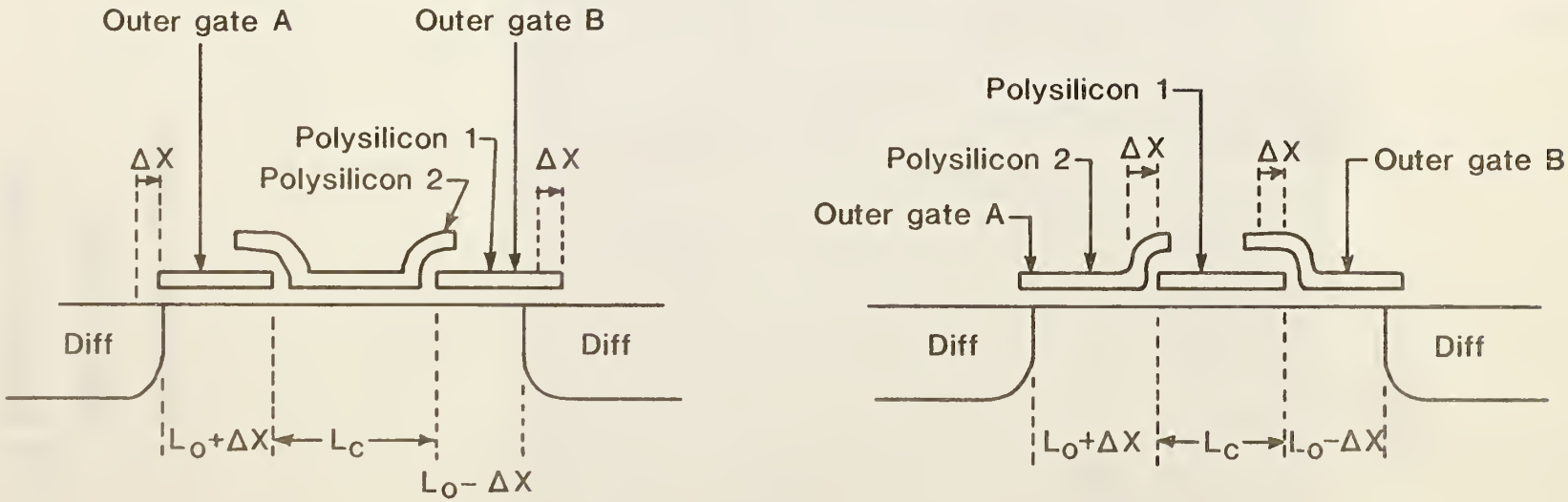


Figure 82. Schematic cross sections of triple-gate transistors showing the effect of a misalignment ΔX, in the source-to-drain current direction, between the PS1 mask and the DIFF mask. Misalignments involving the PS2 mask do not affect the channel lengths L_D and L_C, unless they are large enough to leave an ungated gap in the channel.

APPENDIX
Charge Pumping

Charge pumping is a method for determining the interface state density at the SiO_2-Si interface of a transistor or gated diode [Brugler and Jespers, 1969]. With the source and drain connected and reverse biased with respect to the substrate, the gate is pulsed so that the semiconductor surface is alternately accumulated and inverted. An electrometer connected from the source and drain to the substrate measures the pulsed dc current generated by alternately filling interface traps with free carriers from the inversion layer and then recombination of the trapped carriers with majority carriers in the bulk. The observance of charge pumping current requires that the emission time of the traps be longer than the time required for several other processes: the formation or disappearance of the inversion layer, the response of the majority carriers, and the filling of the traps. Also because of the finite emission time, some of the trapped carriers initially provided by the source and drain return to the inversion layer instead of capturing an opposite sign (majority) carrier from the substrate during accumulation. Capture of an opposite sign carrier is needed to complete the recombination process which causes the measured dc current. A complementary process involves trapping majority carriers from the substrate which recombine with inversion layer carriers during a later portion of the pulse, also causing a charge pumping current.

In an *n*-channel device, the charge pumping current flows from the substrate to the surface and then to the source and drain. The magnitude of the current is proportional to the frequency f at which the gate is pulsed, the area A_g of the gate, and the number of traps per unit area N_{it} which participate [Brugler, 1969]:*

$$I_{cp} = fqA_gN_{it} \quad . \tag{A-1}$$

Table A1 lists and defines the symbols used in this appendix. The above description is oversimplified since during the gate voltage cycle several processes occur, and each affects the magnitude of the measured charge pumping current.

The pulses which bias the gate have finite transition times; these times are also important in determining the magnitude of the charge pumping current. So, from the beginning, trapezoidal pulses with rise time t_1 and fall time t_2, pulse top V_{pos} and pulse bottom V_{neg} are considered. As an alternative, a three-level pulse can be used to pulse the gate (see fig. A1). The gate can be held at some voltage, $V_{baseline}$, for a time τ_1 during the rise of the pulse and for a time τ_2 during the fall of the pulse as shown in the figure. The advantages and disadvantages of this method are discussed later.

During one pulse cycle, the capture and emission processes which occur are illustrated in figure A2 and described below.

---

* See Table A1 for definitions of symbols used in this appendix.

For p-type material (n-channel enhancement-mode MOSFET), during the bottom of the pulse, at V_{neg}, the surface is in strong accumulation with a large concentration of holes forming an accumulation layer. The dominant mechanism for the filling of interface traps is hole capture. Empty traps remain empty and traps filled with an electron capture a hole which neutralizes the electron and results in recombination. The time constant for these reactions τ_{c_p} is given by

$$\frac{1}{\tau_{c_p}} = c_p = v_{th}\, \sigma_p p \,, \tag{A-2}$$

where v_{th} and σ_p are functions of the material and the surface, respectively, and p, the hole concentration depends on the gate voltage. This time constant depends only on the hole concentration and not on the energy of the trap in the band gap.

If during the transition of the pulse from V_{neg} to V_{pos} the inversion layer formed instantaneously, then there would not be time for other mechanisms to alter the state of the interface traps. In fact, the transition time is finite and the emission of holes from the interface states is large enough to make a measurable difference in the final current. The time constant for emission of holes from traps is governed by the difference in energy of the trap and the valence band:

$$\frac{1}{\tau_{e_p}} = e_p = v_{th}\, \sigma_p N_v e^{\frac{-(E_T - E_v)}{kT}} \,. \tag{A-3}$$

Independent of electron concentration, emission of holes is rapid from traps close to the valence band and is slow for those near midgap or the conduction band. The emitted holes return to the bulk and thus do not contribute to the charge pumping current.

The inversion layer forms very rapidly once the gate voltage is beyond the threshold voltage because the source and drain provide the carriers. It is assumed that the inversion layer responds instantaneously to changes in gate voltage although the traps do not. During the top of the pulse at voltage V_{pos}, the traps change their state by electron capture, and the time constant for electron capture is

$$\frac{1}{\tau_{c_n}} = c_n = v_{th}\, \sigma_n n \,. \tag{A-4}$$

Again, note that the time required for electron capture depends on electron concentration and not on trap energy. Traps which have not emitted a hole capture an electron and thus contribute to the charge pumping current.

It is assumed that during the transition from inversion to accumulation, the inversion layer responds instantaneously to the gate voltage although the traps do not. The electron traps emit electrons with a time constant of emission τ_{e_n} which is

$$\frac{1}{\tau_{e_n}} = e_n = v_{th}\,\sigma_n N_c e^{\frac{(E_T - E_c)}{kT}} . \qquad \text{(A-5)}$$

e that electron traps close to the conduction band emit electrons rapid- while those near midgap emit slowly. Many of the emitted electrons re- n to the source and drain from which they came and thus do not contribute the charge pumping current.

en the surface enters accumulation and the time constant for hole capture short, the electrons are neutralized by holes from the bulk as discussed eviously and these electrons contribute to the charge pumping current.

oeseneken *et al.* have assumed that capture and emission processes occur ring different time segments and do not overlap. They have assumed that r surface potentials outside the range from flatband to threshold, the rface states are in equilibrium with the bulk Fermi level. During the ansition period (either rising or falling), they assume that some of the rface states are out of equilibrium if their time constant of emission is nger than the switching time.

immons and Wei have obtained a closed form expression for the nonsteady- state emission from a continuous distribution of traps of constant capture ross section. For electrons trapped at the interface and out of equilibri- m, after a time t all traps above energy $E_m(t)$ will have emitted and any trap below $E_m(t)$ will still have the trapped carrier where

$$E_m(t) = E_i - kT\ell n \left[1-\left[1-e^{(E_i-E_m(0)/kT)}\right] \exp\left(\sigma_n v_{th} te^{(E_i-E_g)/kT}\right)\right] . \qquad \text{(A-6)}$$

Here, E_i is the intrinsic energy level and E_g is the gap energy. $E_m(0)$ is the energy at which nonsteady state emission begins.

Further, Groeseneken *et al.* have assumed that every carrier emitted returns to its origin and does not contribute to the charge pumping current. That is, carriers captured from the inversion layer return to the source and drain when emitted, while majority carriers captured from the bulk return to the bulk when emitted. Furthermore, they assume that the capture by a filled trap of the opposite sign carrier which completes the recombination process does not occur during the nonequilibrium emission part of the transition from flatbands to threshold. This conclusion is quite natural when the depletion approximation is used because in the depletion approximation, $n = p = 0$ in the depletion region.

With the above assumptions, Groeseneken *et al.* [1984] find:

$$I_{cp} = 2q\overline{D_{it}}\, f\, A_g \cdot kT\, \ell n \left[\frac{\left|V_{FB} - V_T\right|}{V_{pos} - V_{neg}} v_{th} n_i \sqrt{\sigma_n \sigma_p t_f t_r}\right] . \qquad \text{(A-7)}$$

In this equation, the term in brackets describes the range of potential in which carriers trapped in the interface state remain trapped until they recombine with the opposite sign carrier. If the fall or rise times are longer or the majority-carrier capture cross sections larger, the charge pumping current decreases in magnitude (note that the quantity in brackets must be less than or equal to unity).

Also, Groeseneken *et al.* [1984] show that the distribution of traps in energy can be measured, if the majority-carrier capture cross sections of the traps are constant, by varying either the rise or fall time. The density of traps per unit area per unit energy is

$$D_{it}(E_1) = - \frac{1}{qA_g f\, kT} \frac{dI_{cp}}{d\ell nt_r}$$

$$D_{it}(E_2) = - \frac{1}{qA_g f\, kT} \frac{dI_{cp}}{d\ell nt_f} , \qquad \text{(A-8)}$$

where E_2 and E_1 are the upper and lower bounds of the energy range of traps which contribute to charge pumping.

The energy at which $D_{it}(E)$ is measured is found from

$$E_2 = E_i - kT\ell n \left[\sigma_n n_i v_{th} \frac{\left|V_{FB} - V_T\right|}{V_{pos} - V_{neg}} t_f\right] , \qquad \text{(A-9)}$$

or

$$E_1 = E_i + kT\ell n \left[\sigma_p n_i v_{th} \frac{\left|V_{FB} - V_T\right|}{V_{pos} - V_{neg}} t_r\right] , \qquad \text{(A-10)}$$

depending on whether the leading edge t_r or falling edge t_f is used. To calculate the value of E, it is necessary to estimate σ_p or σ_n which is a drawback; the geometric mean of σ_n and σ_p can be found by fitting eq (A-7), but σ_p and σ_n cannot be separately determined easily.

A clear-cut test of the validity of these assumptions may be made by measuring the increase in charge pumping current as an inverted surface is pulsed closer and closer to flatbands. Alternatively, the surface may be held near flatbands and pulsed further into depletion and then inversion. These methods have been proposed by others, but never examined in detail [Brugler, 1969, and Elliot, 1975]. A comparison of the charge pumping current measured using the former technique to a surface potential versus gate bias curve shows that a significant I_{cp} is measured before the pulse bottom is sufficiently negative to bias the surface to flatbands. In the case of an *n*-channel device, this nonzero current is produced by either capture of holes by traps containing electrons or failure of emitted carriers to return to the

source or drain. These two phenomena would lead to errors in determination of the density of interface traps from the charge pumping current using eqs (A-7) and (A-8).

The effect on the charge pumping current of capture during the nonsteady-state regime and of inefficient collection of emitted carriers can be shown using the three-level pulse technique described earlier. An advantage of the three-level pulse technique over the variable falltime technique is that the surface potential is held at some constant value during the times τ_1 and τ_2 corresponding to the choice of $V_{baseline}$. The relation between surface potential and gate voltage can be obtained experimentally by measuring the quasi-static capacitance on an adjacent capacitor. The effect of capture or failure to collect emitted carriers in the nonsteady-state emission regime is a function of the surface potential. The emission of carriers from surface traps depends only on the trap properties and whether the trap is in or out of equilibrium, not on the exact value of the carrier concentration at the surface. It is assumed that the response of carriers in the bulk is instantaneous on the time scale of the experiment and that the nonsteady-state emission occurs somewhere in the range from accumulation to strong inversion.

Since there are systematic errors in determining the density of states using the charge pumping current, a comparison of the $D_{it}(E)$ measured using another technique should be made. The high frequency-low frequency capacitance-voltage comparison (Nicollian, 1982) allows a measured $D_{it}(E)$ to be obtained on a capacitor provided that the capture cross sections for surface states are similar to those commonly observed. The comparison can be performed on a gated diode or a transistor with a gate large enough to obtain accurate capacitance-voltage data. Preliminary measurements show that the charge pumping current value can be used to calculate interface trap densities within 20% of the value obtained from capacitance-voltage data. The large capacitor/transistors on TERRY-2 will allow a more precise comparison of the results from these techniques.

Table A1. List of Symbols for Charge Pumping.

I_{cp}	charge pumping current
τ_{c_p}, τ_{c_n}	time constant for capture of holes and electrons, respectively
τ_{e_p}, τ_{e_n}	time constant for emission of holes and electrons, respectively
v_{th}	thermal velocity of electrons or holes $\sim 10^7$
σ_p	capture cross section for holes
σ_n	capture cross section for electrons
p	hole concentration
n	electron concentration
c_p, c_n	capture rates of hole and electrons, respectively
e_p, e_n	emission rates of hole and electrons, respectively
V_{pos}	pulse top voltage
V_{neg}	pulse bottom voltage
t_r	transition time for leading edge, see figure A1
t_f	transition time for trailing edge, see figure A1
τ_1, τ_2	time during which gate is held at voltage $V_{baseline}$, see figure A1
$D_{it}(E)$	number of traps per unit area per unit energy
N_{it}	number of traps per unit area
kT	mean thermal energy, k, Boltzmann's constant, T, absolute temperature
N_c, N_v	density of states of conduction band, valence band
A_g	gate area

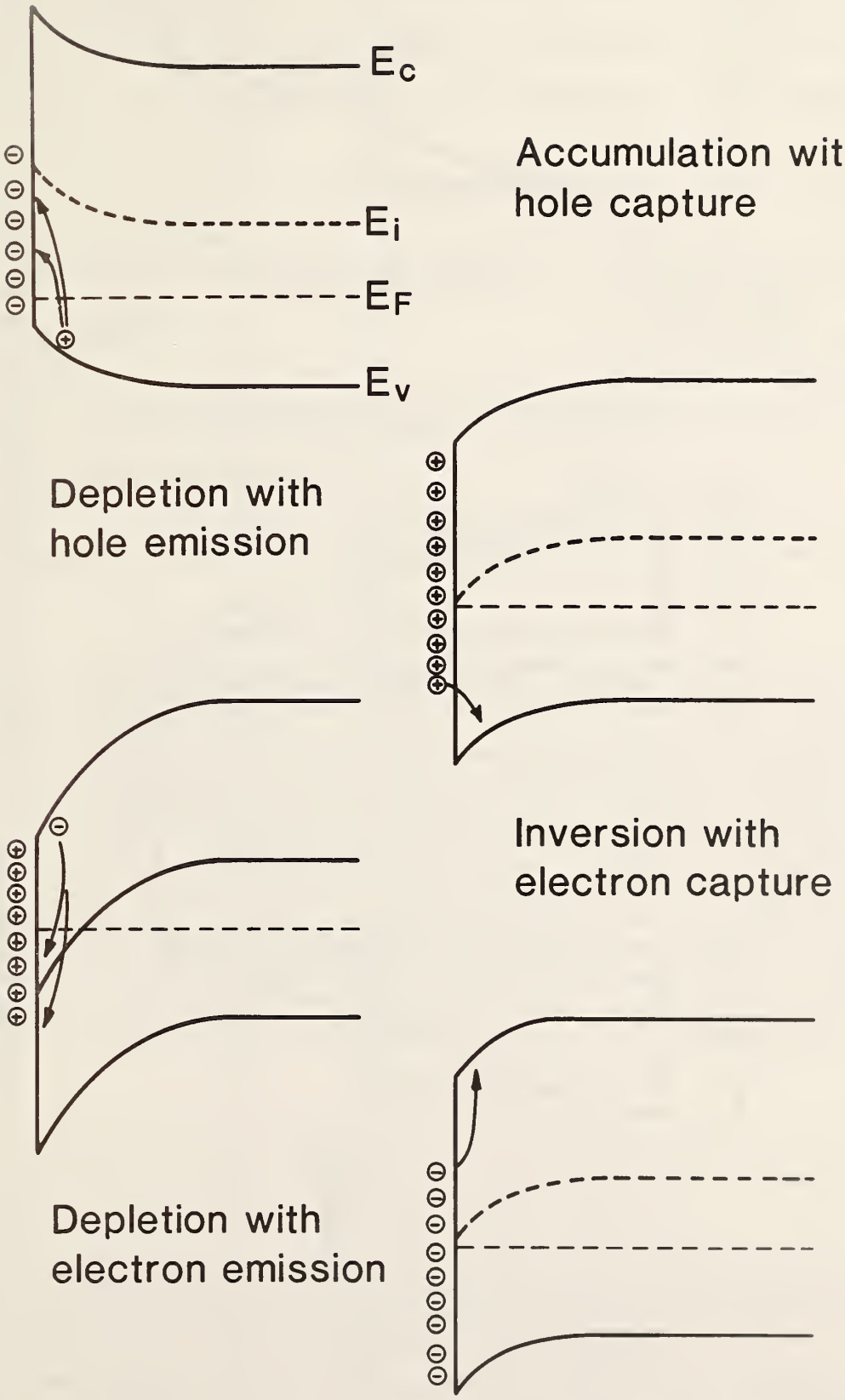


Figure A1. Comparison between trapezoidal pulse (——) and three-level pulse (------). The time spent in nonsteady state emission is τ_1 and τ_2.

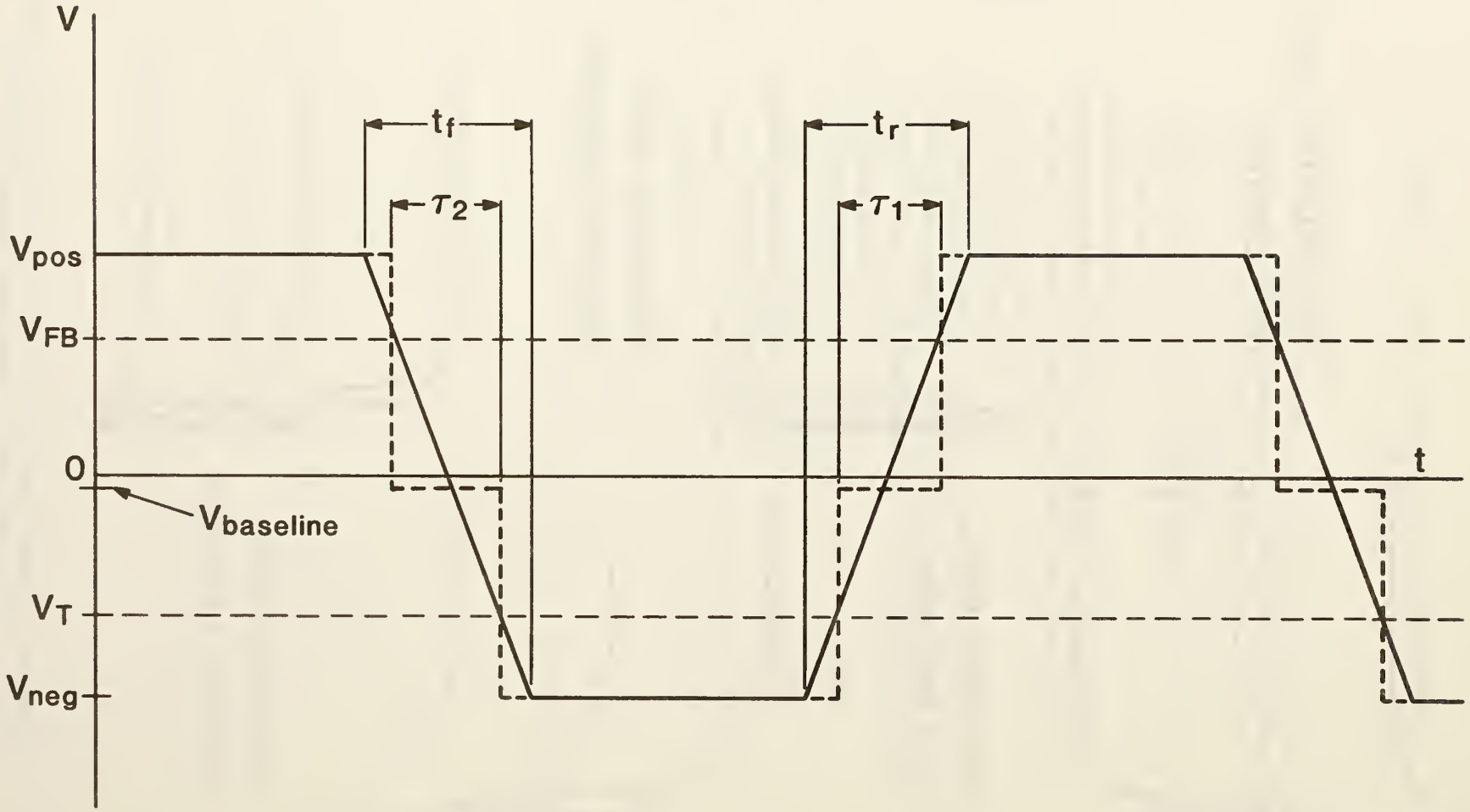


Figure A2. Capture and emission processes during charge pumping on a *p*-type substrate.

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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

Test chip TERRY-2 is intended to be used for characterization of the performance of buried-channel charge coupled device (CCD) imagers fabricated with a double-polysilicon-gate process which includes several implants. Test structures in TERRY-2 address two areas judged to be key ones for CCD performance, device parameters and process parameters, including material properties. TERRY-2 is a modular chip designed for automated testability; wire bonding of selected devices for radiation effects testing; thinning of a region containing test structures, in the same manner a back-side-illuminated CCD would be thinned; and beveling of large devices for spreading resistance or analytical analysis. This report describes the features of TERRY-2, the test structure designs, and the measurement procedures. The technique of charge pumping for measuring interface state density is discussed in an appendix.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

CCD; charge-coupled device; charge pumping; contact resistor; microelectronic test chip; sheet resistor; test chip; test pattern; test structure

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