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An NMOS Test Chip for a Course in Semiconductor Parameter Measurements

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
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Semiconductor Devices and Circuits Division
Washington, DC 20234

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AN NMOS TEST CHIP FOR A COURSE IN SEMICONDUCTOR PARAMETER MEASUREMENTS

K. P. Roenker and L. W. Linholm

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, ***Secretary***
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, ***Director***

TABLE OF CONTENTS

Page

Abstract 1

1. Introduction 1

2. Test Chip Layout and NMOS Process 1

3. Test Structure Descriptions 2
   A. Cross-Bridge Sheet Resistors 2
   B. Split Bridge Resistor Test Structure 3
   C. Misregistration Test Structures 3
   D. Contact Resistance Test Structures 5
   E. Dopant Profiling Measurements 6
   F. Gated Diode Test Structures 7
   G. Capacitance Measurements 8
   H. Mobility Measurements 8
   I. MOSFET Test Structures 8
   J. Circuit Elements 9

4. Summary 9

5. Acknowledgments 9

References 10

Appendix 42

LIST OF FIGURES

1. Test chip NBS-40 16
2. Cross section of an *n*-channel silicon gate enhancement MOSFET . . 17
Key to Photomask Levels 18
3a. Polysilicon cross-bridge resistor. 19
3b. Diffused cross-bridge resistor 20
3c. Metal cross-bridge resistor 21
4. Polysilicon split-bridge resistor 22
5a. Contact window-to-gate-window misregistration test structure . . . 23
5b. Metal-to-polysilicon misregistration test structure 24
6a. Polysilicon-to-gate-window misregistration test structure (NBS) . 25
6b. Polysilicon-to-gate-window misregistration test structure (Perloff) 26
6c. Polysilicon-to-gate-window misregistration test structure (Stickman) 27
7a. Six-terminal metal-to-diffusion contact resistor 28
7b. Six-terminal metal-to-polysilicon contact resistor 29
8. *n*-channel enhancement MOSFET for dopant profile determination . . 30
9a. Polysilicon gate capacitor 31
9b. Metal gate capacitor 32
10a. Gated diode 33
10b. Gated diode electrometer 34

List of Figures (continued)

Page

10c. Schematic drawing of the gated diode electrometer where GD is the gated diode, Q1 the reset switch, Q2 the source-follower, and R_L is the load resistor 35
11. *n*-channel enhancement MOSFET 36
12. Metal-gate, field oxide MOSFET (top) and polysilicon-gate field oxide MOSFET (bottom) 37
13a. *n*-channel enhancement MOSFET array 38
13b. *n*-channel depletion MOSFET array 39
14. Inverter stage 40
15. Ring oscillator 41

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ABSTRACT

This report describes an NMOS test chip, NBS-40, which was developed to be used in graduate level electronics engineering courses involving semiconductor parameter measurements associated with the fabrication of integrated circuits. The 35 test structures included in the test chip and their use in materials, device, and process parameter measurements are described. Details of the silicon gate NMOS process used in the chip fabrication are also provided.

Key words: integrated circuit; microelectronics; parameter measurements; solid-state electronics; test chip; test pattern; test structures.

1. INTRODUCTION

Semiconductor parameter measurements are used for the characterization of materials and devices, extraction of parameters for device and circuit simulation, and characterization and monitoring of integrated circuit processes associated with the fabrication of integrated circuits (ICs). The objective of this report is to describe an NMOS test chip which was developed to be used in electronics engineering courses involving semiconductor parameter measurements [1]. The test chip layout, the NMOS fabrication process used in its preparation, and the test structures and associated parameter measurements are described in this report.

2. TEST CHIP LAYOUT AND NMOS PROCESS

NBS-40 is a 3450-μm by 2760-μm test chip for a polysilicon gate NMOS fabrication process. The test chip contains 35 test structures which are configured in a 2 by 16 probe pad arrangement [2] with 80-μm probe pads located on 160-μm centers. Individual test structures are placed between the pads in the 2 by 16 column. The only exceptions to this placement are the MOS capacitor, ring oscillator, and inverter. The layout scheme permits convenient probing with one fixed probe card on a wafer prober, which may be computer controlled. The MOS capacitor is designed with larger probe pads for manual probing at a separate probe station. A complete list of test structures is given in the table; a layout of the chip is seen in figure 1.

The test chip was designed to be fabricated with a nine-photomask, polysilicon gate, self-aligned NMOS fabrication process. Three ion-implantation steps are used to adjust the threshold voltage of the depletion and enhancement mode Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and to form the sources and drains. In general, a minimum device design feature size of 5 μm was used. The NMOS process described in this report is similar to that employed elsewhere [3].

A cross section and top view of a MOSFET is seen in figure 2. To produce self-aligned MOSFETs and minimize overlap capacitance, a phosphorus source-drain diffusion is performed using an oversize polysilicon gate. A subsequent photomask defines the final gate size, and a phosphorus implant performed resulting in self-alignment and the desired shallow junction depth (0.3 μm). Details of the fabrication process are provided in the appendix.

3. TEST STRUCTURE DESCRIPTIONS

A. Cross-Bridge Sheet Resistors

Two phosphorus-diffused, one metal, and two polysilicon cross-bridge sheet resistor test structures are included in NBS-40 for the measurement of the sheet resistance and the determination of electrical linewidth for each of the conducting layers. The cross-bridge test structure, seen in figures 3a-3c, consists of a van der Pauw cross for sheet resistance determination merged with a bridge resistor for linewidth measurement. The structure has been analyzed numerically [4] and verified experimentally [5] to yield accurate sheet resistance measurements. Electrical measurement of the linewidth of a conducting layer using the bridge resistor has been described [6]. Each of the cross-bridges included in this test chip was configured to conform to the design rules found elsewhere [7-9] so that systematic geometry-related errors are minimized.

The sheet resistance of the conducting layer is measured by forcing a current I between probe pads A and B while the voltage drop V_R is sensed between probe pads E and F. The sheet resistance, R_s, is determined from

$$R_s = f \frac{\pi}{\ell n 2} \frac{V_R}{I}, \qquad (1)$$

where f is a correction factor, close to unity, that is related to the geometrical asymmetry of the structure. Repetition of the measurement on reversal of the current direction and rotation of the contacts by 90 deg can be made to determine the effects of geometrical asymmetry, measurement voltage offsets, and Joule heating on the measurement [5].

To determine the effective electrical linewidth W_e of a conducting layer, a current I is forced between probe pads A and C and the bridge resistor voltage V_w is sensed between probe pads D and E. The effective width is given by

$$W_e = \frac{R_s L_m}{R^*} = \frac{R_s L_m I}{V_w}, \qquad (2)$$

where R_s is the sheet resistance determined from the top of the cross bridge and L_m is the design length between the bridge voltage taps. Each cross-bridge resistor was designed with a bridge length, L_m, of 180 μm.

For the diffused or implanted cross bridges, the effective width W_e is related to the design photomask dimension W_m by

$$W_e = W_m + \alpha x_j \pm W_e , \tag{3}$$

where αx_j is the extent of increase in width due to lateral diffusion and W_e is the amount of oxide over or under etching and the offsets introduced by the photolithographic process [6]. For the metal and polysilicon cross bridges, the lateral diffusion term is omitted in eq (3) and W_e represents the over or under etching of the film and associated photolithographic offsets.

B. Split Bridge Resistor Test Structure

An extension of the cross-bridge resistor, termed the split cross bridge, has been proposed for the measurement of the linewidth, line-to-line spacing, and line-to-line pitch in conducting layers [10]. The structure, seen in figure 4, consists of a polysilicon cross-bridge resistor (W_b = 20 μm, L_b = 150 μm) with the bridge extended and split into two identical conducting channels, W_s (W_s = 5 μm), with a line-to-line spacing of S = 10 μm. The combined width, W_s', of the split portion of the bridge is determined by using cross-bridge eqs (2) and (3) in section A. The width of the split bridge elements, where $W_s' = 2 W_s$, is then subtracted from the width of the unsplit portion W_b to obtain the line spacing S

$$S = W_b - 2W_s . \tag{4}$$

The line pitch P is then determined by

$$P = S + W_s . \tag{5}$$

C. Misregistration Test Structures

The misregistration or misalignment between features on different photomask levels limits the packing density of circuits being manufactured. Errors due to misalignment of the photomask to the wafer, random and systematic alignment errors between the photomasks themselves, and distortions introduced during processing of the photomask and IC all contribute to a total misregistration error that may occur. At least three different misregistration test structures have been developed [11-13], and modified versions of each of three structures have been incorporated in this test chip.

Misregistration between the contact window and gate window photomasks is measured using a test structure similar to the one studied by Russell *et al.* [11] and is shown in figure 5a. The structure is analogous to a pair of linear potentiometers, one oriented vertically and the other horizontally.

The gate window photomask defines the two diffused resistors, joined together by the probe pad F. To measure misregistration, a current I is forced between pad B and pad G and the voltage between the four resistors measured. Perfect alignment of the contact window photomask positions the contact windows for the voltage taps (pads D and J) midway between pads C and E and H and I, respectively. For misregistration between the photomasks, the error in the vertical direction d_y is proportional to the difference between $V_{CD} = V_C - V_D$ and $V_{DE} = V_D - V_E$ and is

$$d_y = \frac{W}{2IR_s}\left(V_{DE} - V_{CD}\right) = \frac{L}{2}\,\frac{V_{DE} - V_{CD}}{V_{AC}} . \tag{6}$$

Similarly, in the horizontal direction the misregistration d_x is

$$d_x = \frac{L}{2}\,\frac{V_{JI} - V_{HJ}}{V_{AC}} . \tag{7}$$

The results are usually displayed in the form of a vector map and can be analyzed to determine the sources of the misregistration error [13-15,17].

An analogous structure for measuring misalignment between the metal and final polysilicon photomasks is seen in figure 5b. The contact windows have been enlarged along the length of the resistors in both cases, while the overlapping metal has been narrowed so that the misregistration of the metal photomask rather than the contact window photomask is sensed. The method of measurement is the same as for the previous structure.

Figures 6a, b, and c show three different test structures incorporated in NBS-40, each designed to measure misregistration between the final polysilicon photomask and the gate window photomask. The final structure, seen in figure 6a, is a modification of that seen in figure 5a. The position of the voltage taps (which are connected to pads D and J) are determined by the alignment of the final polysilicon photomask. The same fabrication technique is used to construct the misregistration structure seen in figure 6b following the approach developed by Perloff [12,16,17]. The location of the oversize polysilicon photomask and the final level polysilicon photomask determines the position of the voltage taps. To determine misregistration, a current I is forced between pad E and pad F and the voltage measured between voltage taps C and B and B and D. The misregistration in the horizontal direction is

$$d_x = 0.3159\ \alpha \arcsin \frac{V_{CB} - V_{BD}}{V_{CB} + V_{BD}} , \tag{8}$$

where α = 40 µm is the width of the body of the structure, $V_{CB} = V_C - V_B$, and $V_{BD} = V_B - V_D$. Similarly, misregistration in the vertical direction is

$$d_y = 0.3159\ \alpha \arcsin \frac{V_{CA} - V_{AE}}{V_{CA} + V_{AE}} . \tag{9}$$

The structure also provides for sheet resistance determination from the four voltage differences measured above and the current as given by

$$\rho_s = \frac{\pi}{\ln 2} \frac{V_{CB} + V_{BD} + V_{CA} + V_{AE}}{2I} . \qquad (10)$$

A third misregistration test structure designed to measure misregistration between the same two photomask levels as the previous two structures is the Stickman-type structure seen in figure 6c. The structure is a modification of that of Nicholas *et al.* [15,18] in which the current taps and voltage taps are separated in order to provide a four-terminal or Kelvin measurement of resistance. For this design, a long blocking bar on a second photomask is aligned with a larger rectangle on the first photomask level to form two parallel and narrow resistors of equal size for no misregistration. The blocking bar is the final size polysilicon that is aligned with the larger, rectangular gate window opening. The subsequent source-drain implant then forms the two identical resistors. This structure and an identical structure rotated by 90 deg can be used to measure the misregistration between polysilicon and gate window in both the x- and y-directions.

The measurement and analysis is similar to that of the previous misregistration structures. A current I is forced between pad A and pad B while the voltage drops between probe pads F and E and C and D along the bridge resistors are sensed. The displacement in the y-direction is given by

$$d_y = \frac{I\rho_s L}{2} \left(V_{FE}^{-1} - V_{CD}^{-1}\right) , \qquad (11)$$

where L = 160 μm, ρ_s is the sheet resistance obtained from an adjacent cross-bridge structure, and $V_{FE} = V_F - V_E$, and $V_{CD} = V_C - V_D$. Similarly, the x misregistration component is given by

$$d_x = \frac{I\rho_s L}{2} \left(V_{GI}^{-1} - V_{JH}^{-1}\right) . \qquad (12)$$

The availability of the three polysilicon-to-gate-window misregistration structures located immediately adjacent to one another provides the opportunity for a close comparison of the three structures and associated measurement methods.

D. Contact Resistance Test Structures

The six contact resistor test structures [19,20] were incorporated in the NBS-40 test chip to measure interfacial contact resistance $R_c(\Omega)$ for the metal-to-diffusion and metal-to-polysilicon contacts. Three test structures of each type with square contacts of 5, 10, and 20 μm on a side were included in the test chip. A metal-to-diffusion and a metal-to-polysilicon contact resistor test structure with a design 100-μm^2 contact window area can be seen in figures 7a and 7b, respectively. The six-terminal structure [19] allows measurement in the interfacial contact resistance and the "end" contact resistance and the subsequent calculation of the "front" contact resistance

using the transmission line formulation of Berger [21]. The structure and measurement method were designed to minimize the influence of parasitic resistances and contact-to-diffusion misalignment on the result. For a current I forced beween pad A and pad E, the ratio of the voltage difference between pads C and F to the current gives the interfacial contact resistance [22]. Similarly, the ratio of the voltage difference between pads D and F to the current gives the end contact resistance. Uniformity in the interfacial layer can be estimated by using all three structures of the same type, since the interfacial contact resistance is expected to be inversely proportional to the contact window area for a uniform contact layer [22]. The specific contact resistance $\rho_c (\Omega \cdot cm^2)$, for a uniform interfacial layer, the ratio of the voltage drop across the interface to the current density through it, can be calculated from

$$R_c = \rho_c / A \, . \tag{13}$$

E. Dopant Profiling Measurements

A large, -channel silicon gate MOSFET, seen in figure 8, was included for profiling the boron threshold adjust implant using a dc current measurement technique. For the device operating in the linear region at a fixed drain-source voltage, the gate-to-source bias, V_{GS}, is adjusted to obtain a predetermined current level. Subsequently, as V_{GS} is changed, the back gate bias, V_{SB}, is adjusted to maintain a constant drain current. The dopant profile N(W) can be determined by

$$N(W) = \frac{C_{ox}^2}{qK_s} \left(\frac{d^2 V_{SB}}{dV_{GS}^2} \right)^{-1} \tag{14}$$

for the depth W

$$W = \frac{K_s}{C_{ox}} \left(\frac{dV_{SB}}{dV_{GS}} \right) , \tag{15}$$

where C_{ox} is the gate oxide capacitance per unit area, K_s is the relative permittivity of silicon, V_{GS} is the gate-to-source voltage, and V_{SB} is the back gate bias. In general, profiles determined by this technique are limited to distances from the surface greater than three times the Debye length for the material [23]. Further description of the measurement technique and analysis is found elsewhere [23-27]. The design dimensions for the MOSFET gate are L = 10 μm and W = 440 μm. A polysilicon gate capacitor, see figure 9a, has been included on the chip to permit experimental determination of the oxide capacitance per unit area C_{ox} (area = 2.94×10^5 μm^2) of the gate oxide region. The metal gate capacitor, see figure 9b, (area = 7.35×10^5 μm^2) can be used to determine the field oxide thickness.

The boron enhancement implant can be profiled from the polysilicon gate MOS capacitor using the capacitance-voltage measurement [28,29]. For lightly

doped substrates, the effect of series resistance on the measurement should be considered [30].

For the C-V technique, the dopant concentration N(W) can be determined by

$$N(W) = \left[qK_s \frac{1}{C_m} \frac{d}{dV_{GS}} \left(\frac{1}{C_m}\right)\right]^{-1} , \tag{16}$$

for a depth

$$W = K_s \left[\frac{1}{C_m} - \frac{1}{C_{ox}}\right] , \tag{17}$$

where C_m is the capacitance measured in depletion at a gate bias V_{GS}. The limitations of the C-V method are described in detail by Nicollian and Brews [29].

F. Gated Diode Test Structures

Both a gated diode [31,32] and a gated diode electrometer [33,34], seen in figures 10a and 10b, respectively, have been included in the test chip for measurement of generation lifetime and surface leakage current. In the former, direct measurements of the low, reverse leakage current of the *p-n* junction under various biases on the MOS gate are used to separate the bulk, the surface depletion region, and the interface generation components. For the first component, an associated bulk generation lifetime τ_G can be derived using

$$\tau_G = \frac{qn_i W A_{MJ}}{2I_G} , \tag{18}$$

where q is the electronic charge, n_i is the intrinsic carrier concentration, I_G is the reverse leakage current of the junction for the surface region in accumulation, W is the junction depletion width, and A_{MJ} is the junction surface area ($A_{MJ} = 5.52 \times 10^4\ \mu m^2$).

When the surface under the MOS gate is inverted, the reverse leakage current consists of two components: I_G, and the current I_{GI} due to the induced depletion region under the gate. The generation lifetime in the vicinity of the surface, τ_s, can then be obtained from

$$\tau_s = \frac{qn_i W_I A_I}{2I_{GI}} , \tag{19}$$

where A_I is the area under the gate ($A_I = 8.21 \times 10^3\ \mu m^2$) and W_I is the depletion width of the field-induced depletion region.

A gated diode electrometer is included in the test chip. The gated diode previously described is incorporated into this structure. The electrometer is intended to reduce off-chip loading effects encountered in gated diode

measurements. A schematic circuit diagram for the electrometer is seen in figure 10c where a MOSFET operating in the saturated mode is used as the load resistor R_L.

To analyze the measured dV_o/dt output of the electrometer, the *p-n* junction capacitance C, gate-source capacitance C_{GS}, load resistance R_L, and transconductance g_m of the source follower transistor are needed. The junction capacitance C can be estimated using the known junction area given above and substrate doping or measured directly on the gated diode. The gate-source capacitance can only be estimated from the known geometry of the self-aligned MOSFET (W = L = 20 µm), oxide thickness, and gate-source overlap nominally the source-drain implant junction depth. The transconductance g_m of the enhancement MOSFET can be obtained directly from measurement on an identical MOSFET (W = L = 20 µm) in column 1 of the chip. The saturated MOSFET used as the load resistor R_L can be measured directly between pads C and E of the electrometer to obtain R_L.

G. Capacitance Measurements

The polysilicon gate capacitor (see fig. 9a) can be used to determine the gate oxide capacitance per unit area, gate oxide thickness, and flat band capacitance and voltage from C-V measurements. It can also be used to determine Debye length [35], mobile ion density [36], oxide fixed charge [37], and interface trap density [38]. The generation lifetime can be measured using a transient capacitance technique [39] or a modified linear sweep technique [40,41].

H. Mobility Measurements

An enlarged (W = 240 µm, L = 35 µm) silicon gate MOSFET seen in figure 11 was included to measure the electron inversion layer mobility in the *n*-channel enhancement MOSFETs. The effective electron mobility is obtained from the dc drain conductance g_d measured in the linear region [42] using

$$\mu_{eff} = \frac{(L/W)\, g_d}{q\, N_{inv}}, \qquad (20)$$

where W and L are the design MOSFET channel width and length, and $q\, N_{inv}$ is the total induced charge in the channel per unit area. This relation is only valid for long-channel devices. By employing a large MOSFET, errors in determining actual device geometries are minimized. The determination of μ_{eff} using this approach does require that the gate capacitance per unit area be obtained from the silicon gate capacitor. The degradation of the mobility with increasing gate voltage [42,43] can be quantified using this measurement.

I. MOSFET Test Structures

A metal gate thick oxide MOSFET and a polysilicon gate thick oxide MOSFET, seen in figure 12, with W = L = 30 µm are included in the test chip for field threshold voltage determination. The silicon gate MOSFET will provide the threshold voltage for the polysilicon over the thermally grown field oxide;

the metal gate will provide the threshold voltage of the metal over the total field oxide which consists of the thermally grown field oxide and the oxide deposited over the polysilicon.

Two sets of silicon gate MOSFETs seen in figures 13a and b are included. One set consists of enhancement devices with fixed width (W = 20 μm) and differing lengths (L = 2.0 μm, 5.0 μm, 10 μm, and 20 μm). The other set consisting of depletion devices has a fixed length (L = 50 μm) and varying widths (W = 2.0 μm, 5.0 μm, 10 μm, and 20 μm). The set of enhancement devices can be used to electrically estimate the effective channel length [42,43] and to determine the total source, drain, and contact resistance [45].

The measurement of MOSFET parameters such as threshold voltage, transconductance, drain resistance, body effect, channel length modulation, breakdown, interface trapped charge, etc., are described in a number of publications [42,48-52].

J. Circuit Elements

An inverter seen in figure 14 consisting of an enhancement driver with W = 20 μm, L = 10 μm and a depletion load with W = 10 μm, L = 50 μm is included. Measurement of the static transfer characteristic of the inverter can be used to obtain the logic level voltages and noise margins. A ring oscillator consisting of 19 inverter stages with a NAND startup and a four-stage, separately powered output buffer [53] is seen in figure 15. Both the propagation delay and power dissipation per stage can be determined. Also, the ring oscillator can be used to evaluate the sensitivity of circuit codes to process-induced variations in input parameters [54]. The initial stage of the output buffer is the same inverter used in the ring. Each subsequent stage has the channel width of both the driver and load enlarged by a factor of three over the previous stage so that load capacitance of 20 pF can be driven without an excessive propagation time penalty [55].

4. SUMMARY

An NMOS test chip has been described that includes 35 test structures for the measurement of a variety of device, fabrication process, and circuit parameters associated with the fabrication of ICs. In general, the test structures and measurement methods described assume long-channel device characteristics. Structure layout, the method of parameter measurement, and references to the literature are provided for each structure.

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REFERENCES

1. Roenker, K. P., A Graduate Laboratory in Semiconductor Parametric Measurements, *Proc. 5th Biennial University/Government/Industry Microelectronics Symposium,* May 25-29, 1983, pp. 94-99.

2. Buehler, M. G., Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-Pad Array Approach, *Solid State Technology* 22, 89-94 (1979).

3. Ogura, S., *et al.,* Design and Characteristics of the Lightly Doped Drain Source (LDD) Insulated Gate Field Effect Transistor, *IEEE Trans. Electron Devices* ED-27, 1359-1367 (1980).

4. David, J. M., and Buehler, M. G., A Numerical Analysis of Various Cross Sheet Resistor Test Structures, *Solid State Electronics* 20, 539-543 (1977).

5. Buehler, M. G., and Thurber, W. R., An Experimental Study of Various Cross Sheet Resistor Test Structures, *J. Electrochem. Soc.* 125, 645-650 (1978).

6. Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Linewidth of Conducting Layers, *J. Electrochem. Soc.* 125, 650-654 (1978).

7. Yen, D., Linholm, L. W., and Buehler, M. G., A Cross Bridge Test Structure for Evaluating the Linewidth Uniformity of an Integrated Circuit Lithography System, *J. Electrochem. Soc.* 129, 2313-2318 (1982).

8. Carver, G. P., Mattis, R. L., and Buehler, M. G., Design Considerations for the Cross-Bridge Sheet Resistor, NBSIR 82-2548 (July 1982), pp. 1-18.

9. Hall, P. M., Resistance Calculations for Thin Film Patterns, *Thin Solid Films* 7, 277-295 (1967/68).

10. Buehler, M. G., Griswold, T. W., Pinn, C. A., Blaes, D. R., Timoc, C., Nixon, R. H., and Suszko, S., Product Assurance Technology for Procuring Reliable, Custom, LSI/VLSI Electronics, JPL Publication No. 83-70, Oct. 1983.

11. Russell, T. J., Leedy, T. F., and Mattis, R. L., A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing, *Tech. Digest, International Electron Devices Meeting,* Washington, D.C., December 5-7, 1977, pp. 7A - 7F.

12. Perloff, D. S., A Four-Point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafers, *IEEE J. Solid State Circuits* SC-13, 436-444 (1978).

13. Stemp, I. J., Nicholas, K. H., and Brockman, H. E., Automatic Testing and Analysis of Misregistrations Found in Semiconductor Processing, *IEEE Trans. Electron Devices* ED-26, 729-732 (1979).

14. Matsuzawa, T., Sunami, H., and Hashimoto, N., Analysis of Superposition Errors in Wafer Fabrication, *Microelect. and Reliab.* 16, 173-176 (1977).

15. Nicholas, K. H., Stemp, I. J., and Brockman, H. E., Measurement and Identification of Distortion, Alignment and Mask Errors in IC Processing, *J. Electrochem. Soc.* 128, 609-614 (1981).

16. Hasan, T. L., Katzman, S. U., and Perloff, D. S., Automated Electrical Measurements of Registration Errors in Step-and-Repeat Optical Lithography Systems, *IEEE Trans. Electron Devices* ED-27, 2304-2313 (1980).

17. Perloff, D. S., A van der Pauw Resistor Structure for Determining Mask Superposition Errors on Semiconductor Slices, *Solid State Electronics* 21, 1013-1018 (1978).

18. Nicholas, K. H., and Tree, R. J., The Electrical Measurement of Pattern Placement Errors of Mask Makers, *J. Electrochem. Soc.* 129, 1800-1802 (1982).

19. Proctor, S. J., Linholm, L. W., and Mazer, J. A., Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity, *IEEE Trans. Electron Devices* ED-30, 1535-1542 (1983).

20. Mazer, J. A., Linholm, L. W., Pramanik, D., Tsai, S., and Saxena, A. N., Effects of Phosphorus Contact Doping and Sheet Resistance Variations on Al/Si Interfacial Contact Resistance, *Proc. 1983 Custom Integrated Circuits Conf.*, Rochester, New York, May 23-25, 1983, pp. 291-294.

21. Berger, H. H., Models for Contacts to Planar Devices, *Solid State Electronics* 15, 145-158 (1972).

22. Proctor, S. J., and Linholm, L. W., A Direct Measurement of Interfacial Contact Resistance, *IEEE Electron Devices Lett.* EDL-3, 294-296 (1982).

23. Buehler, M. G., The DC MOSFET Dopant Profile Method, *J. Electrochem. Soc.* 127, 701-704 (1980).

24. Shannon, J. M., DC Measurement of the Space Charge Capacitance and Impurity Profile Beneath the Gate of an MOST, *Solid State Electronics* 14, 1099-1106 (1971).

25. Buehler, M. G., Effect of the Drain-Source Voltage on Dopant Profiles Obtained from the DC MOSFET Profile Method, *IEEE Trans. Electron Devices* ED-27, 2273-2277 (1980).

26. Carver, G. P., Influence of Short-Channel Effects on Dopant Profiles Obtained from the DC MOSFET Profile Method, *IEEE Trans. Electron Devices* ED-30, 948-954 (1983).

27. Balasubramanian, C. S., and Jayakumar, V., Estimation of Doping Profiles in Short Channel MOSFETs Using DC Measurements, *IEEE Electron Devices Lett.* EDL-3, 250-253 (1982).

28. Nicollian, E. H., and Brews, J. R., *MOS Physics and Technology* (Wiley-Interscience, New York, 1982), pp. 222-226, 380-406.

29. Gordon, B. J., On-Line Capacitance-Voltage Doping Profile Measurement of Low Dose Ion Implants, *IEEE Trans. Electron Devices* ED-27, 2268-2272 (1980).

30. Wiley, J. D., and Miller, G. L., Series Resistance Effects in Semiconductor CV Profiling, *IEEE Trans. Electron Devices* ED-22, 265-272 (1975).

31. Grove, A. S., *Physics and Technology of Semiconductor Devices* (Wiley, New York, 1967), pp. 296-305.

32. Van der Spiegel, J., and Declerck, G. J., Theoretical and Practical Investigation of the Thermal Generation in Gate Controlled Diodes, *Solid State Electronics* 24, 869-877 (1981).

33. Carver, G. P., and Buehler, M. G., An Analytical Expression for the Evaluation of Leakage Current in the Integrated Gated-Diode Electrometer, *IEEE Trans. Electron Devices* ED-27, 2245-2252 (1980).

34. Carver, G. P., Linholm, L. W., and Russell, T. J., Use of Microelectronic Test Structures to Characterize IC Materials, Processes, and Processing Equipment, *Solid State Technology* 23, 85-92 (1980).

35. Lehovec, K., Rapid Evaluation of C-V Plots for MOS Structures, *Solid State Electronics* 11, 135-137 (1968).

36. Snow, E. H., *et al.*, Ion Transport in Insulating Films, *J. Appl. Phys.* 36, 1664-1672 (1965).

37. Reference 28, 425-429.

38. Reference 28, 325-333.

39. Rabbani, K. S., and Lamb, D. R., Direct Correlation of Generation Lifetimes Obtained from Pulsed MOS Capacitance and Gated Diode Measurements, *Solid State Electronics* 26, 161-168 (1983).

40. Pierret, R. F., and Small, D. W., A Modified Linear Sweep Technique for MOS-C Generation Rate Measurements, *IEEE Trans. Electron Devices* ED-22, 1051-1052 (1975).

41. Small, D. W., and Pierret, R. F., Separation of Surface and Bulk Components in MOS-C Generation Rate Measurements, *Solid State Electronics* 19, 505-511 (1976).

42. Sun, S. C., and Plummer, J. D., Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces, *IEEE Trans. Electron Devices* ED-27, 1497-1508 (1980).

43. Fang, F. F., and Fowler, A. B., Transport Properties of Electrons in Inverted Silicon Surfaces, *Phys. Rev.* 169, 619-631 (1968).

44. Chern, J. G. J., Chang, P., Motta, R. F., and Godinho, N., A New Method to Determine MOSFET Channel Length, *IEEE Electron Device Lett.* EDL-1 170-173 (1980).

45. Terada, K., and Muta, H., A New Method to Determine Effective MOSFET Channel Length, *Jpn. J. Appl. Phys.* 18, 953-959 (1979).

46. Ma, Y. R., and Wang, K. L., A New Method to Electrically Determine Effective Channel Width, *IEEE Trans. Electron Devices* ED-29, 1825-1827 (1982).

47. Suciu, P. I., and Johnston, R. L., Experimental Derivation of the Source and Drain Resistance of MOS Transistors, *IEEE Trans. Electron Devices* ED-27, 1846-1848 (1980)

48. Penney, W. M., and Lau, L., *MOS Integrated Circuits* (Krieger, New York, 1979), pp. 72-129.

49. Hodges, D. A., and Jackson, H. G., *Analysis and Design of Digital Integrated Circuits* (McGraw-Hill, New York, 1983), pp. 43-59.

50. Sze, S. M., *Physics of Semiconductor Devices* (Wiley, New York, 1981), pp. 446-448.

51. Brugler, J. S., and Jespers, P. G. A., Charge Pumping in MOS Devices, *IEEE Trans. Electron Devices* ED-16, 297-302 (1969).

52. Russell, T. J., Wilson, C. L., and Gaitan, M., Determination of the Spatial Variation of Interface Trapped Charge Using Short-Channel MOSFETs, *IEEE Trans. Electron Devices* ED-30, 1662-1671 (1983).

53. Buehler, M. G., Microelectronic Test Chip for VLSI Electronics, *VLSI Electronics: Microstructural Science*, Vol. 6, pp. 529-576 (Academic Press, New York, 1983).

54. Cassard, J. M., A Sensitivity Analysis of SPICE Parameters Using an Eleven-Stage Ring Oscillator, joint special issues of *IEEE J. Solid State Circuits* SC-19, 130-135 and *IEEE Trans. Electron Devices* ED-31, 264-269 (February 1984).

56. Lin, H. C., and Linholm, L. W., An Optimized Output Stage for MOS Integrated Circuits, *IEEE J. Solid State Circuits* SC-10, 106-109 (1975).

TABLE

Test Chip NBS-40

Device #	Test Structure	Parameters Determined
1.	Enhancement MOSFET array with W = 20 μm, L = 2.0, 5.0, 10, 20 μm	threshold voltage, transconductance, effective channel length and width
2.	Depletion MOSFET array with L = 50 μm, W = 2.0, 5.0, 10, 20 μm	
3.	Polysilicon cross bridge, W = 10 μm, L = 180 μm	polysilicon sheet resistance, linewidth
4.	Polysilicon cross bridge, W = 5 μm, L = 180 μm	polysilicon sheet resistance, linewidth
5.	Metal cross bridge, W = 10 μm, L = 180 μm	metal sheet resistance, linewidth
6.	Contact window to gate window misregistration (NBS) L = 160 μm	misregistration between contact window and gate window
7.	MOSFET L = 10 μm, W = 440 μm	dopant profile
8.	Polysilicon-to-gate window misregistration (Perloff) α = 40 μm	misregistration between final polysilicon and gate window
9.	Polysilicon-to-gate window misregistration (NBS) L = 160 μm	misregistration between final polysilicon and gate window
10.	Split cross-bridge resistor	line-to-line spacing between conductors, line-to-line pitch
11.	Polysilicon-to-gate window misregistration (Stickman) L = 160 μm	misregistration between final polysilicon and gate window
12.	n^+ diffused cross bridge, W = 10 μm, L = 180 μm	n^+ sheet resistance, linewidth
13.	n^+ diffused cross bridge, W = 5 μm, L = 180 μm	n^+ sheet resistance, linewidth

Device #	Test Structure	Parameters Determined
14.	Metal-to-polysilicon misregistration (NBS) $L = 160\ \mu m$	misregistration between metal and and polysilicon
15.	Metal-polysilicon contact resistance, 20-μm square contact	interfacial, front, and end contact resistance, interfacial layer uniformity
16.	Metal-polysilicon contact resistance, 10-μm square contact	"
17.	Metal-polysilicon contact resistance, 5-μm square contact	"
18.	Metal and polysilicon gate field oxide MOSFETs with $W = L = 30\ \mu m$	field threshold voltage
19.	Gated diode $A_{MJ} = 5.52 \times 10^4\ \mu m^2$ $A_I = 8.21 \times 10^3\ \mu m^2$	generation lifetime, surface leakage current
20.	Metal-n^+ contact resistance, 20-μm square contact	interfacial, front, and end contact resistance, interfacial layer uniformity
21.	Metal-n^+ contact resistance, 10-μm square contact	"
22.	Metal-n^+ contact resistance, 5-μm square contact	"
23.	Gated diode electrometer	generation lifetime, surface leakage current
24.	Enhancement MOSFET $W = 240\ \mu m$, $L = 35\ \mu m$	inversion layer mobility
25.	Polysilicon gate MOS capacitor $A = 2.94 \times 10^5\ \mu m^2$	oxide thickness, dopant profile, oxide charge
26.	Seventeen-stage ring oscillator with output buffer	propagation delay, power dissipation
27.	Single-stage inverter of ring oscillator, driver $W = 20\ \mu m$, $L = 10\ \mu m$ load $W = 10\ \mu m$, $L = 50\ \mu m$	transfer characteristic, voltage levels, noise margins
28.	Metal gate capacitor $A = 7.35 \times 10^5\ \mu m^2$	oxide thickness, dopant profile, oxide charge

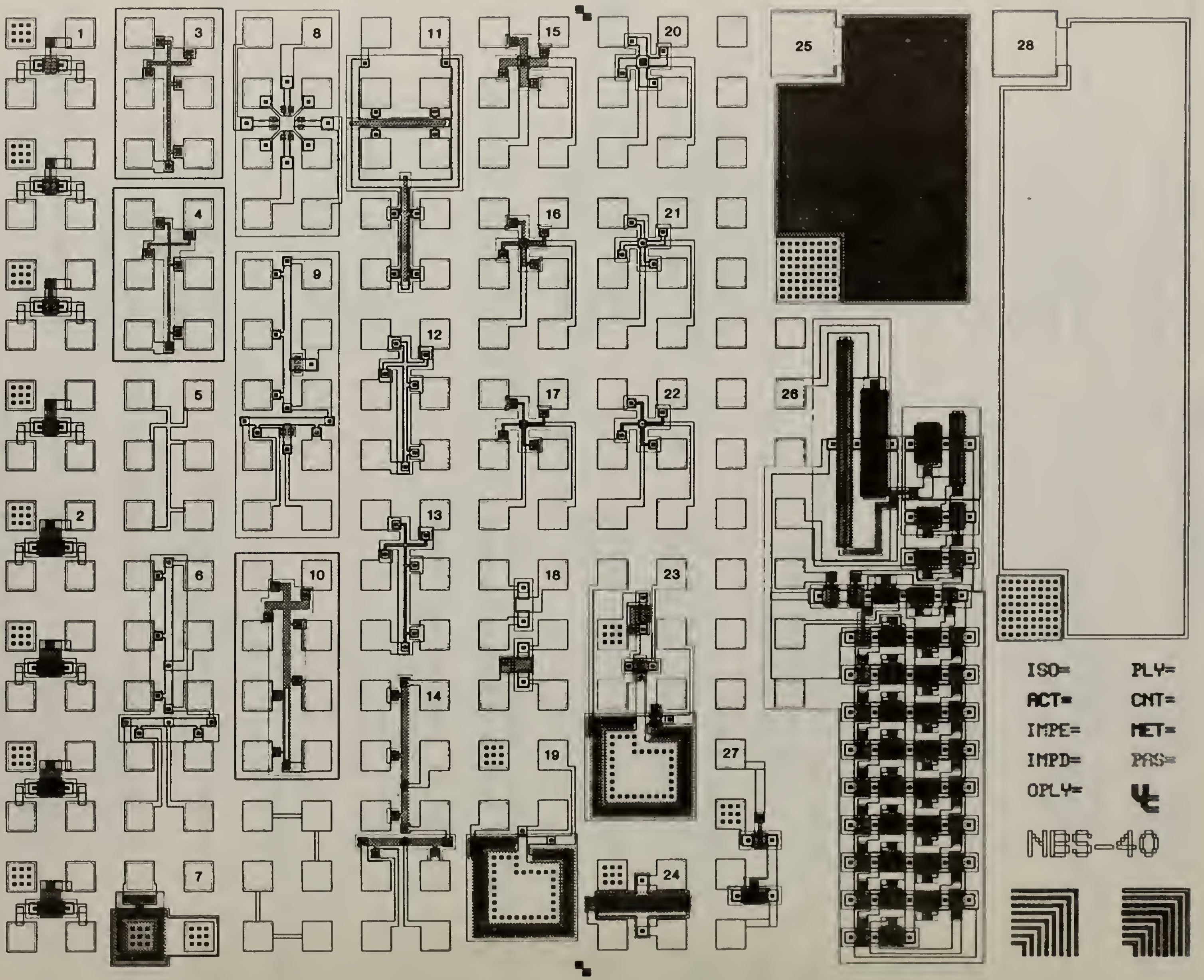
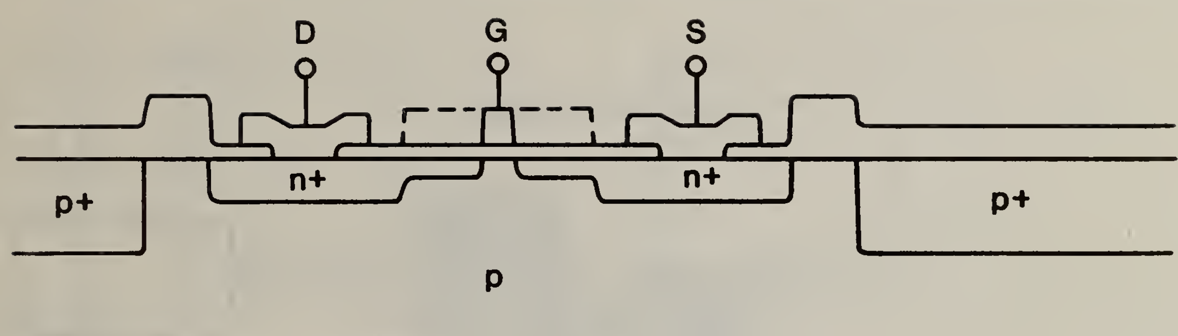


Figure 1. Test chip NBS-40.



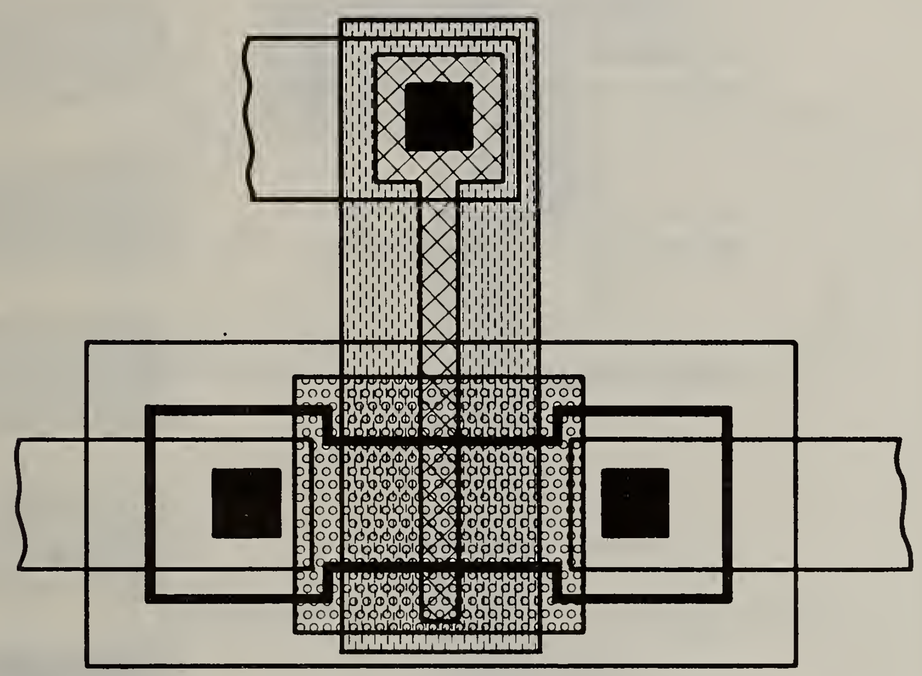


Figure 2. Cross section of an n-channel silicon gate enhancement MOSFET.

Key to Photomask Levels

Photomask Level	Description	Symbol
1	p^+ isolation diffusion	
2	gate window	
3	enhancement threshold adjust implant (boron)	
4	depletion threshold adjust implant (phosphorus)	
5	oversize polysilicon	
6	final size polysilicon	
7	contact window	
8	aluminum metallization	
9	passivation	

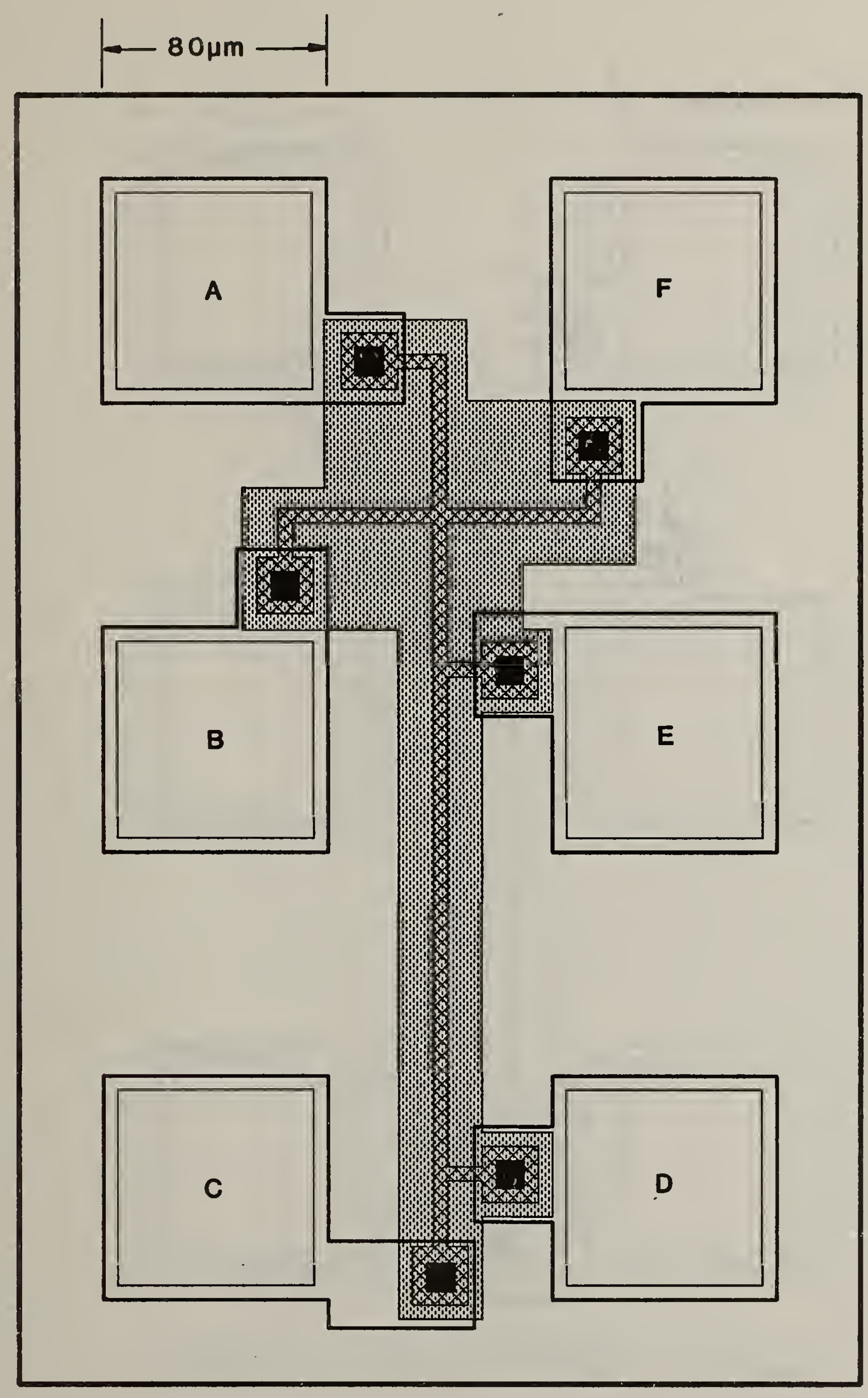


Figure 3a. Polysilicon cross-bridge resistor.

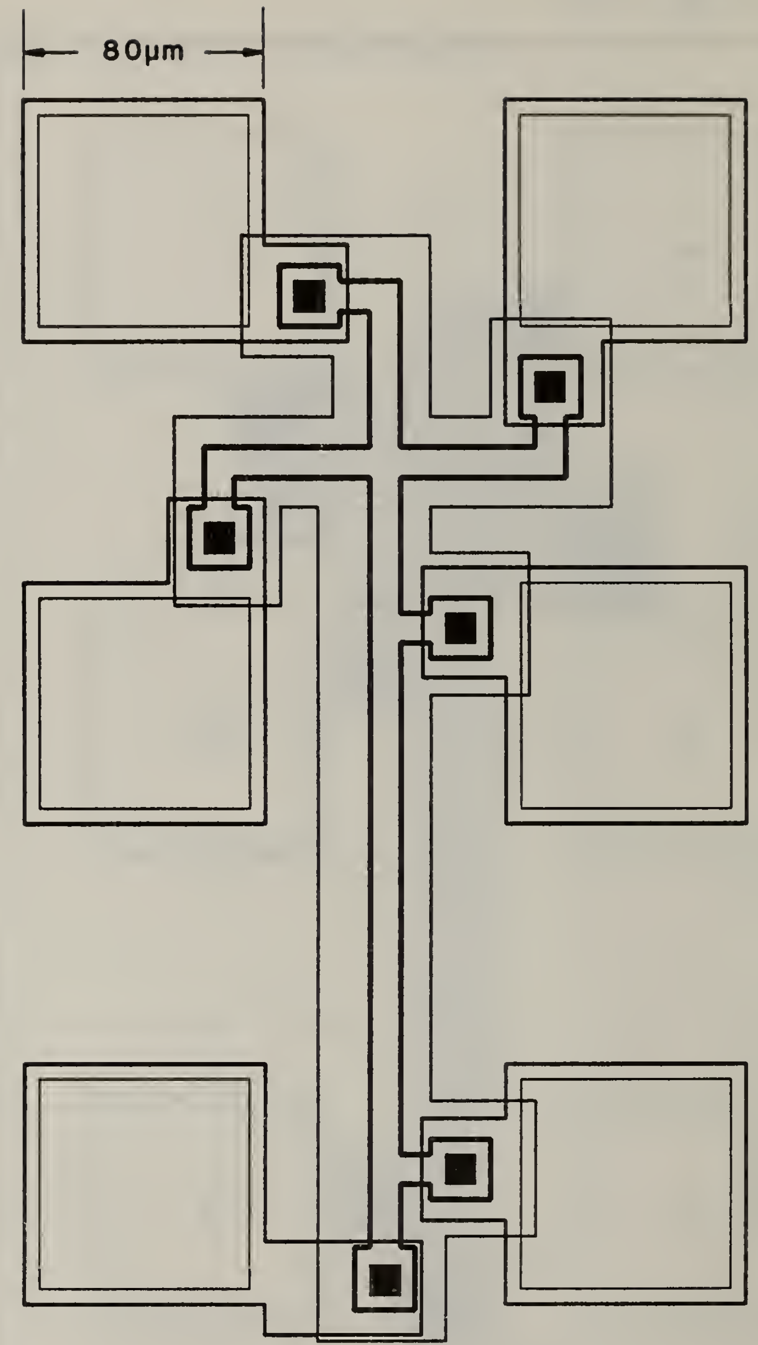


Figure 3b. Diffused cross-bridge resistor.

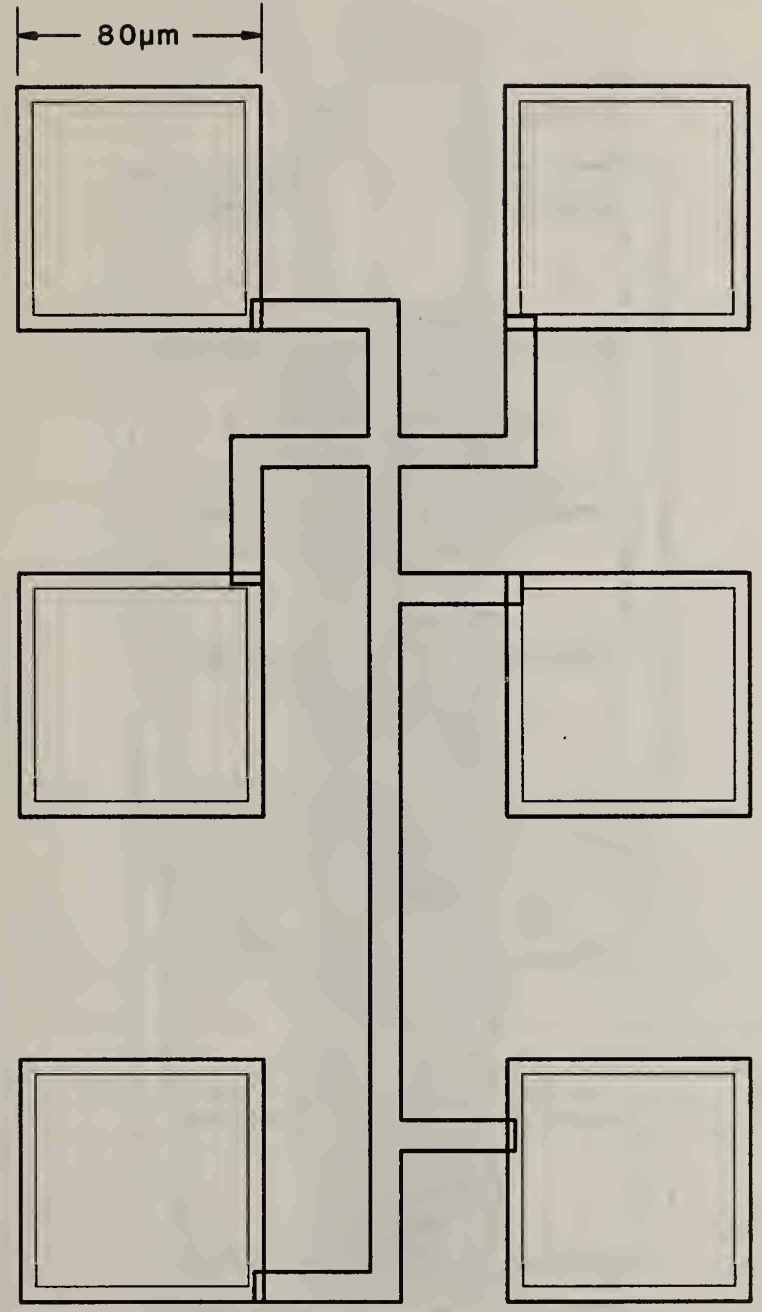


Figure 3c. Metal cross-bridge resistor.

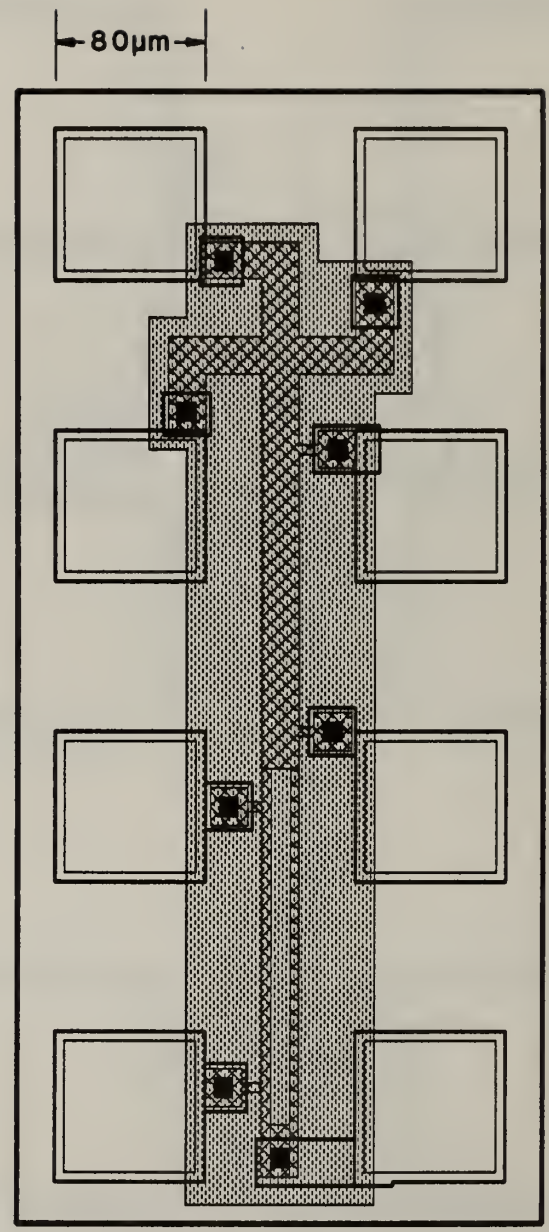


Figure 4. Polysilicon split-bridge resistor.

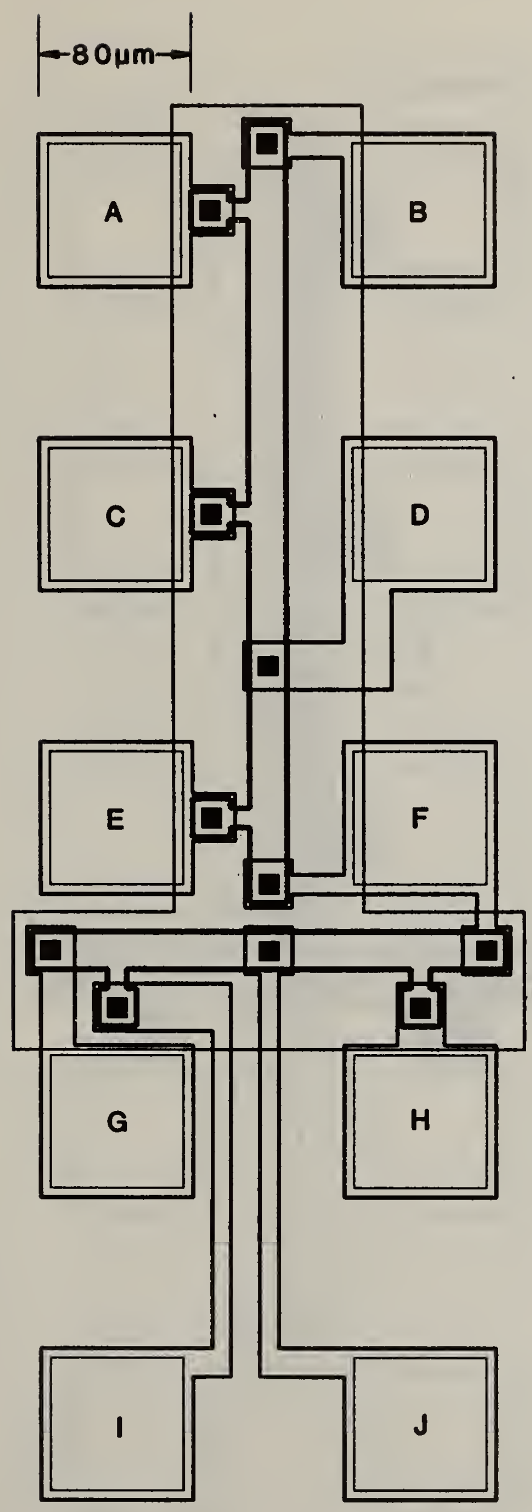


Figure 5a. Contact window-to-gate-window misregistration test structure.

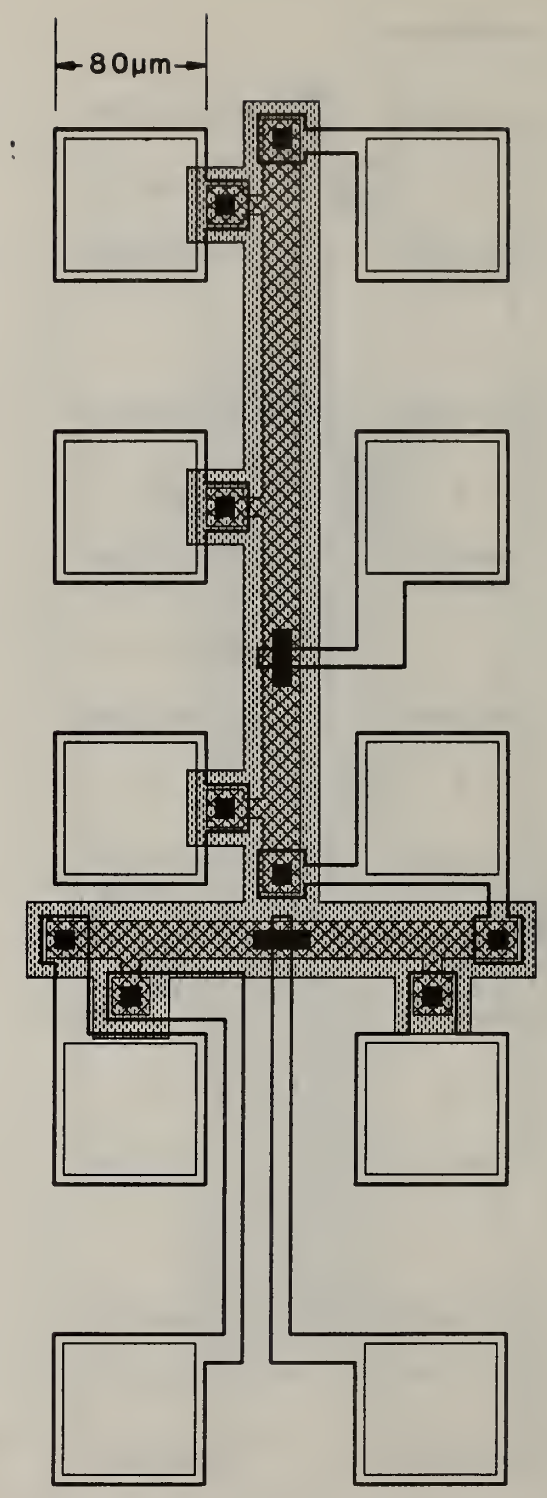


Figure 5b. Metal-to-polysilicon misregistration test structure.

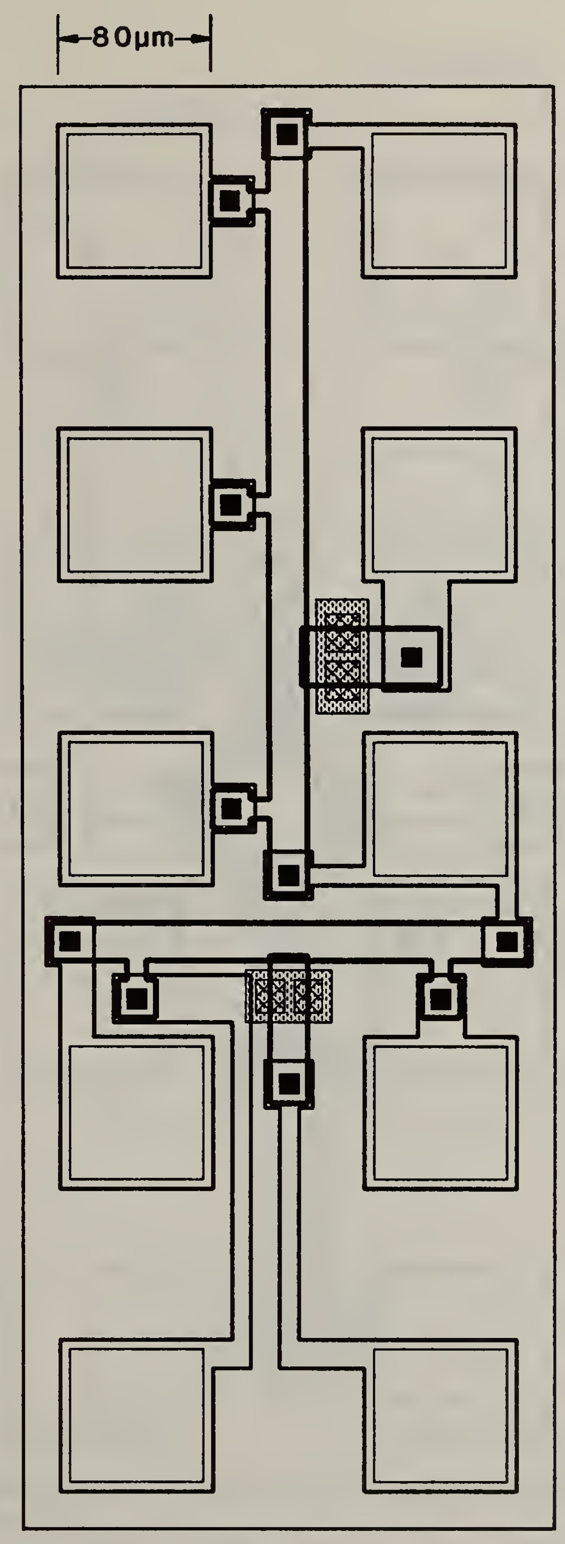


Figure 6a. Polysilicon-to-gate-window misregistration test structure (NBS).

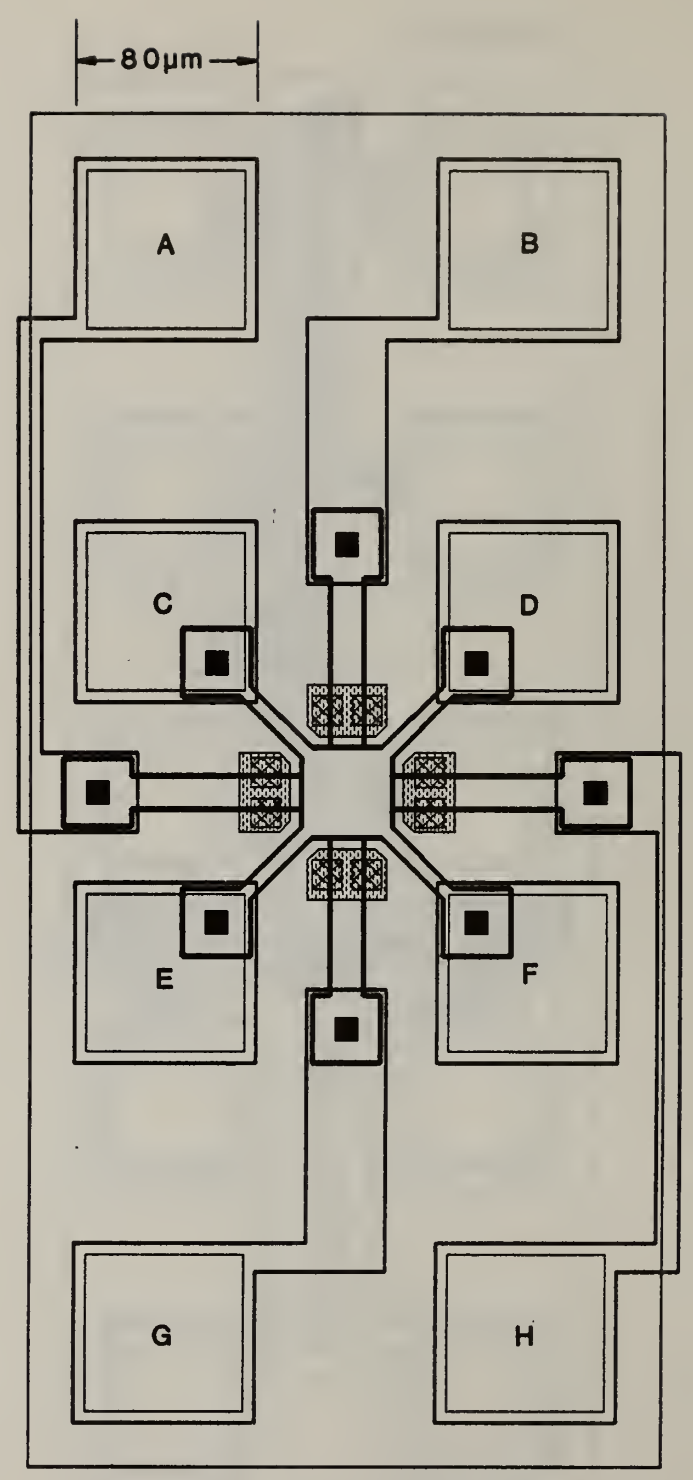


Figure 6b. Polysilicon-to-gate-window misregistration test structure (Perloff).

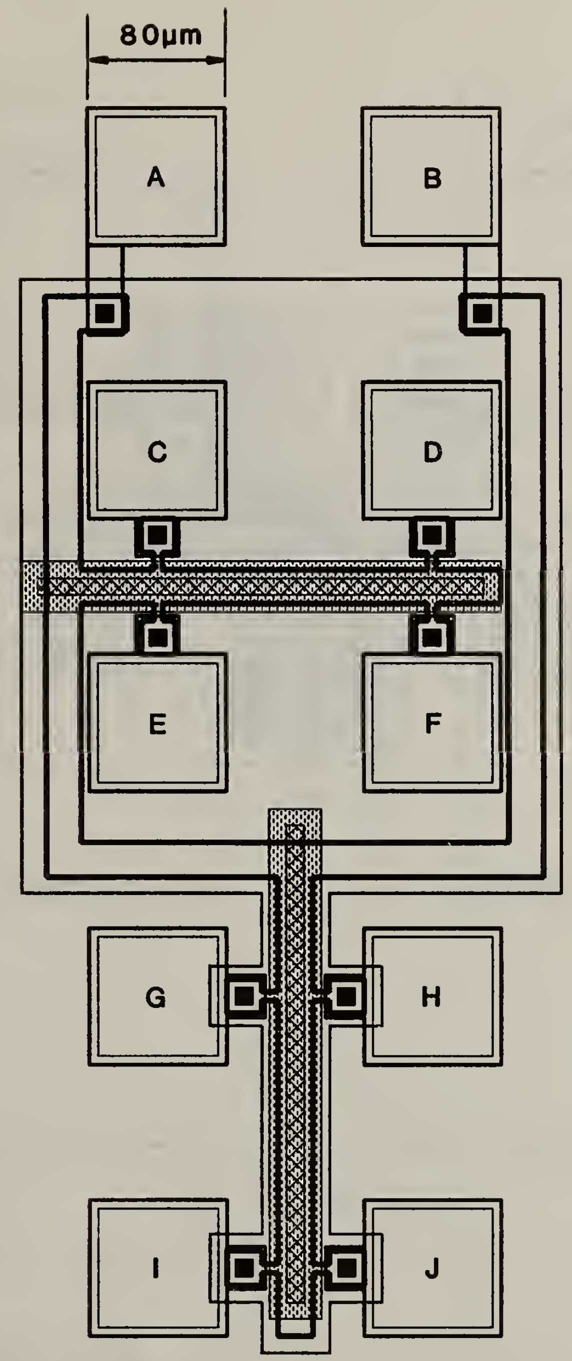


Figure 6c. Polysilicon-to-gate-window misregistration test structure (Stickman).

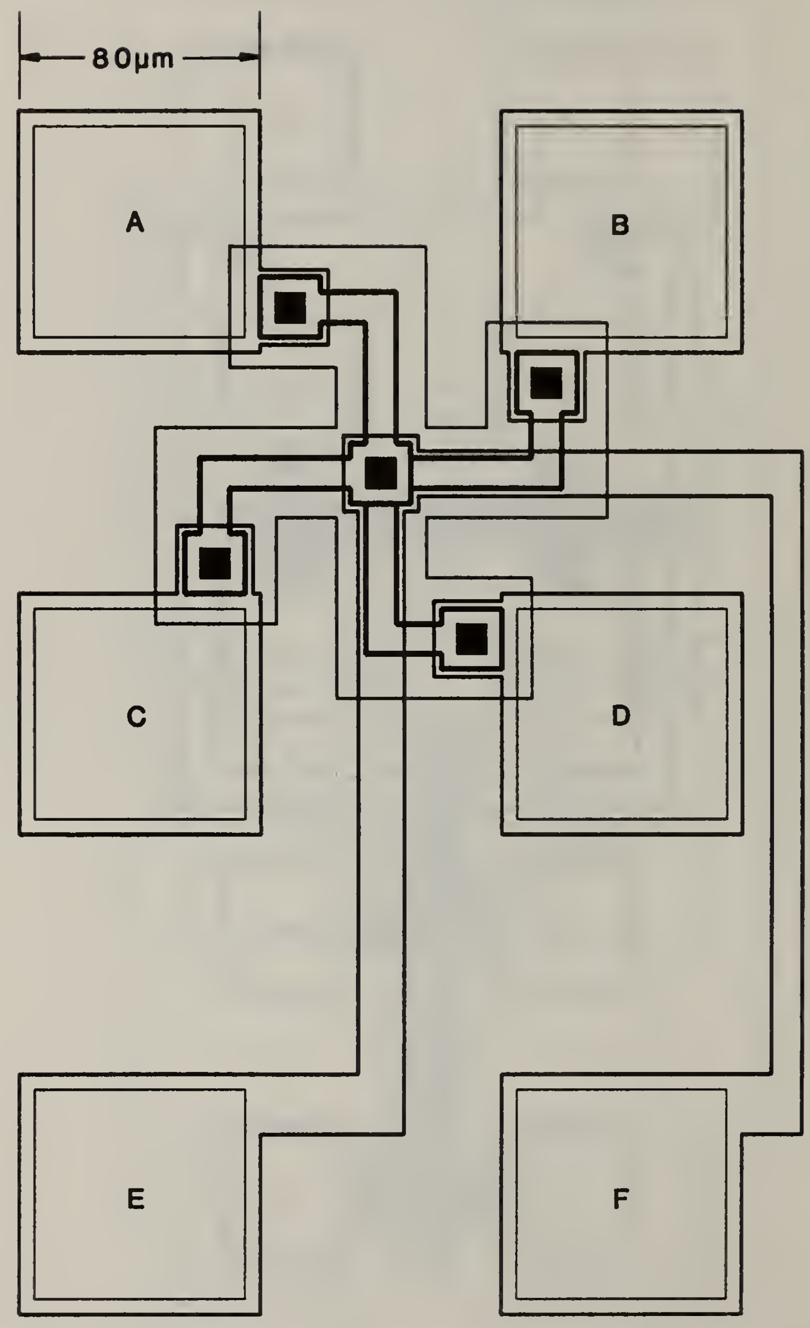


Figure 7a. Six-terminal metal-to-diffusion contact resistor.

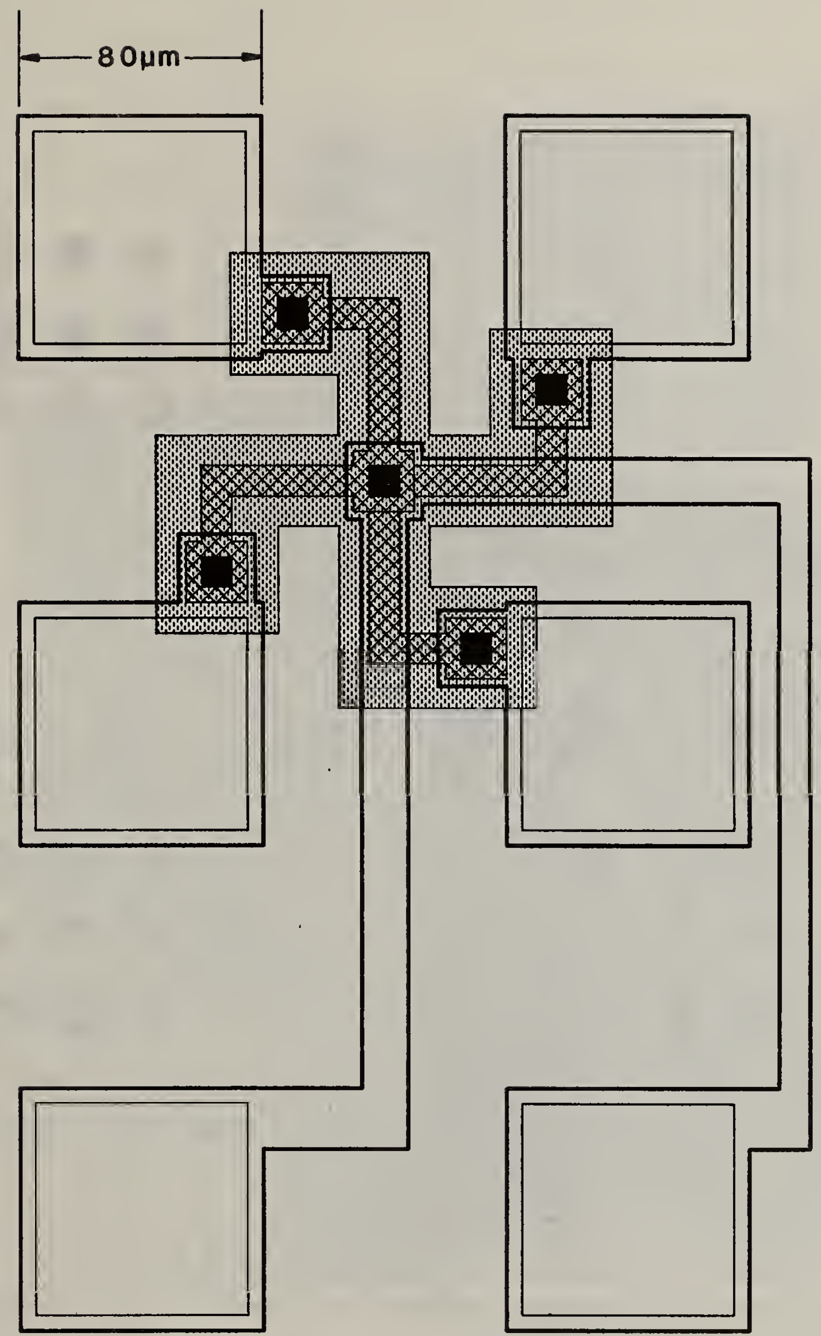


Figure 7b. Six-terminal metal-to-polysilicon contact resistor.

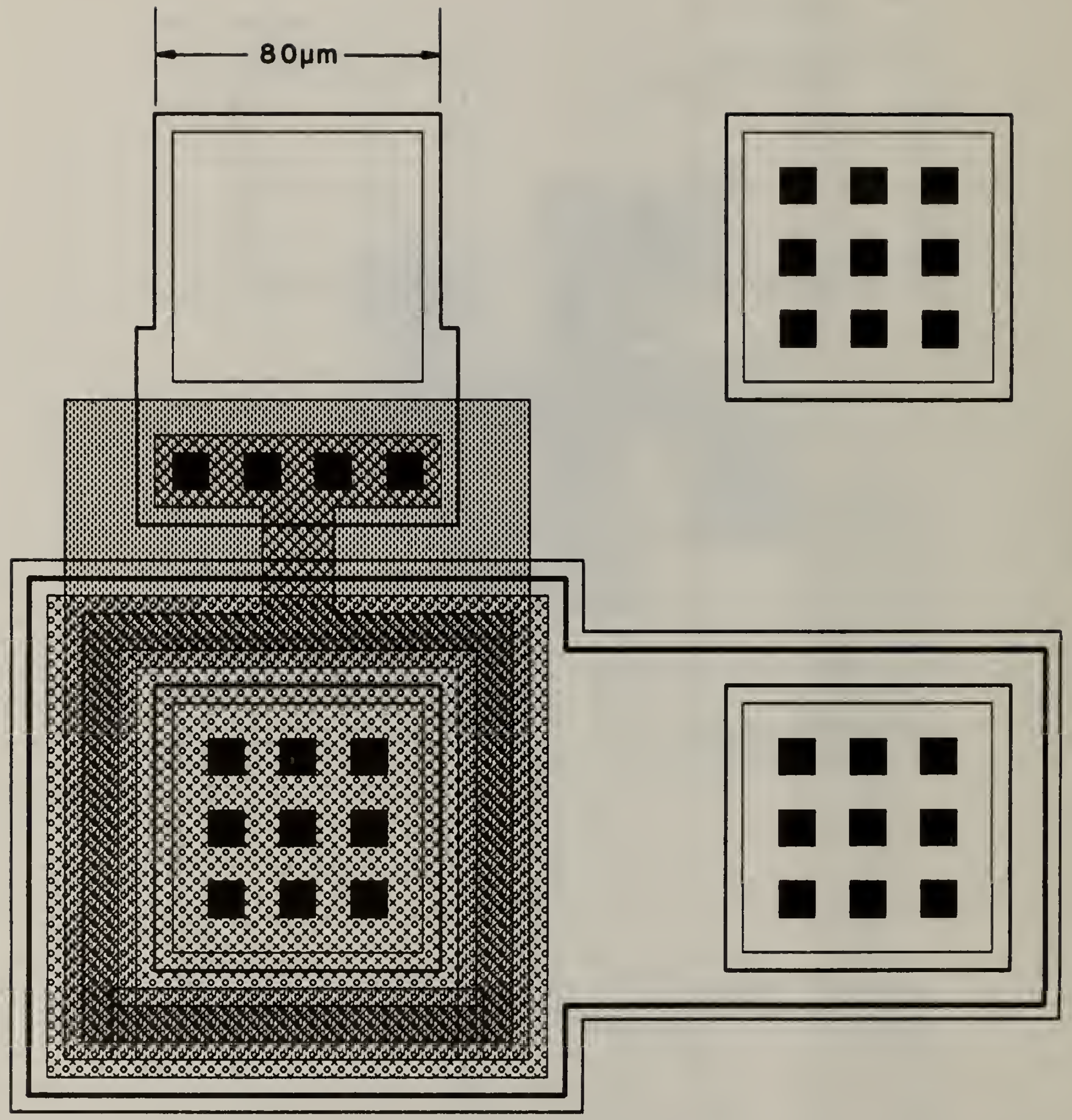


Figure 8. n-channel enhancement MOSFET for dopant profile determination, L = 10 µm, W = 440 µm.

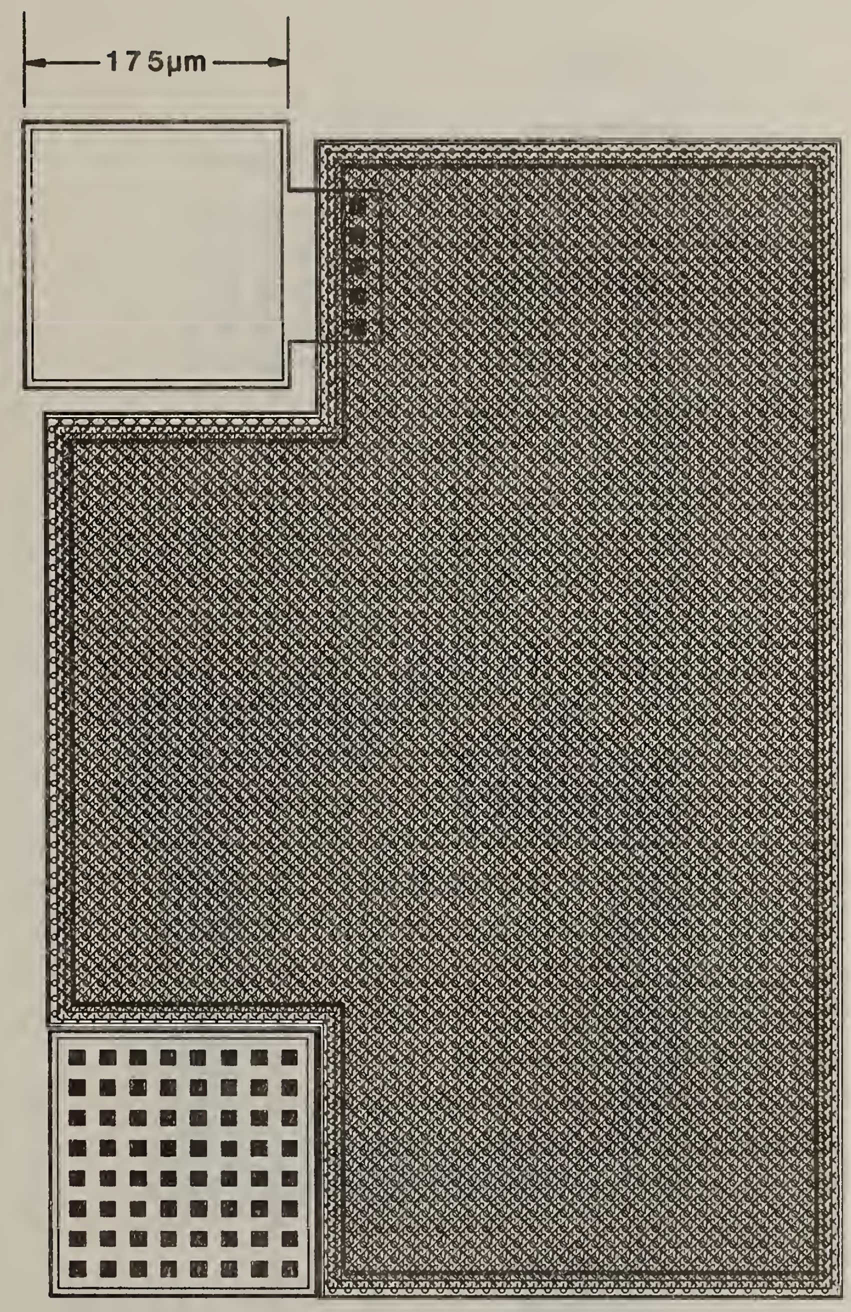


Figure 9a. Polysilicon gate capacitor, $A = 3.06 \times 10^5\ \mu m^2$.

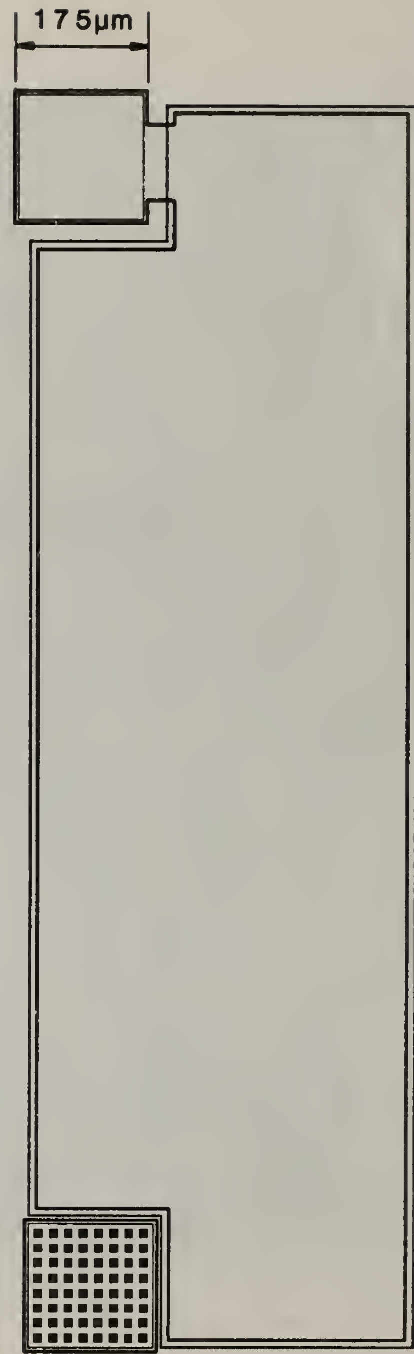


Figure 9b. Metal gate capacitor, $A = 7.30 \times 10^5\ \mu m^2$.

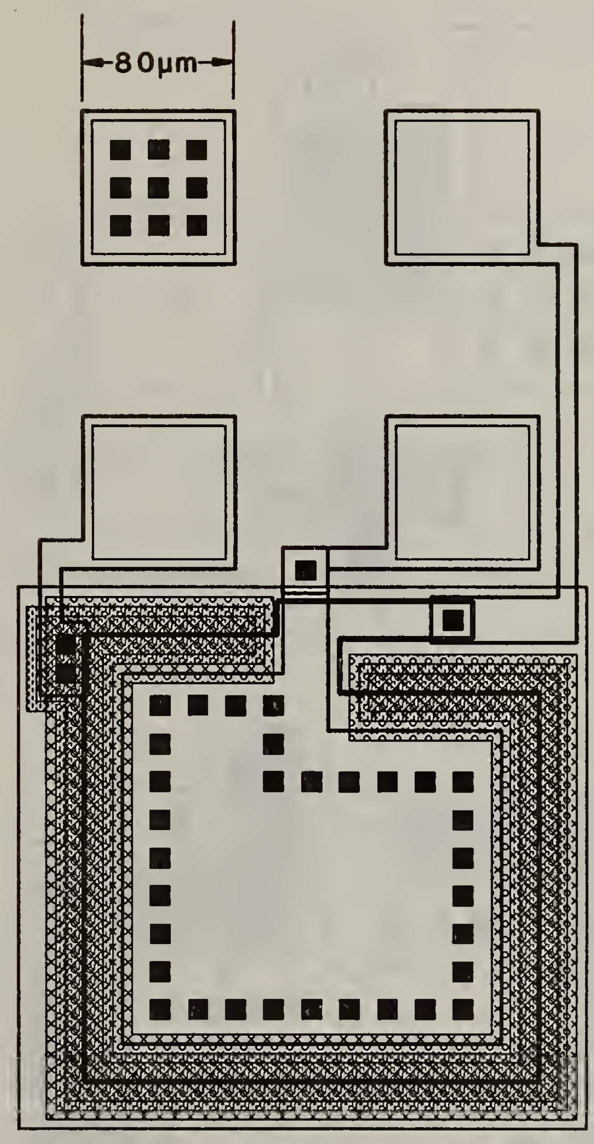


Figure 10a. Gated diode.

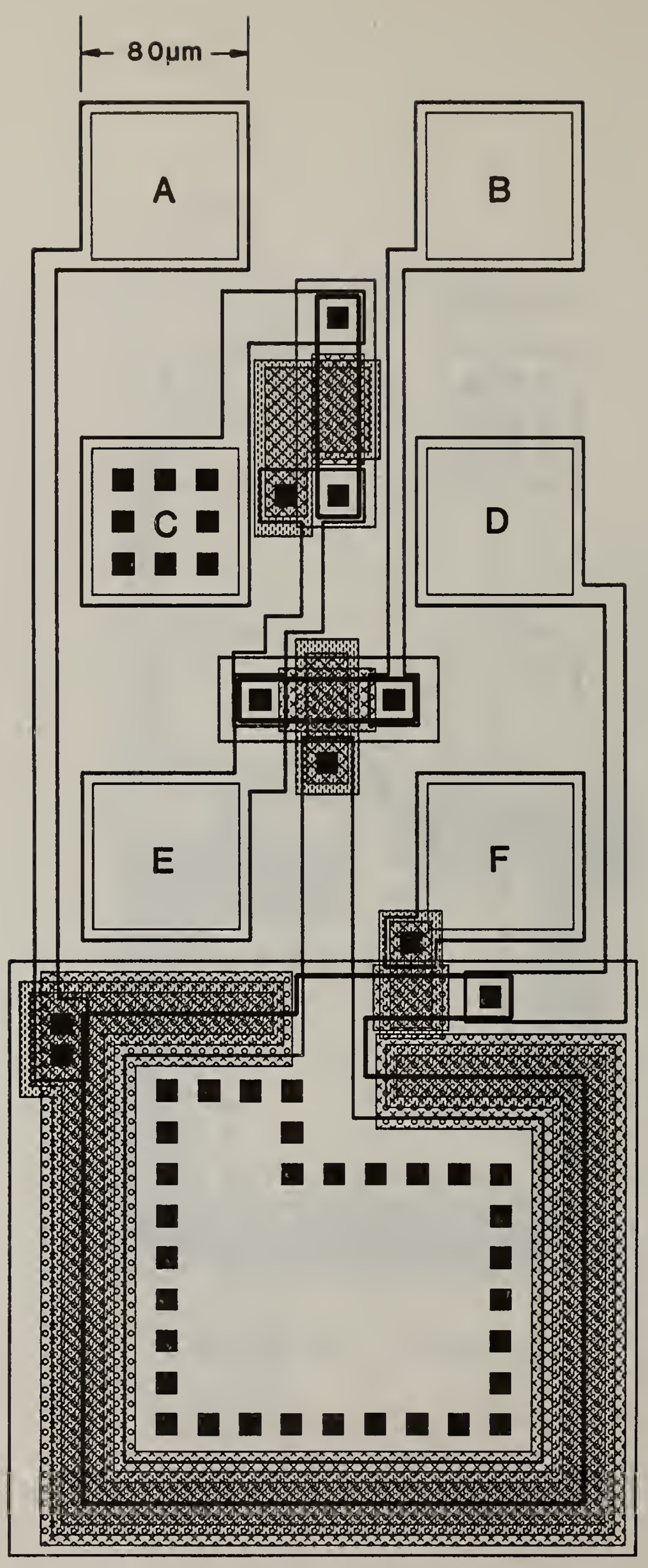


Figure 10b. Gated diode electrometer.

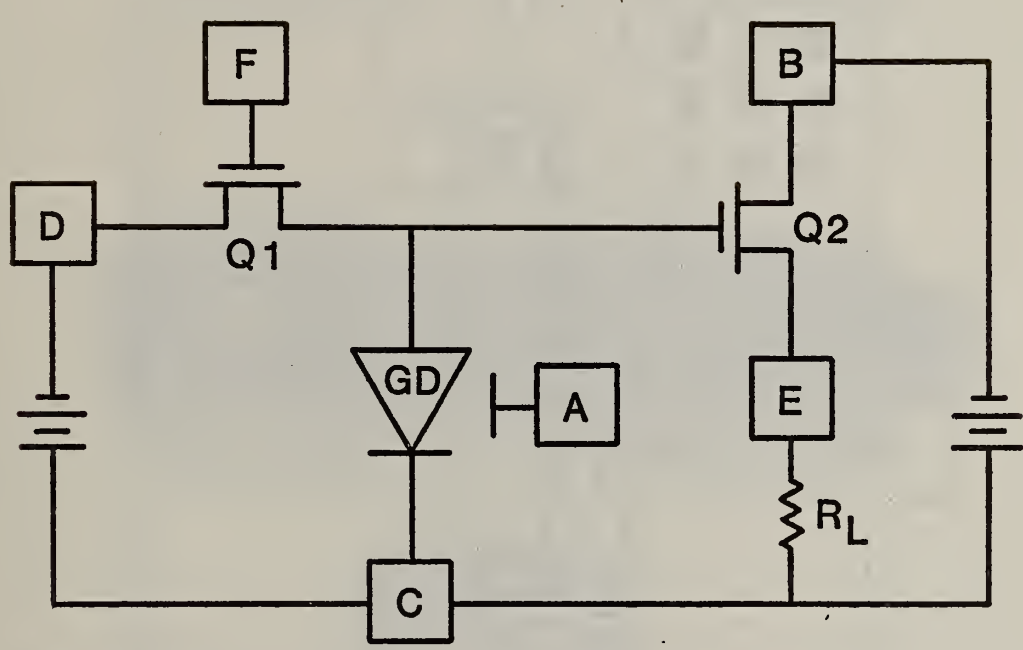


Figure 10c. Schematic drawing of the gated diode electrometer where GD is the gated diode, Q1 the reset switch, Q2 the source-follower, and R_L is the load resistor.

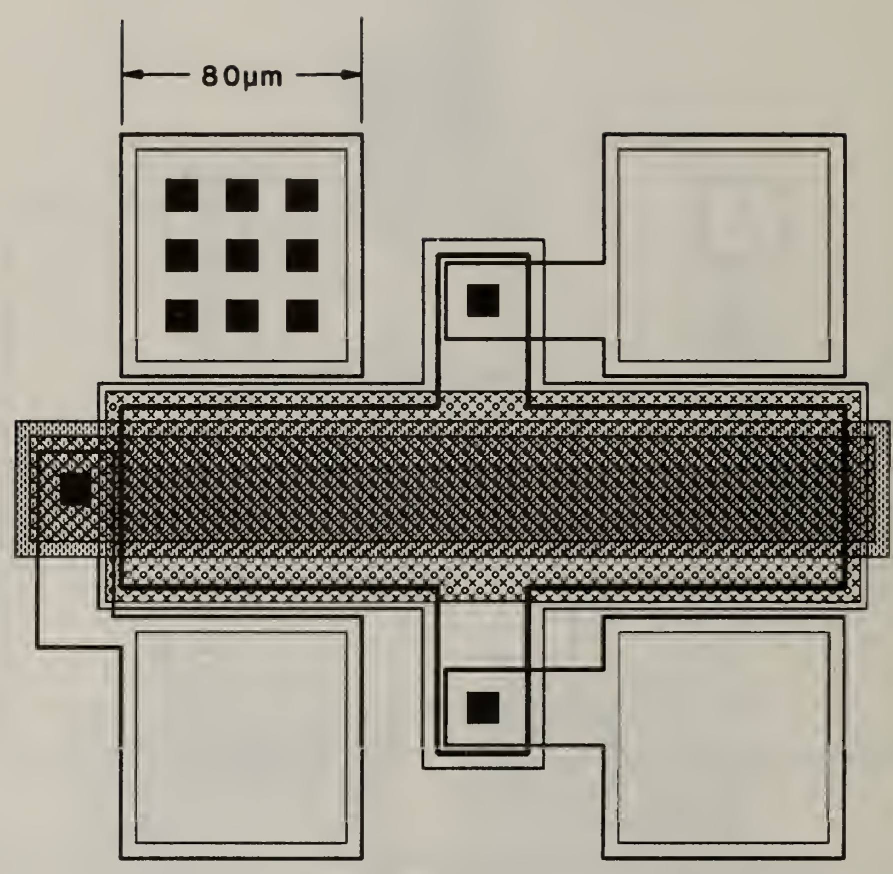


Figure 11. *n*-channel enhancement MOSFET, L = 35 μm, W = 240 μm.

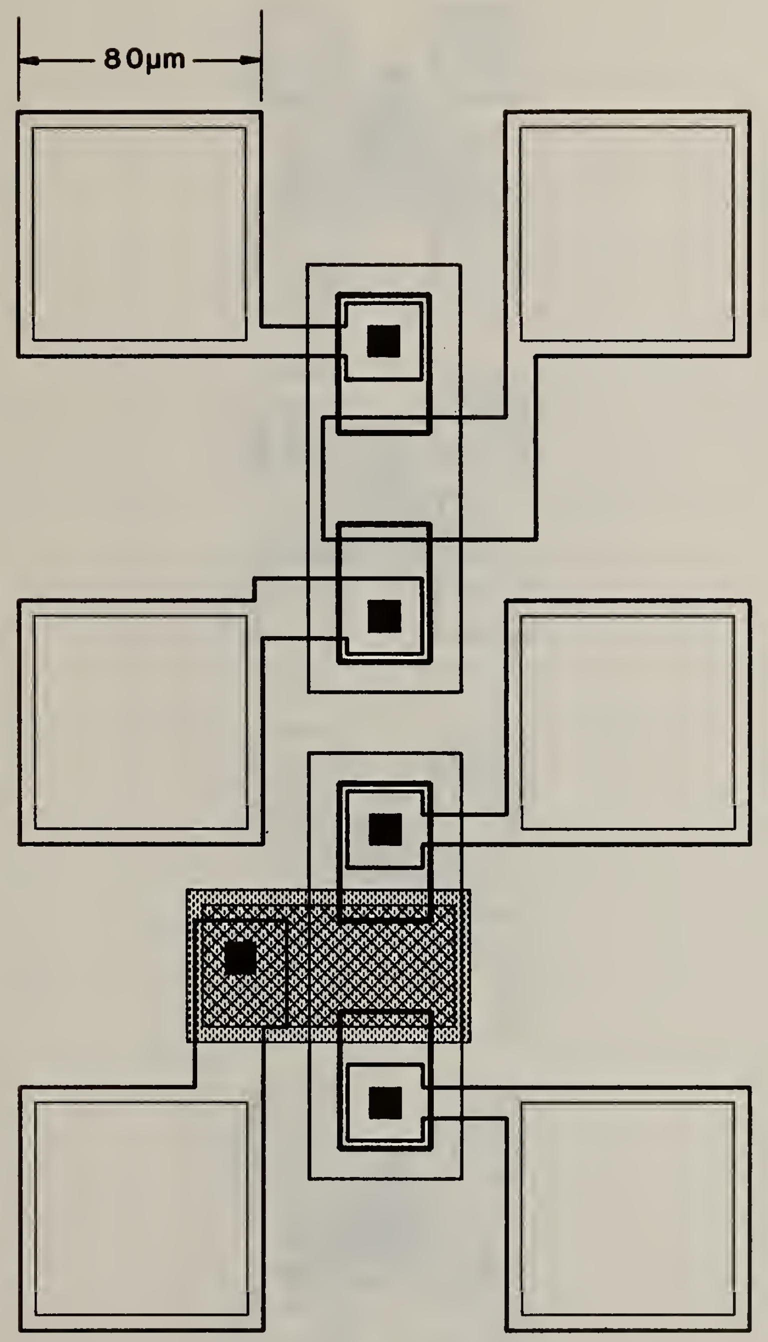


Figure 12. Metal-gate, field oxide MOSFET (top) and polysilicon-gate field oxide MOSFET (bottom).

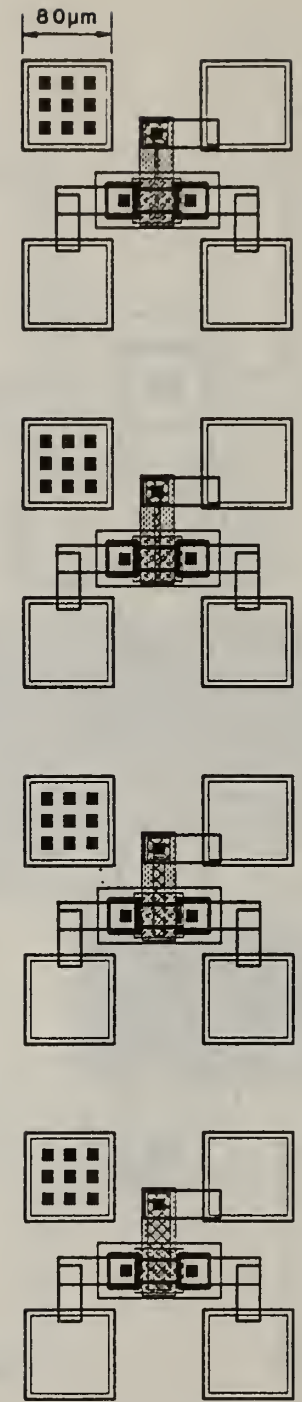


Figure 13a. *n*-channel enhancement MOSFET array, L = 2.0, 5.0, 10.0, and 20.0 µm, W = 20 µm.

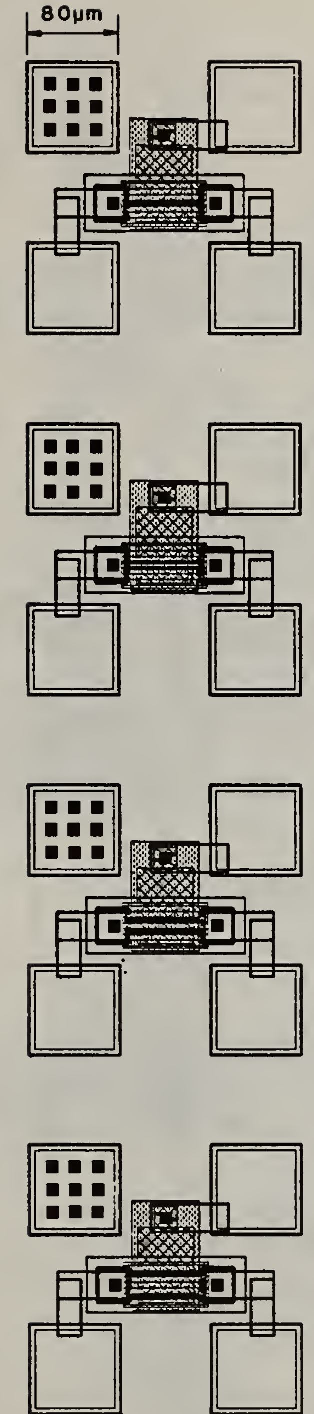


Figure 13b. n-channel depletion MOSFET array, L = 2.0, 5.0, 10.0, and 20.0 μm, W = 50 μm.

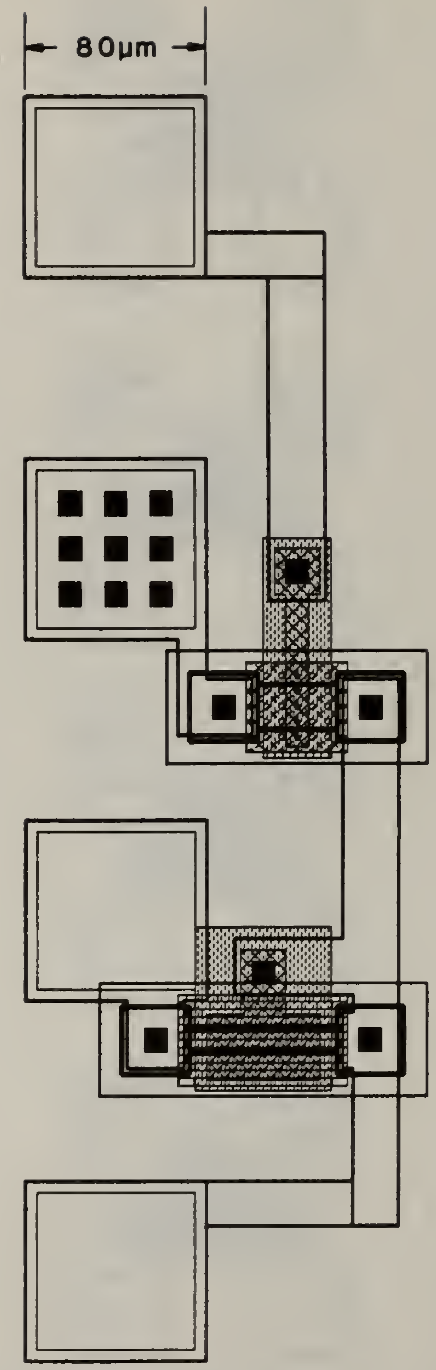


Figure 14. Inverter stage.

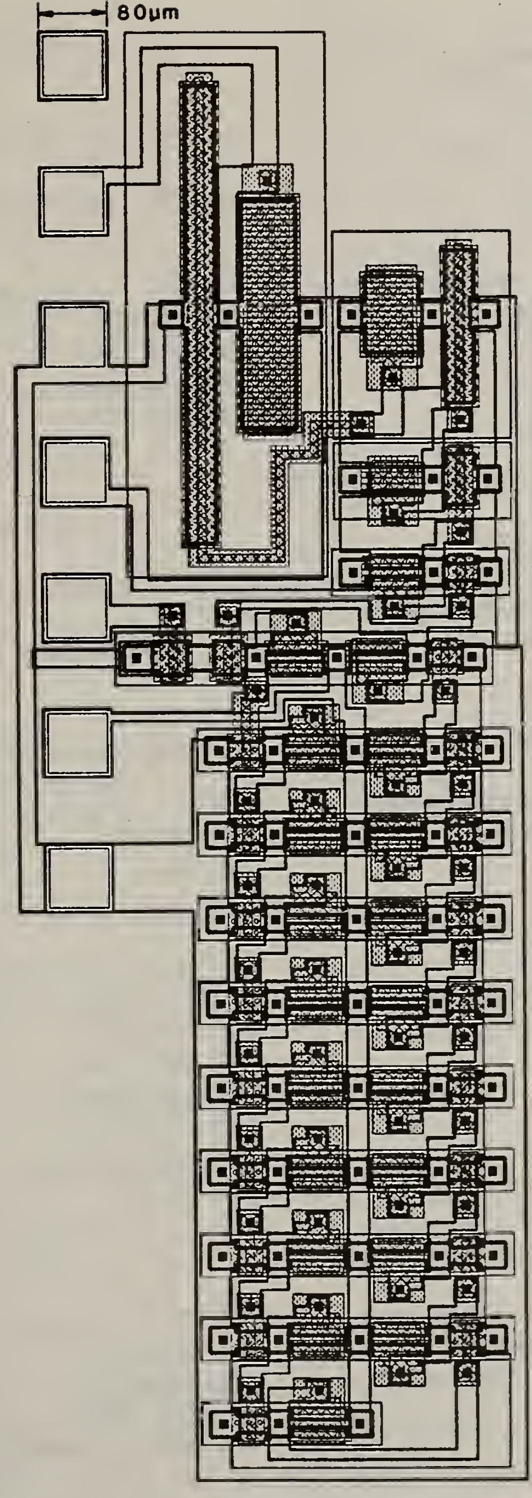


Figure 15. Ring oscillator.

APPENDIX
NMOS Process for NBS Test Chip

Wafer: ρ = 20 Ω•cm, *p*-type (100)
Diffusion tube inside diameter: 75 mm

1. Initial wafer clean

2. Initial oxidation

Furnace temperature:	1100°C
O_2 flow rate:	500 cc/min
Cycle:	20 min dry
	20 min wet
	20 min dry t_{ox} = 0.33 μm

3. Isolation lithography (photomask #1)

4. Boron predeposition

Furnace temperature:	975°C
N_2 flow rate:	500 cc/min
Cycle:	15 min

5. Boron skin removal

Furnace temperature:	700°C
O_2 flow rate:	300 cc/min
Cycle:	20 min

6. Boron drive-in and reoxidation

Furnace temperature:	1100°C
O_2 flow rate:	500 cc/min
Cycle:	20 min dry
	40 min dry
	120 min dry

7. Gate window lithography (photomask #2)

8. Gate oxide growth (75 nm)

Furnace temperature:	1000°C
O_2 flow rate:	500 cc/min
N_2 + TCE flow rate:	25 cc/min
Cycle:	110 min dry
	10 min N_2 anneal
	t_{ox} = 0.076 μm

9. Enhancement threshold implant lithography (photomask #3)

10. Enhancement threshold implant (target V_{TE} = 1.0 V)

Ion:	Boron
Ion energy:	60 keV
dose:	5×10^{11} ions/cm^2

11. Depletion threshold implant lithography (photomask #4)

12. Depletion threshold implant (target V_{TD} = -3.0 V)

Ion:	Phosphorus
Ion energy:	120 keV
Dose:	6×10^{11} ions/cm^2

13. Polysilicon deposition

Temperature:	650°C
Time:	13 min
Thickness:	0.8 μm

14. Oversize polysilicon lithography (photomask #5)

15. Phosphorus predeposition for source-drain and polysilicon gate doping

Furnace temperature:	950°C
N_2 flow rate:	500 cc/min
O_2 flow rate:	50 cc/min
Cycle:	14 min

16. Phosphorus drive-in and reoxidation

Furnace temperature:	1000°C
O_2 flow rate:	500 cc/min
Cycle:	18 min dry

17. Polysilicon gate lithography (photomask #6)

18. Phosphorus source-drain implant

Ion energy:	120 keV
Dose:	2×10^{13} ions/cm^2

19. Implant activation

Furnace temperature:	900°C
N_2 flow rate:	500 cc/min
Cycle:	20 min

20. Oxide deposition

Temperature:	800°C
Time:	30 min

22. Aℓ deposition

23. Aℓ interconnect lithography (photomask #8)

24. Aℓ alloying

Furnace temperature:	500°C
N_2 flow rate:	250 cc/min
Cycle:	3 min

25. P SiO_2 glass deposition

26. Passivation lithography (photomask #9)

NBS-114A (REV. 2-80)

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11. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)*

This report describes an NMOS test chip, NBS-40, which was developed to be used in graduate level electronics engineering courses involving semiconductor parameter measurements associated with the fabrication of integrated circuits. The 35 test structures included in the test chip and their use in materials, device, and process parameter measurements are described. Details of the silicon gate NMOS process used in the chip fabrication are also provided.

12. KEY WORDS *(Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)*

Integrated circuit; microelectronics; parameter measurements; solid-state electronics; test chip; test pattern; test structures.

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