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SEMICONDUCTOR TECHNOLOGY PROGRAM

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ABSTRACT - This report provides abstracts of recent publications of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Topics include: defects and impurities, IC test structures, micrometrology, packaging, physical analysis, power devices, process and device modeling, and radiation effects. In addition, publications in press and conference presentations are listed. Information is also given on recent seminars, workshops, and symposia and those scheduled for the near future.

KEY WORDS - Compound semiconductors; electronics; GaAs; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report is comprised of abstracts of results published during the fifty-third through the fifty-seventh quarters (July 1981 through September 1982) of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program was provided by a variety of Federal agencies during the period covered by this report: 1. The National Bureau of Standards; 2. The Defense Advanced Research Projects Agency; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Defense Nuclear Agency; 5. The Naval Weapons Support Center; 6. The Solar Energy Research Institute; 7. The Electronic Technology and Devices Laboratory, Department of the Army; 8. The Air Force Weapons Laboratory; and 9. and The Harry Diamond Laboratories.

This report is provided to disseminate results to the semiconductor community. The Program is a continuing one; the results and conclusions reported herein are subject to modification and refinement. Further information may be obtained directly from responsible staff members. General information, past issues of progress briefs, and a list of publications may be obtained from the Semiconductor Materials and Processes Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Recent Publications . . .

Defects & Impurities

Tertiary Interferograms in Fourier Transform Spectroscopy, Baghdadi, A., and Forman, R. A., *Applied Spectroscopy* 35, 473-475 (1981).

Multiple passes, both within a semiconductor specimen and between the specimen surface and the interferometer, give rise to a series of extraneous "tertiary" interferograms in a Fourier transform spectrophotometer. These tertiary interferograms can lead to a possible error on the order of 1% in the measurement of the impurity content of a silicon wafer. However, this effect can be eliminated by a straightforward manipulation of the interferogram prior to transformation.

**Semiconductor Measurement Technology:* Differential Capacitance-Voltage Profiling of Schottky Barrier Diodes for Measuring Implanted Depth Distributions in Silicon, Wilson, R. G., and Jamba, D. M., NBS Spec. Publ. 400-71 (February 1982).

This report discusses experimental and analytical aspects of differential capacitance-voltage profiling of ion-implanted carrier depth distributions using reverse-biased Schottky barrier diodes and the associated accuracies, experimental errors, and ranges of applicability.

Improved Thermometry for Deep-Level Measurements, Phillips, W. E., *J. Physics E.* 15, 499-501 (May 1982).

The various semiconductor deep-level measurement techniques are often limited in their precision by thermometry. A temperature-measurement procedure is described which uses a statistical calibration of forward-biased temperature-sensing diodes to achieve a two-sigma precision of ±8 mK. Several applications are discussed to illustrate where the improved thermometry can significantly affect the quality of the results.

Vibronic Spectrum of the U_2 Isoelectronic Center in Si:In, Stahlbush, R. E., and Forman, R. A., *J. Luminescence* 26, 227-232 (1982).

The photoluminescence spectrum of Si:In measured at 2 and 4 K using samples from several suppliers has been found to be preparation sensitive. In particular, intensity variations allow us to distinguish a sharp no-phonon line at 1.118 eV, variously referred to as U_2 or P, and its associated vibronic spectrum from the In(NP) lines and their phonon replicas. Whereas the intensity of the latter did not show preparation sensitivity, the former has been observed to change by three orders of magnitude. The U_2 vibronics form a broad-structured spectrum containing density-of-states features. The appearance of phonons other than those conserving crystal momentum demonstrates the exciton is bound to a low symmetry site. In addition, the spectrum includes a peak at 1.109 eV, called R, and a shoulder at 1.107 eV which involves too small an energy loss to be density-of-states related, and these features are most likely modes of the U_2 impurity complex. This complex has been tentatively identified as an isoelectronic center composed of an indium-phosphorus nearest-neighbor substitutional pair.

IC Test Structures

Electrical Test Structures for Characterization and Control of Microelectronics Processing, Mitchell, M. A.,

*Non-NBS authors

Linholm, L. W., Russell, T. J., and Carver, G. P., *Proc. Microelectronics Measurement Technology Seminar*, San Jose, California, March 17-18, 1981, pp. VI-1 - VI-29 (Benwill Publishing Co., Boston, 1981).

The trend toward smaller devices in larger integrated circuits makes assurance that the product will function as desired increasingly difficult. The results of measurements from specially designed microelectronic test structures can be a critical ingredient in process characterization and control, two of the primary factors affecting circuit functionality. Test structures can be used to evaluate IC materials, to evaluate and control process uniformity, to measure and control device and circuit parameters, to quantify the occurrence of process-related random faults, and to evaluate processing equipment performance. The electrical test structures and test methodologies reviewed here have been developed for rapid automated measurement of a variety of parameters including sheet resistance (of metal, polysilicon, or diffusion/implant), linewidth (in two orthogonal directions), photomask misalignment, contact resistance, minority carrier lifetime, dopant profile, and densities of several different types of process-induced random faults. These test structures are modular and may be grouped to form a test pattern in whatever way suits the needs of the user. Test patterns can be located at a few drop-in sites on a wafer for spot checking parameters, or repeated at all sites for statistical and spatial analysis of a process. Simple, fast, visual correlations of the parameters in the form of wafer maps provide information about yield-reducing variations in parameters. Examples of such correlations are discussed.

Semiconductor Measurement Technology: The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control, Linholm, L. W., NBS Spec. Publ. 400-66 (August 1981).

A Process Validation Wafer (PVW) is a wafer containing only test patterns. One PVW accompanies a product lot during the fabrication process. Test patterns NBS-16 and NBS-26 are designed to be used on PVWs. They contain both process parameter test structures and random fault test structures. Eighteen NBS-16 PVWs were fabricated in a radiation-hardened silicon-gate CMOS/SOS process. These PVWs were tested on a high-speed computer-controlled dc test system. Test results from the process parameter test structures were used to establish the baseline electrical parameters for each product lot and to produce an eight-level gray scale wafer map for these parameters. Based on correlations of selected wafer maps, it was possible to identify specific yield-related process problems otherwise unknown to the manufacturer or user.

Test results from two random fault test structures were used to establish a statistically significant data base for identifying and evaluating major yield-limiting fault mechanisms in the process. Test results from a developmental random access fault structure and a gate dielectric integrity array are presented. The results are analyzed for selected PVWs and a major yield-limiting fault mechanism detected. A description of the test pattern and test results, including a drawing of each test structure, recommended test procedure, and design rules, are found in the appendices.

Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened Charge-Coupled Device (CCD) Imagers: Annual Report, May 15, 1980 to May 14, 1981, Carver, G. P., NBSIR 81-2319 (August 1981).

The purpose of this project is to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. During the period covered by this report, consultation was provided to The Charles

Stark Draper Laboratory, Inc. (CSDL) and to CSDL contractors on the implementation and use of test structures developed previously during this project. In addition, the results of measurements on CCD imager wafers using the surface-channel and buried-channel, integrated gated-diode electrometers, before and after exposure to ^{60}Co radiation, and using the cross bridge/electrical alignment test structures are reported. Examples of cross sections of the CCDs made by beveling and staining are also presented.

Role of Test Chips in Coordinating Logic and Circuit Design and Layout Aids for VLSI, Buehler, M. G., and Linholm, L. W., *Solid State Technology* 24, 68-74 (September 1981).

The need for multipurpose test chips and comprehensive procedures for use in supplying accurate input data to both logic and circuit simulators and chip layout aids is emphasized. It is shown that the location of test structures within test chips is critical in obtaining representative data, because geometrical distortions introduced during the photomasking process can lead to significant intrachip parameter variations. The need for a commonly accepted portable chip layout notation and commonly accepted parametric tester language is demonstrated. The need to develop parametric testers with improved architecture in conjunction with innovative test structures with on-chip signal conditioning is also discussed.

Production-Compatible Microelectronic Test Structures for the Measurement of Interface State Density and Neutral Trap Density, Russell, T. J., NBSIR 81-2413 (January 1982).

Interface states and oxide neutral traps are defects in metal-oxide-semiconductor (MOS) structures which adversely affect the operation of integrated circuits (ICs). For very large scale integration (VLSI), the advanced techniques which are used to fabricate circuits with devices of submicrometer geometries expose the devices to ionizing radiation which can create these defects or alter the number of defects and their charge state and thus modify device operating characteristics. The physical identities of the defects which trap charge at the interface and in the bulk oxide are not well established. This means that one cannot *a priori* predict the behavior of the defects to a stress or fabrication process. Thus, it is desirable that the density of these defects be monitored routinely and that the measurement method used be easy to perform and fast and that it provide unambiguous results and be compatible with a production environment. The purpose of this study is to identify production-compatible measurement methods which can be used for routine measurement of neutral trap density and interface trapped charge. This study reviews the application of existing methods for quantifying the number of these defects. Methods determined to be most appropriate for the stated purpose are discussed in detail.

A Computer Program for Analysis of Data from Microelectronic Test Structures, Mattis, R. L., Till, L. J., and Frisch, R. C., NBSIR 82-2492 (June 1982).

A computer program, STAT2, is described which performs the following functions: reads data as a two-dimensional array; calculates mean, sample standard deviation, and median; identifies outliers; calculates replacement values for outliers; makes a gray-tone data map on a line printer; makes a character map on the user's terminal; constructs a data base for examining correlations among various data sets; and searches the data base for correlations using several selective keys. The emphasis in this document is on program usage, and detailed descriptions of the commands are given. Program portability and data input requirements are addressed. Guidance regarding several types of program modifications is provided.

Evaluation of a CMOS/SOS Process Using Process Validation Wafers, Suehle, J. S., Linholm, L. W., and Marshall, G. M., NBSIR 82-2514 (June 1982).

The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.

Design Considerations for the Cross-Bridge Sheet Resistor, Carver, G. P., Mattis, R. L., and Buehler, M. G., NBSIR 82-2548 (July 1982).

The cross-bridge sheet resistor test structure is used to obtain the sheet resistance and electrical linewidth of a conducting layer. It has been used to characterize various conducting layers found in an integrated circuit fabrication process and to evaluate lithographic equipment used for processing photomasks and wafers. Three geometrical design factors for the cross bridge have been investigated and are shown to cause systematic inaccuracies of less than 1 percent in the sheet resistance and linewidth measurements. Based upon experimental results from sequences of devices with incrementally different geometrical parameters, several design criteria for the cross-bridge sheet resistor have been established.

Micrometrology

Optical Linewidth Measurements on Photomasks and Wafers, Bullis, W. M., and Nyyssonen, D., Chapter in *VLSI Electronics: Microstructure Science*, Vol. 3, Norman G. Einspruch, Ed. (Academic Press, New York), January 1982.

This chapter discusses the origins of systematic errors in optical linewidth measurement systems, outlines advances in modeling the linewidth measurement process including imaging in the optical microscope, describes a primary linewidth measurement system in use at the National Bureau of Standards (NBS), and discusses the use of primary measurements to calibrate less accurate systems conventionally used for linewidth measurements. Although emphasis is placed on measurements of patterns on antireflective (AR) chromium photomasks in transmitted light, measurements on other types of materials including see-through photomasks and wafers are also discussed.

Calibration of Optical Systems for Linewidth Measurements on Wafers, Nyyssonen, D., *Opt. Eng.* 21, 882-887 (September/October 1982).

In contrast to earlier work with nearly opaque photomasks, optical linewidth measurements on wafers encompass materials with a much wider variation in optical parameters and material profiles. Accurate optical edge detection requires corrections for both the relative reflectance and phase at the line edge because of the partial coherence present in optical microscopes. However, measurement systems which cannot provide the appropriate corrections and cannot detect edge location accurately can be calibrated. Since the correction curve is material dependent, calibrated standards are theoretically required for each step in the wafer fabrication process where linewidths are measured. In the proposed approach for thin layers (less than 200 nm), a small number of etched silicon-dioxide-on-silicon wafers can be used for calibration of a large class of wafer materials. Examples of wafer calibration data for filar, image-splitting and image-scanning systems are given. The problems associated with accurate linewidth measurement and calibration for thick layers are also discussed.

Packaging

The Use of Acoustic Emission as a Test Method for Electronic Interconnections and Joints, Harman, G. G., *Proc. Int. Conf. Soft Soldering in Electronics and Precision Mechanics,* Munich, Germany, November 11-12, 1981, pp. 104-110.

The use of acoustic emission (AE) to determine the integrity of various microelectronic joints is relatively new. Considerable success has been achieved using AE as an in-process production monitor, and some of these uses are reviewed. However, implementation problems have been experienced using AE as an after-production screen. These problems result from the small size of the electronic components as well as the difficulty of applying an appropriate nondestructive mechanical or thermal stress to the tiny joints. The small size also causes difficulty in interpreting the AE signals. These and other problems are discussed and various solutions proposed.

The paper describes a newly designed miniature AE detector in a TO-5 sized package appropriate for microelectronic use that has high sensitivity to surface waves and contains its own built-in 40-dB preamplifier. Methods and criteria for discriminating against extraneous acoustic noise and triggering only on signals representing a predetermined failure level are discussed. Examples of AE testing (using the above principles) such as an AE-monitored automatic fatigue tester for electronic joints and a production tester for TAB devices are given.

Acoustic-Emission-Monitored Tests for TAB Inner Lead Bond Quality, Harman, G. G., *Proc. 1982 32d Electronic Components Conf.,* San Diego, California, May 10-12, 1982, pp. 268-276.

This paper gives a brief introduction to acoustic-emission (AE) based tests applied to quality control in the electronics industry and describes some recent research on this testing technique. Equipment and circuits are described that may be used to implement such AE-monitored testing. Acoustic-emission monitored test systems to determine the inner lead bond quality for Tape Automated Bonding (TAB) have been developed. These include a pull tester and a microfatigue tester for off-line evaluation of bond quality and metallurgical system reliability as well as an automatic on-line production bond quality tester. The microfatigue tester for TAB leads can apply a small oscillatory (up to 80 Hz) force on top of a constant force bias of a few grams. A major result of such fatigue tests was to show that the most common metallurgical system (tin-plated copper leads bonded to gold bumps) results in the formation of brittle intermetallic compounds which crack easily. The cracks propagate under cyclic stress and result in a very low fatigue life, compared to another TAB metallurgical system. The acoustic-emission-monitored inner lead bond integrity tester and lead-forming system is designed to be used on-line. Precision wedge-shaped tools rise up from below a clamped chip and apply a predetermined force ($\sim$100 mN) to the leads, which both nondestructively tests the bonds and forms the leads. If any lead separates, or partially separates from the bump, or the bump separates from the chip, the AE monitor can indicate failure and the device can be rejected. Data are presented to show various failure modes of the TAB system.

Semiconductor Measurement Technology: The Use of Acoustic Emission to Determine the Integrity of Large Kovar Glass-Sealed Microelectronic Packages, Harman, G. G., NBS Spec. Publ. 400-70 (May 1982).

The general objective of this research was to develop tests to determine the integrity of large hybrid packages under various thermal and mechanical stresses that may be encountered during assembly, during installation in systems, or in operation. Several measurement techniques were investigated, but emphasis was placed on acoustic-emission test procedures. The accomplishments were: (1) The effects of avionics environmental vibration on the seals of hybrid packages mounted on printed-circuit (PC) boards were determined. A major conclusion of this section was that lead fatigue failure occurs before seal damage on packages from high quality lots. (2) A small acoustic-emission detector was developed that is sensitive to surface waves, but relatively insensitive to vibration-induced cable noise. (3) A high-temperature (125°C) open-package helium leak test method was successfully developed to observe marginal seal damage. (4) An acoustic-emission test for inspection of hybrid packages during high-temperature thermal shock was developed. (5) A study of possible damage to seals during thermocompression and thermosonic bonding, during lead forming, and during other assembly operations was carried out. A general conclusion of this study is that the glass-metal seals in packages from known high quality lots are very reliable even when subjected to high stresses. However, the seals from packages "screened as good" from reject or poor quality lots are subject to hermetic failure under moderate stresses. There is little correlation between visual inspection failures of glass seals and their hermeticity.

Physical Analysis

**Semiconductor Measurement Technology:* The Capabilities and Limitations of Auger Sputter Profiling for Studies of Semiconductors, Schwarz, S. A., Helms, C. R., Spicer, W. E., and Taylor, N. J., NBS Spec. Publ. 400-67 (September 1981).

Materials characterization is a critical area in current silicon integrated circuit technology. Those techniques that are commonly used include Auger sputter profiling, X-ray photoelectron spectroscopy, secondary ion mass spectrometry, and Rutherford backscattering. All of these techniques have unique capabilities and limitations for studies of silicon device structures. In this paper, we describe the capabilities and limitations of Auger sputter profiling especially with regard to sensitivity, spatial resolution, depth resolution, and chemical state determination. Although much of the discussion centers on Auger sputter profiling, the results are also applicable to X-ray photoelectron spectroscopy and secondary ion mass spectrometry.

Investigation of the Two-Dimensional Shape of Ion-Implanted Regions, Roitman, P., Albers, J., Ehrstein, J. R., and Myers, D. R., NBSIR 81-2398 (December 1981).

The two-dimensional shape of arsenic ion-implanted regions in single-crystal silicon was investigated both experimentally and theoretically. Experimentally, two techniques were shown to have the necessary submicron resolution: a junction etch process and an SEM-induced current collection method. A comparison of junction depths determined by the etch technique, the EBIC technique, and spreading resistance with the depths calculated using several amorphous target codes was made. For the case of low temperature (600°C) anneals, the etch technique agrees very well with the junction depths predicted by the amorphous target code due to Winterbon. The lateral junction locations obtained from the etch technique are in good agreement with the predictions of a two-dimensional Monte-Carlo code (TRIM) which indicates that arsenic does not show any significant lateral scattering under mask edges. For the case of high temperature (1000°C) anneals, the etch and EBIC techniques agree with each other, but show consistently deeper junction locations than does the spreading resistance technique. Comparison

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with arsenic-diffusion models shows that concentration-dependent effects are important. Presently available processing models do not appear to adequately forecast junction depths.

Measurement of the Interlayer Between Aluminum and Silicon Dioxide Using Ellipsometric, Capacitance-Voltage and Auger Electron Spectroscopy Techniques, Candela, G. A., Galloway, K. F., Liu, Y. M., and Fine, J., *Thin Solid Films* 82, 183-193 (1981).

Ellipsometric and capacitance-voltage measurements were combined to detect both the Al-SiO_2 interlayer and the Si/SiO_2 interlayer for the $Si/SiO_2/Al$ system. The Al-SiO_2 interlayer was characterized by Auger electron spectroscopy (AES), combined with argon ion sputter profiling, of the $Al/SiO_2/Si$ structure and also of the remaining SiO_2/Si structure after the aluminum had been chemically removed. An effective interlayer thickness is defined as the product of the interlayer thickness and the fractional change in the dielectric SiO_2 constant. The results of these experiments indicate that the Al-SiO_2 effective interlayer thickness has a range of 0.1-0.5 nm. The AES data can be readily interpreted if it is assumed that collision cascade mixing and recoil implantation occur as a consequence of sputter depth profiling through the aluminum.

Laser Ablation and Resonance Ionization Spectrometry for Trace Analysis of Solids, Mayo, S., Lucatorto, T. B., and Luther, G. G., *Anal. Chem.* 54, 533-556 (1982).

The first application of resonance ionization spectrometry to trace analysis of solids is demonstrated by using laser ablation to evaporate small amounts of single-crystal silicon and detecting sodium in the evaporated material. Sodium is detected by using two tunable laser probes to induce resonantly enhanced multiphoton ionization. Several samples, both Czochralski and float-zoned silicon, were analyzed. Using certain simplifying assumptions about the laser-evaporated plume, we estimated that the sodium contamination density in the purest sample was of the order of 10^{11} atoms/cm^3. For further development of this technique for absolute quantitative measurements, the various processes involved in laser evaporation of solids should be more completely understood. Generalization of this technique to other contaminant species in metals, semiconductors, and insulators is subject to laser availability.

Principal Angle Spectroscopic Ellipsometry Utilizing a Rotating Analyzer, Chandler-Horowitz, D., and Candela, G. A., *Appl. Optics* 21, 2972-2977 (August 1982).

The variations of the intensity of the reflected light near null as a function of the angle of incidence are compared for three ellipsometric techniques. For films of either SiO_2 or Si_3N_4 on silicon, the highest accuracy of the film thickness measurement is always obtained when the angle of incidence is either equal or nearly equal to the principal angle for all thicknesses of the film layer. Based on these results, it is shown that a variable angle of incidence spectroscopic ellipsometer operated at the principal angle of incidence and using a rotating analyzer combines the advantage of versatility with near maximum accuracy and sensitivity.

Power Devices

Use of Vacuum Tubes in Test Instrumentation for Measuring Characteristics of Fast High-Voltage Semiconductor Devices, Berning, D. W., *IEEE Trans. Instrumentation & Measurement* IM-30, 226-227 (1981).

Circuits are described that permit measurement of fast events occurring in power semiconductors. These circuits were developed for the dynamic characterization of transistors used in inductive-load switching applications. Fast voltage clamping using vacuum diodes is discussed, and reference is made to a unique circuit that was built for performing nondestructive, reverse-bias, second-breakdown tests on transistors.

Power MOSFET Temperature Measurements, Blackburn, D. L., and Berning, D. W., *PESC '82 Record, IEEE Power Electronics Specialists Conf. 1982*, Cambridge, Massachusetts, June 14-17, 1982, pp. 400-407.

Three temperature-sensitive electrical parameters are compared as thermometers for power MOSFET devices. The parameters are the forward drain-body diode voltage, the source-gate voltage, and the on-resistance. The results are also compared with temperatures measured with an infrared microradiometer. The procedure, apparatus, and circuits required to use each of the parameters as a thermometer are described. Some general considerations for measuring the temperature of power semiconductor devices are also discussed. Each parameter is found to be satisfactory for measuring the temperature of power MOSFETs. The source-gate voltage measures a temperature nearest to the peak device temperature, and the drain-body diode voltage shows the least variation in calibration from device to device.

Proceedings of Symposia

Semiconductor Measurement Technology: NBS/RADC Workshop, Moisture Measurement Technology for Hermetic Semiconductor Devices, II, Cohen, E. C., and Ruthberg, S., NBS Spec. Publ. 400-72 (April 1982).

The workshop, one of a series concerned with measurement problems in integrated circuit processing and assembly, served as a forum to examine the progress that has been made in the measurement and control of moisture in hermetically packaged semiconductor devices. While moisture-induced failure modes and mechanisms have been extensively documented, the lack of accurate and reliable measurement of the moisture content itself has been a major obstacle to meaningful efforts to limit and control this pervasive contaminant. Manuscripts are provided of 36 presentations which detail the progress that has been made in mass spectrometer measurements and calibration of internal package moisture, in increased assurance with moisture sensors, in testing, and in package control.

Process & Device Modeling

Upper Limits for the Number of Bound States Associated with the Yukawa Potential, Bennett, H. S., *J. Res. Natl. Bur. Standards* 86, 503-508 (September-October 1981).

The number of bound-state solutions of the Schrödinger equation for the screened Coulomb potential (Yukawa potential), $-(C/r)\exp(-\alpha r)$, occurs frequently in theoretical discussions concerning, for example, gas discharges, nuclear physics, and semiconductor physics. The number of bound states is a function of (C/α). Three upper limits for the number of bound states associated with the Yukawa potential are evaluated and compared. These three limits are those given by Bargmann, Schwinger, and Lieb. In addition, the Sobolev inequality states that whenever $(C/\alpha) < 1.65$ no bound state occurs. This agrees to within a few percent of the numerical calculations of Bonch-Bruevich and Glasko. The Bargmann and Lieb limits and the Sobolev inequality are substantially easier to evaluate than the Schwinger limit. Among the three limits, the Schwinger limit gives the most restrictive limit for the existence of only one bound state and, therefore, is the best one to use for the approach to no binding, i.e., $1.65 < (C/\alpha) \leq 1.98$. The Lieb limit is the best among the three when $(C/\alpha) > 1.98$. The Bargmann limit is the least restrictive.

Effect of Donor Impurities on the Density of States near the Band Edge in Silicon, Bennett, H. S., and Lowney, J. R., *J. Appl. Phys.* 52, 5633-5642 (1981).

Using the effective mass approximation and assuming that the scattering events for the electrons and holes by the assembly of donors are independent, we have calculated the effects of heavy doping on the conduction and valence states in silicon. When no bound-electron states associated with donors exist, the results show that: (1) the electron-donor interaction lowers the energy of the conduction and valence states, (2) band distortions occur, and (3) appreciable band-gap narrowing occurs. Our numerical results tend to support the band-gap estimates interpreted from optical measurements.

<u>Calculating Eigenvalues and Eigenfunctions Using an Interior Constraint</u>, Blue, J. L., and Wilson, C. L., *J. Computational Phys.* <u>44</u>, 70-83 (1981).

A new method for calculating eigenvalues and eigenfunctions of elliptic operators is presented. An interior constraint is used to allow reliable convergence to any desired eigenfunction. The method has been implemented in a portable Fortran computer program which features adaptively generated triangulations in two dimensions, and which uses multilevel iteration. The program has been used to calculate efficiently eigenvalues and eigenfunctions on singly- and multiply-connected regions, with internal and boundary singularities.

<u>CS1: A Two-Dimensional Finite Element Charge-Sheet Model of a Short-Channel MOS Transistor</u>, Wilson, C. L., and Blue, J. L., NBSIR 82-2471 (April 1982).

A two-dimensional charge-sheet model for short-channel MOS transistors has been developed. The unique feature of the model is that the effect of channel inversion layer charge is included as a nonlinear integral boundary condition on the two-dimensional electrostatic field in the transistor. The average inversion layer charge density and source-drain current are obtained directly from the model rather than from the electron density or electron quasi-Fermi level. The model retains all of the physical detail of more complex two-dimensional models such as sensitivity to source-drain profile shape, channel profile, and oxide field shape. This allows the model to represent the changes in drain current associated with short-channel effects while still allowing simple comparison with long-channel models. For long-channel transistors, the results of this model are identical to Brews' long-channel charge-sheet model. The accuracy of this model is verified by modeling a sequence of transistors with channel lengths between 4.6 and 1.1 μm. In short-channel transistors, effects previously attributed to high field mobility are explained by simple two-dimensional electrostatics.

The simulations produced using this model have been compared to experimental measurements on an array of n-channel MOSFETs; the model is in good agreement for transistors with channel lengths as short as 1.1 μm. In this verification process, the model represented accurately the onset of subthreshold current, channel-length-induced threshold voltage offset, and drain-field-induced output conductance changes.

From studies of numerical accuracy, we conclude that the charge-sheet model can easily simulate drain current with an accuracy which exceeds that required for most applications. To obtain 5-percent accuracy for drain current, a 146 element mesh is sufficient. Refinement of the 146 element mesh to a 455 element mesh gives a current which is accurate to 0.16 percent. Average computer time for a high accuracy solution is 2.5 min on a DEC-20.

The numerical solutions were obtained using general-purpose software for solving elliptic partial differential equations. Problems with exact solutions have been solved to test the correctness and accuracy of the codes. Also, the physics included in this model and the geometry of the transistor can be easily changed. The finite element method used allows refinement of oblique triangles which is important in achieving computational efficiency. The program is portable and has been run on a DEC-20, a VAX 11/780, a Cyber 175, and a Univac 1108.

Two-Dimensional Finite Element Charge-Sheet Model of a Short-Channel MOS Transistor, Wilson, C. L., and Blue, J. L., *Solid-State Electronics* 6, 461-477 (1982).

A two-dimensional charge-sheet model for short-channel MOS transistors has been developed. The unique feature of the model is that the effect of channel inversion layer charge is included as a nonlinear integral boundary condition on the two-dimensional electrostatic field in the transistor. The average inversion layer charge density and source-drain current are obtained directly from the model rather than from the electron density or electron quasi-Fermi level. The model retains all of the physical detail of more complex two-dimensional models such as sensitivity to source-drain profile shape, channel profile, and oxide field shape. This allows the model to represent the changes in drain current associated with short-channel effects while still allowing simple comparison with long-channel models. For long-channel transistors, the results of this model are identical to Brews' long-channel charge-sheet model. The accuracy of this model is verified by modeling a sequence of transistors with channel lengths between 4.6 and 1.1 μm. In short-channel transistors, effects previously attributed to high field mobility are explained by simple two-dimensional electrostatics.

The Effect of Bandgap Narrowing on Diffusion Processes in Silicon, Lowney, J. R., *VLSI Science and Technology /1982*, C. J. Dell'Oca and W. M. Bullis, Eds., pp. 123-129 (ECS, Pennington, N.J., 1982).

As the dimensions of devices become smaller, the effect of bandgap narrowing, which occurs in silicon as a result of heavy doping, becomes increasingly more important. The diffusion coefficients of dopant ions depend strongly on the ratio of the majority carrier density to the intrinsic carrier density, which increases with decreasing energy gap. A model has previously been developed, restricted to donors, which accounts for the bandgap narrowing observed optically at 35 and 300 K. These results have been extended to the case of a donor density of 1.0×10^{20} cm^{-3} at 1100°C, for which this model predicts a bandgap reduction of 123 meV. However, the intrinsic carrier density is increased by only 15 percent because the perturbed bands are nonparabolic. It is concluded that bandgap narrowing resulting from heavy doping has a much smaller effect on diffusion coefficients than predicted by a prior model which unlike this work is based on impurity bands. This calculation indicates that there may be near cancellation between the effect of bandgap narrowing and that of degenerate statistics which is consistent with the linear dependence of the arsenic diffusion coefficient on electron concentration.

Probe-Spacing Experiment Simulation and the Relation Between Spreading Resistance and Sheet Resistance, Albers, J., *J. Electrochem. Soc.* 129, 599-605 (1982).

Recently, Dickey has proposed that the two-probe spreading resistance measured on the surface of a thin, nonuniform, junction-isolated layer is a linear function of the natural logarithm of the probe separation with a slope proportional to the sheet resistance and an intercept related to the probe radius. Model spreading resistance data generated from the multilayer solution of Laplace's equation were used to test the validity of this relation between spreading resistance and sheet resistance. The model data were meant to simulate diffusions or implants into same conductivity type as well as junction-isolating substrates. For a junction-type structure, the model data indicate that probe-spacing experiments will yield the correct sheet resistance in the surface region, but that the intercept is not related to the radius. The same conclusion is obtained for a heavily doped layer over a substrate of the same conductivity type. For lightly and moderately doped layers over a substrate of the same conductivity type, the relation between the spreading resistance and the sheet resistance is found not to hold.

Effect of Donor Impurities on the Conduction and Valence Bands of Silicon, Lowney, J. R., and Bennett, H. S., *J. Appl. Phys.* 53, 433-438 (1982).

The energy shifts of valence and conduction band states in silicon due to the interaction of electrons and holes with ionized donors have been calculated by performing a partial wave analysis. The potential is modeled by the Yukawa form with the screening radius determined self-consistently by the Friedel sum rule. The results show that this effect is an important part of the optically measured band-gap narrowing. The variation of the Fermi energy due to this phenomenon is also calculated.

Effect of Impurity Pairs on the Disappearance of Impurity Levels in Silicon, Kahn, A. H., and Lowney, J. R., *J. Appl. Phys.* 53, 454-456 (1982).

We report calculations of the binding energy of an electron to a pair of charged donor ions in the presence of screening by free carriers. The effective-mass approximation was assumed. We used a two-dimensional finite-element analysis to obtain numerical solutions, as we did in a previous study of the screening of single donor ions. The ground state was found to disappear into the conduction band at a doping level of 1.27×10^{19} cm^{-3}, at 300 K, with a uniform distribution of donors. The results support the conclusion that at doping levels of 2×10^{19} cm^{-3} or higher, the density of electronic states in silicon contains no contribution from localized boundary impurity levels.

Radiation Effects

VDMOS Power Transistor Drain-Source Resistance Radiation Dependence, Blackburn, D. L., Robbins, T. C., and Galloway, K. F., *IEEE Trans. Nucl. Sci.* NS-28, 4354-4359 (1981).

Data on the effects of neutron and gamma radiation on the drain-source resistance characteristics of power VDMOS transistors are presented. The change in resistance with neutron exposure is related to the resistivity of the drain material, which in turn can be related to the drain-source breakdown voltage. A device with a 450-V rating experienced a factor of 13 increase in resistance on exposure to a neutron fluence of $10^{14}/cm^2$ whereas one with a breakdown voltage of 150 V experiences no increase in resistance. Threshold voltage shifts of about 2 V occurred at a gamma dose of 10^5 rad(Si) without bias and was accelerated by positive gate bias. All of these data are consistent with the predictions of a simple model for the dependence of drain-source resistance on gate voltage and drain resistivity. This model illustrates a general separability of neutron and gamma effects on power VDMOS devices. The systems implications for using this type of device in a radiation environment are briefly addressed.

Temperature Dependence of Transient Electron Radiation Upset in TTL NAND Gates, Leedy, T. F., McLane, G. F., and Guenzer, G. C., *IEEE Trans. Nucl. Sci.* NS-28, 4597-4605 (1981).

The temperature dependence of transient upset caused by a 40-MeV electron flux was investigated for junction-isolated gold-doped and nongold-doped TTL NAND gate devices in the temperature range from 20 to 125°C. Data for five devices are presented. Over this temperature range, the dose rate required to upset the logical 1 and logical 0 output levels of the gate increased by a factor of between 2 and 3 for the gold-doped devices, but remained essentially constant for the nongold-doped (Schottky) devices. Schottky-clamped devices are not gold-doped, and the gold-doped devices did not employ Schottky clamps. A correlation was observed between the temperature dependence of the upset dose rate and the collector-substrate depletion width as determined from capacitance measurements for both device types. It is proposed that nearly all of the upset photocurrent for gold-doped devices is generated in the collector-substrate depletion region and that variations in the depletion width with temperature cause the observed results.

Miscellaneous

Measurements for Commercial Photovoltaics: A Status Report, Schafft, H. A., *Proc. Commercial Photovoltaics Measurements Workshop,* Vail, Colorado, July 17-19, 1981, pp. 275-278.

The first part of this report discusses how reliable measurements play an important role along the chain of supplier-user links that make up the photovoltaics industry and its customers. Such measurements provide accurate information on materials, fabrication processes, product characterization, and product needs upon which sound decisions can be made to optimize the performance of processes and products. They also are indispensable for effective communication in the market place. The second part reviews the results of industry visits to identify measurements-related issues that affect the expeditious development and application of photovoltaics. The results are organized into nine categories: (1) silicon characterization; (2) quality assurance; (3) electrical measurements of solar cells and modules (including accuracy and reproducibility of measurements, spectral response, reference cells, and simulators and spectral distribution); (4) solar data; (5) interactions with customers; (6) measurement equipment; (7) module certification; (8) standards; and (9) role of government. The third part of the report provides an overview of measurement and standards development activities. The intent of this is to promote an awareness of such work to encourage thereby greater participation and also timely use of the results of this work.

Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1979 to September 30, 1980, Larrabee, R. D., Phillips, W. E., and Thurber, W. R., NBSIR 81-2325 (September 1981).

The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during crystal growth and during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The effective utilization of deep-level measurements for this purpose requires three things: (1) development of well-characterized measurement and data analysis procedures, (2) characterization of a variety of levels to establish the validity of the techniques and establishing a data bank of the properties of known defect levels, and (3) understanding the relationship between the properties of deep levels and the corresponding device parameters. Efforts in deep-level metrology during the present reporting period were concentrated specifically on the first and third of these basic requirements. This effort is divided into two ongoing tasks concerned with (1) the introduction of specific impurities into silicon wafers and the characterization of the resulting deep levels and (2) the correlation of the results of these deep-level characterization techniques with the electrical properties of devices. A third task concerned with the standardization of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon was essentially completed during the year.

Integrated Circuit Metrology, Bullis, W. M., *EDN Magazine* 26 (20), 120-122, 127 (October 14, 1981).

Projected trends in integrated circuit metrology during the next quarter century are discussed. The picture that emerges for the IC factory of 2006 is one of extensive computer control of both fabrication and characterization based on more complete understanding of the materials and processes employed. The metrological advances which will occur in the next quarter century may be expected both to enhance our fundamental understanding of the solid state and to provide the means for reliable and economical manufacture of more complex and more powerful integrated circuits.

Reference Materials and the Semiconductor Industry, Bullis, W. M., and Ehrstein, J. R., *Solid State Technology* 24 (11), 56-63 (November 1981).

The development of increasingly sophisticated semiconductor technologies such as VLSI will put increasingly stringent demands on materials and fabrication processes as well as on the measurement techniques used to characterize them. The advent of many new measurement techniques and instructions, often noncontacting and automatic, has offered convenience to the user, but many times it is at the price of measurements which are inconsistent with those obtained by more traditional techniques. The Standard Reference Materials (SRM) program at the National Bureau of Standards, which provides calibrated artifacts to various user communities, is one approach for improving measurement accuracy and compatibility. This article describes the SRM program at NBS and the requirements for effective utilization of SRMs. Application of the SRM program to the semiconductor industry is discussed both with respect to present and planned SRMs and with regard to meeting the more extensive and longer range needs of the industry.

Gallium Arsenide Materials Characterization: Annual Report, October 12, 1978 to October 12, 1979, Ehrstein, J. R., and Seabaugh, A. C., NBSIR 81-2403 (December 1981).

Ohmic and Schottky barrier contacts for use in electrical characterization were examined both conceptually and experimentally with particular focus on the problems associated with ohmic contacts to semi-insulating GaAs. The conductivity type of the semi-insulating material, which can be either *n*- or *p*-type, was investigated by means of a potential profiling technique. In addition, the feasibility of spreading resistance measurements was examined and applied to both low resistivity bulk GaAs and ion-implanted semi-insulating substrate material.

Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1980 to December 31, 1981, Thurber, W. R., Phillips, W. E., and Larrabee, R. D., NBSIR 82-2552 (August 1982).

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. Emphasis is on the development of measurement methods for power-device grade silicon. Major accomplishments during this reporting period were: (1) characterizing by deep level transient spectroscopy (DLTS) the energy levels in silicon power rectifier diodes, (2) writing of a computer program to predict lifetime-related parameters using as input the measured properties of the deep energy levels, (3) developing a novel method to detect nonexponential transients using a conventional double-boxcar DLTS system, (4) analyzing transient capacitance measurements to extend the techniques to nonexponential decays, (5) using a platinum resistance thermometer to calibrate temperature sensing diodes to obtain the precision needed for careful isothermal capacitance measurements, and (6) utilizing trap charging time as a technique to resolve overlapping DLTS peaks in sulfur-doped silicon.

Publications in Press . . .

Albers, J., Spreading Resistance Probe-Spacing Experiment Simulations: Effects of Probe-Current Density and Layer Thickness, *J. Electrochem. Soc.*

Bennett, H. S., Improved Device Physics for Calculating the Gain of Bipolar Structures in Silicon, *Proc. Workshop on Submicron Physics.*

Blackburn, D. L., Berning, D. W., Benedetto, J. M., and Galloway, K. F., Ionizing Radiation Effects on Power MOSFETs During High Speed Switching, *IEEE Trans. Nucl. Sci.*

Buehler, M. G., and Linholm, L. W., The Role of Test Chips in Coordinating Logic and Circuit Design and Layout Aids for VLSI, *Proc. 2d Cal. Tech. Conf. on VLSI.*

Chandler-Horowitz, D., Ellipsometric Accuracy and the Principal Angle of Incidence, *Proc. Soc. Photo-Optical Instrum. Engrs.* 342.

Harman, G. G., and Harmison, K. A., The Assessment of Hybrid Package Glass-Metal Seal Reliability Using Acoustic-Emission Measurement Techniques, *Int. J. for Hybrid Microelectronics.*

Jerke, J. M., Croarkin, M. C., and Varner, R. N., *Semiconductor Measurement Technology:* Interlaboratory Study on Linewidth Measurements for Antireflective Chromium Photomasks, NBS Spec. Publ. 400-74.

Jerke, J. M., and Wendell, C. E., Use of the NBS AR-Chromium Optical Linewidth Standard for Measurements on Other Types of Chromium Photomasks, *Proc. Soc. Photo-Optical Instrum. Engrs.* 342.

Nyyssonen, D., Design of an Optical Linewidth Standard Reference Material for Wafers, *Proc. Soc. Photo-Optical Instrum. Engrs.* 342.

Nyyssonen, D., Theory of Optical Edge Detection and Imaging of Thick Layers, *J. Opt. Soc. Am.*

Proctor, S. J., and Linholm, L. W., A Direct Measurement of Interfacial Contact Resistance, *IEEE Electron Devices Letters.*

Ruthberg, S., Leak Testing of Hermetically Sealed Electronic Components, *Proc. Qualtest I, ASNT.*

Ruthberg, S., *Semiconductor Measurement Technology:* Graphical Solution for the Helium Leak Detector and Radioisotope Methods of Hermetic Test, Master Graphs and Instructions, NBS Spec. Publ. 400-73.

Thurber, W. R., Forman, R. A., and Phillips, W. E., A Novel Method to Detect Nonexponential Transients in DLTS, *J. Appl. Phys.*

Yen, D., Electrical Test Methods for Evaluating Lithographic Processes and Equipment, *Proc. Soc. Photo-Optical Instrum. Engrs.* 342.

Yen, D., Linholm, L. W., and Buehler, M. G., A Cross-Bridge Test Structure for Evaluating the Linewidth Uniformity of an Integrated Circuit Lithography System, *J. Electrochem. Soc.*

Yen, D., Linholm, L. W., and Proctor, S. J., Recent NBS Work on IC Test Structures for Measurement of Process Parameters, *Proc. Microelectronics Measurement and Test Conf.*

Wilson, C. L., and Blue, J. L., Modeling of Ionizing Radiation Effects in Short-Channel MOSFETs, *IEEE Trans. Nucl. Sci.*

Scheduled Symposia

Two identical four-day training seminars on Linewidth Measurements on Integrated Circuit Photomasks and Wafers are being held in Palo Alto, California on March 1-4 and 7-10, 1983. These are the sixth and seventh in a series of seminars designed to assist in transferring measurement technology developed at NBS to those in the semiconductor community concerned with linewidth measurement and control. These seminars present up-to-date information on the accurate and precise measurement of linewidths in the 0.5- to 10-μm range. Lectures and discussions will cover the theory and problems associated with optical measurements of linewidths on photomasks in transmitted light and linewidths on patterned wafers in reflected light. The dependence of reflected-light measurements on the optical properties of materials will be stressed with emphasis on the differences that occur between measurements on thick and thin dielectric and metallic layers on wafers. Statistical lectures will include a discussion of data analysis, derivation of calibration curves based on the NBS linewidth standards, and control chart methods. [D. Nyyssonen, x3786]

The IEEE CHMT Society and NBS are jointly sponsoring a VLSI Chip Packaging Workshop to be held in Gaithersburg on September 12-13, 1983. New developments and critical overviews in the following areas will be presented: package design and evaluation, hermetic, plastic; package thermal design, characteristics, problems, and test methods; bonding and interconnections for high lead count devices; coordinated chip, interconnection, and package design, including design for automatic assembly; materials for VLSI packaging; die attach methods and problems for large chips; and new package-related failure mechanisms.
[G. G. Harman, x3621]

The IEEE Electron Devices Society and NBS are co-sponsoring the Power Semiconductor Devices Workshop scheduled for December 8, 1983 in Gaithersburg, Maryland. The workshop is designed to bring together those actively working in the field of power semiconductor devices and will be held in conjunction with the IEEE International Electron Devices Meeting in Washington, D.C.
[F. F. Oettinger, x3541]

A Symposium on Semiconductor Processing scheduled for February 6-10, 1984, will be sponsored by ASTM and co-sponsored by NBS, SEMI, and Stanford University. Technical sessions will address new problems arising from rapid increases in device complexity and performance and the emergence of integrated systems-on-a-chip, automated factories, and silicon foundries. [R. I. Scace, x3786]

Co-sponsored by IEEE and NBS, the Power Electronics Specialist Conference, Gaithersburg, Maryland, June 18-21, 1984 will bring together specialists in circuits, systems, electron devices, magnetics, control theory, instrumentation, and power engineering for discussions of new ideas, research, development, applications, and the latest advances in power electronics.
[F. F. Oettinger, x3541]

Recent Seminars and Workshops

The Symposium on Silicon Processing sponsored by ASTM, NBS, and Stanford was held in San Jose, California, on January 19, 1982. Proceedings of this symposium are available from ASTM, 1916 Race Street, Philadelphia, Pennsylvania 19103.

The Society of Photo-Optical Instrumentation Engineers and NBS co-sponsored a meeting on Integrated Circuit Metrology at the 1982 Technical Symposium East in Arlington, Virginia on May 4-5, 1982. Four talks by Division personnel were presented. The Proceedings, Volume 342, are available from SPIE, Box 10, Bellingham, Washington 98227.

The Fourth Biennial International Neutron Transmutation Doping Conference was held at NBS on June 1-3, 1982. The purpose of these NTD conferences is to exchange ideas and discuss latest developments in areas related to the production, characterization, processing, and application of neutron-doped semiconductors. The proceedings of the conference will be published by Plenum Press.
[R. D. Larrabee, x3786]

A two-day limited attendance VLSI Packaging Workshop was held in Gaithersburg, Maryland on September 13-14, 1982. The workshop was jointly sponsored by NBS and the CHMT Society of the IEEE. Copies of the program and extended abstracts of the talks are available.
[G. G. Harman, x3621]

Conference Presentations

IEEE Nuclear and Space Radiation Effects Conf., University of Washington, Seattle, Washington, July 21-24, 1981
- Galloway, K. F., Blackburn, D. L., and Robbins, T. C., VDMOS Power Transistor Drain-Source Resistance Radiation Dependence

Commercial Photovoltaics Measurements Workshop, Vail, Colorado, July 27, 1981
- Schafft, H. A., Measurements for Commercial Photovoltaics - A Status Report
- Scace, R. I., Solar Grade Silicon Specification by the Semiconductor Equipment and Materials Institute

American Institute of Aeronautics and Astronautics, Outlook for VHSIC Applications and Technology, Washington, DC, August 4, 1981 and Boston, Massachusetts, September 4, 1981
- Scace, R. I., Metrology for VLSI - Where We Are and Where We Are Going

1981 SEMICON/EAST, Boston, Massachusetts, September 22-24, 1981
- Russell, T. J., Wilson, C. L., Linholm, L. W., and Roitman, P., Microelectronic Test Structures for Process and Device Models

1981 SOS Technology Workshop, Sunriver Resort, Sunriver, Oregon, October 6-8, 1981
- Linholm, L. W., Analyzing Critical CMOS/SOS Process Parameters Using Microelectronic Test Structures

Symposium on Silicon Processing, San Jose, California, January 19, 1982
- Scace, R. I., NBS Work for the Semiconductor Industry: Introductory Remarks

Microelectronic Measurement Technology Seminar, San Jose, California, March 22, 1982
- Yen, D., Linholm, L. W., and Proctor, S. J., Recent NBS Work on IC Test Structures for Measurement of Process Parameters

Society of Photo-Optical Instrumentation Engineers, Arlington, Virginia, May 4, 1982
- Chandler-Horowitz, D., Ellipsometric Accuracy and the Principal Angle of Incidence
- Jerke, J. M., Use of the NBS AR-Chromium Optical Linewidth Standard for Measurements on Other Types of Photomasks
- Nyyssonen, D., Design of an Optical Linewidth Standard Reference Material for Wafers
- Yen, D., Electrical Test Methods for Evaluating Lithographic Processes and Equipment

S.P.S.E. 35th Annual Conference, Rochester, New York, May 9-14, 1982
- Bennett, W. O., and Nyyssonen, D., Mathematical Modeling of a Laser Microspot Scanning Reflection Measuring Microscope

Electronics Components Conference (IEEE), San Diego, California, May 10-12, 1982
- Harman, G. G., Acoustic Emission Monitored Tests for TAB Inner Lead Bond Quality

1982 Spring Meeting of the Electrochemical Society, Inc., Montreal, Canada, May 13, 1982
- Proctor, S. J., and Linholm, L. W., A Microelectronic Test Structure for Measuring Contact Resistance in Integrated Circuits

1982 Computer Elements Workshop (IEEE), New York, May 21, 1982
- Linholm, L. W., The Role of Integrated Circuit Test Structures for Evaluating VLSI Circuits

IEEE Power Electronics Specialists Conf., Cambridge, Massachusetts, June 14-17, 1982
- Blackburn, D. L., and Berning, D. W., Power MOSFET Temperature Measurements

Device Research Conference, Ft. Collins, Colorado, June 21-23, 1982
- Russell, T. J., Wilson, C. L., and Gaitan, M., Measurement of Interface Trapped Charge in Short-Channel MOSFETs
- Wilson, C. L., Roitman, P., and Albers, J., Verification of Models for the Annealing of Arsenic Implants
- Bennett, H. S., Improved Models for Predicting the Gain of Bipolar Structures in Silicon

Physics of Submicron Structures Workshop, Urbana-Champaign, Illinois, June 28, 1982
- Bennett, H. S., Device Physics for Bipolar Structures in Silicon

IEEE Nuclear and Space Radiation Effects

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

This report provides abstracts of recent publications of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Topics include: defects and impurities, IC test structures, micrometrology, packaging, physical analysis, power devices, process and device modeling, and radiation effects. In addition, publications in press and conference presentations are listed. Information is also given on recent seminars, workshops, and symposia and those scheduled for the near future.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

Compound semiconductors; electronics; GaAs; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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- Wilson, C. L., and Blue, J. L., Modeling of Ionizing Radiation Effects in Short-Channel MOSFETs
- Blackburn, D. L., Berning, D. W., Benedetto, J. M., and Galloway, K. F., Ionizing Radiation Effects on Power MOSFETs During High Speed Switching

IEEE VLSI Packaging Workshop, Gaithersburg, Maryland, September 14, 1982

- Harman, G. G., How the "New Technology" Has Changed and Increased Classical Package-Related Failure Modes
- Oettinger, F. F., and Albers, J., Thermal Test Chips for VLSI Package Evaluation

ICALEO '82, Laser Institute of America, Boston, Massachusetts

- Nyyssonen, D., Laser Micrometrology for Integrated Circuits

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