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...surement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1980 to December 31, 1981

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Semiconductor Materials and Processes Division
Washington, DC 20234

August 1982

Prepared for
Department of Energy
...vision of Electric Energy Systems
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MEASUREMENT TECHNIQUES FOR HIGH POWER SEMICONDUCTOR MATERIALS AND DEVICES: ANNUAL REPORT, OCTOBER 1, 1980 TO DECEMBER 31, 1981

W. R. Thurber, W. E. Phillips, and R. D. Larrabee

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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PREFACE

This work was conducted as a part of the Semiconductor Technology Program at the National Bureau of Standards (NBS). This program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems of the Department of Energy (DOE) under DOE Task Order A021-EES. The contract is monitored by Mr. Kenneth Klein of DOE. The NBS point of contact for information on the various task elements of this project is R. D. Larrabee of the Semiconductor Materials and Processes Division at the National Bureau of Standards.

The authors would like to acknowledge guidance and support from R. A. Forman, J. R. Lowney, and many other colleagues at the National Bureau of Standards.

Measurement Techniques for High Power
Semiconductor Materials and Devices

ANNUAL REPORT
October 1, 1980 to December 31, 1981

W. R. Thurber, W. E. Phillips, and R. D. Larrabee

1. INTRODUCTION AND EXECUTIVE SUMMARY

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. Application of this measurement technology will, for example, enable industry to make devices with higher individual power-handling capabilities, thus permitting reductions in the cost of power-handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major effort under this continuing program is to determine procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce lifetime or contribute to leakage current in power-device grade silicon. This effort is divided into two ongoing tasks concerned with (1) the correlation of the results of deep-level characterization techniques with the electrical properties of devices and (2) the introduction of specific impurities into silicon wafers and the characterization of the resulting deep levels.

The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during crystal growth and during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. In either case, the dominant effect of the deep level is to modify the excess-carrier lifetime. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The use of such techniques for process diagnostics would enhance the manufacturer's ability to control the quality (yield, reliability, and cost) of his product. The effective utilization of deep-level measurements requires three things: (1) developing well-characterized measurement and data analysis procedures, (2) characterizing a variety of levels to establish the validity of techniques and establishing a data bank of the properties of known defect levels, and (3) understanding the relationship between the presence of deep levels and the corresponding device parameters. Efforts in deep levels during this contract period were aimed specifically at the first and third of these basic requirements.

Correlation to Device Performance - Deep-level defects in the silicon bandgap play an important role in determining the behavior of high-power devices. These defects control the excess-carrier lifetime in the active regions of devices and consequently control such electrical parameters as reverse leakage current, forward voltage drop, and switching speed. Therefore, it is important to understand the nature of the mechanism of excess-carrier recombination and its effects on relevant device parameters. One test of the depth of understanding that has been achieved is to determine the degree of correlation between lifetime measurements and the results of modeling the behavior of the excess-carrier lifetime as a function of the measured deep-level characterization parameters. Previous reports have presented the results of experiments where such a correlation was demonstrated qualitatively in specially prepared gold-doped specimens. The present continuing effort is directed at demonstrating this correlation quantitatively in real device material.

Previous work has shown that the deep-level transient spectroscopy (DLTS) curves obtained from diodes commercially fabricated on rectifier material exhibit overlapping positive and negative peaks. A typical DLTS curve shows two or three positive peaks and five negative peaks, which suggests that many levels may be important in determining the recombination properties of the material. In addition, the absolute and relative densities of the levels vary with position on the wafer. Consequently, a major thrust of the work this year was to understand the many features of these DLTS curves in preparation for later correlation of the DLTS results with the lifetime-related parameters. Since the positive peaks were thought to arise from extraneous surface or near-surface hole traps, efforts were directed toward eliminating the contribution of these traps; and a DLTS curve representing only the bulk traps was obtained and resolved into five well-characterizable peaks.

A computer program was written for predicting the excess-carrier lifetime of multilevel systems given the density, activation energy, and carrier capture cross sections of all the states in the bandgap. The program computes a variety of lifetime-related parameters as a function of temperature. The purpose of the program is to determine how well the calculated lifetime compares with values measured experimentally. In order for the predicted lifetimes to agree with the measured values over a range of experimental conditions, it is necessary that: (1) the techniques used to measure the thermal emission rates and the models used to convert these rates to activation energies and capture cross sections be not only accurate, but also fully relevant to lifetime-related applications, (2) the algorithm of the computer program accurately model the details of the carrier-recombination mechanism and include all pertinent variations of the parameters with experimental conditions, and (3) the technique used to measure the lifetime for purposes of comparison produce meaningful results that approximate the conditions assumed in the computer model. If the predicted and measured values of lifetime do not agree, it would indicate that one or more of these factors is not true or is not completely understood and under control. It is believed that a study of this kind, directly demonstrating the utility of deep-level measurements to lifetime prediction in actual device material, is one prerequisite for a more widespread acceptance and utilization of deep-level measurements by the power-device community.

Deep-Level Measurement Procedures - The ability to detect both intentional and unintentional impurities in order to take corrective action when necessary would greatly enhance the manufacturer's capability to control the quality of his product. The rapid identification and quantification of deep-level states require a prior knowledge of the characteristics of each energy level. However, there are often a number of different values of activation energy reported in the literature for material doped with the same impurity. It is probable that some of the discrepancies can be attributed to measurement problems in general (e.g., nonexponential transients and inaccurate thermometry) and to variability unintentionally introduced by differences in the processing of test devices or experimental conditions during the measurement. During this reporting period, work was undertaken on several measurement and data analysis procedures designed to improve the accuracy and precision of the parameters derived from deep-level measurements. The following paragraphs summarize each of the procedures:

1. A novel method to detect nonexponential transients using a conventional double-boxcar deep-level transient spectroscopy system was investigated and found to be sufficiently sensitive to examine typical cases of interest. It relies only on the reproducibility of the instrumentation, not on its absolute accuracy.

2. A more rigorous analysis was made of the capacitance transient in a space charge layer due to thermal emission from charged defect centers in a semiconductor depletion region. This analysis extends the range of applicability of capacitance-transient defect characterization techniques to nonexponential transient conditions such as those found either in heavily doped diodes or when defect centers are charged in only a part of the depletion region. The analysis was also applied to the more widely used DLTS method. This results in a correction term to the conventional equation used to model DLTS time constants.

3. Precision thermometry continues to be an essential concern for the accurate identification and characterization of electrically active defect centers in semiconductors by deep-level measurement techniques. The use of a platinum resistance thermometer to calibrate the temperature-sensing diodes, which measure the temperature of the device under test, was instituted and found to give more than an order of magnitude improvement over the previously used technique employing a thermocouple.

4. Closely spaced energy states in sulfur-doped silicon were resolved by obtaining DLTS curves as a function of trap charging time. This procedure, which depends upon the states in question having significantly different capture rates, will have applicability to other situations where overlapping peaks occur that cannot be resolved by more conventional DLTS techniques.

2. CORRELATION TO DEVICE PERFORMANCE

2.1 Task Objective

Deep-level defects in the silicon bandgap play an important role in determining the behavior of high-power devices. Impurity-related defects can be added intentionally (e.g., to control switching speed) or can result from contamination contained in the starting material or introduced during the crystal growth process or during high-temperature device processing operations. In any event, impurity-related defects can control the excess-carrier recombination lifetime in the active regions of bipolar devices. In this way, they can affect such electrical parameters as reverse leakage current, forward voltage drop, and switching speed. Therefore, it is important to understand the nature of these lifetime-controlling defect states and their effects on the relevant device parameters.

Traditional transient-capacitance techniques such as deep-level transient spectroscopy (DLTS) and isothermal transient capacitance (ITCAP) measure the emission properties, rather than the recombination properties, of deep levels. Therefore, some modeling is necessary to relate the measured thermal emission properties to the desired recombination properties such as the carrier capture cross sections and thermal activation energies of the recombination centers. Since the modeling will necessarily involve assumptions and simplifications, it is not a foregone conclusion that the results will adequately relate the thermal emission results to the carrier recombination properties. This has been one factor limiting the utilization of deep-level techniques in industry and motivating a search for ways to measure recombination properties directly.

The emphasis of this continuing task is to test the depth of understanding that has been achieved by determining the degree of correlation between the results of deep-level measurements *per se* and the results of modeling the behavior of excess-carrier recombination lifetime as a function of the measured transient-capacitance thermal-emission parameters. The ultimate goal is the establishment of better techniques for utilizing the results of deep-level measurements for device diagnostic and process-control purposes.

2.2 Approaches Being Pursued

The work on deep-level characterization of commercially available power rectifier diodes has proceeded in the direction of understanding and correlating the results obtained from DLTS measurements with the results of lifetime-related measurements on the same diode. Previous work [2-1] has shown that the DLTS curves obtained from a particular lot of diodes exhibit overlapping positive and negative peaks. A typical DLTS curve shows two or three positive peaks and five negative peaks, which suggests that many levels may be important in determining the excess-carrier recombination properties of this material. In addition, the absolute and relative densities of the levels vary with position on the wafer. Consequently, a major thrust of the work this year was to understand the many features of the DLTS curves in preparation for later correlation of the DLTS results with the lifetime-related parameters. Since the positive peaks were thought to arise from surface or near-surface hole traps, efforts were directed toward eliminating the contribution of these traps and thus obtaining a DLTS curve representative of the bulk states. The justification for studying only the negative peaks is that they arise from traps in the bulk silicon and are much more important than surface traps in determining the recombination properties of these large diodes. Majority carrier DLTS (reverse bias only) measures traps in only the majority-carrier half of the bandgap. Traps in the other half may be equally important and can often be seen with forward bias trap-filling conditions. However, our experience on other specimens suggests that this response is weaker and that a null result does not mean that traps in the minority-carrier side of the bandgap are absent. Additional efforts are planned to find the most effective technique to measure the recombination centers throughout the bandgap of this rectifier material.

A FORTRAN computer program has been written for predicting the excess-carrier recombination lifetime in multilevel systems. The program follows the theoretical background presented in last year's annual report [2-2] and can handle up to three donor and three acceptor states in the bandgap of silicon. The program accepts the density, activation energy, degeneracy, and carrier cross sections of these bandgap states and then calculates a variety of lifetime-related parameters as a function of temperature. In order for the predicted lifetime to agree with the measured lifetime over a range of experimental conditions, it is necessary that: (1) the techniques used to measure the thermal emission rates and the models used to convert these rates to activation energies and capture cross sections be not only accurate, but also fully relevant to lifetime-related applications; (2) the algorithm of the computer program accurately model the details of the carrier-recombination mechanism and include all pertinent variations of the parameters with experimental conditions; and (3) the technique used to measure the lifetime for comparison purposes produce meaningful results that approximate the conditions assumed in the computer model. If the predicted and measured values of lifetime do not agree, it would indicate that one or more of these factors is not true or is not completely understood and under control. It is believed that a study of this kind directly demonstrating the utility of deep-level measurements to lifetime prediction in actual device material, is one prerequisite for a more widespread acceptance and utilization of deep-level measurements by the power-device community.

2.3 Accomplishments During Reporting Period

2.3.1 DLTS Measurements of High-Voltage Rectifier Material

Considerable progress was made in understanding the DLTS curves obtained on mesa-diode devices commercially fabricated on a wafer of high-resistivity n-type silicon for use as high-voltage rectifiers. Efforts were concentrated on the study and elimination of the positive peaks due to surface states in order to obtain a simpler DLTS curve representative of only the bulk n-type region. This should lead to a better correlation of the defect parameters measured by DLTS with the measured lifetime-related parameters. In last year's report, it was tentatively postulated that the positive DLTS peaks were due to surface, or near-surface, hole traps. Work this year has confirmed that the peaks originate from material at or near the surface and thus are not important as bulk recombination centers in these large volume devices.

The evidence in support of the view that the positive (minority carrier) peaks are due to surface traps includes the following observations: (1) They are present even when the trap-charging pulse does not go into forward bias which implies band bending at the surface as the source of minority carriers. (2) Their magnitude increases with increasing duration of the trap-charging pulse: The negative peaks are saturated with a charging pulse of less than 30 µs, whereas the positive peaks are still growing at 300 µs. (3) They are much larger at higher temperatures for a fixed charging pulse. (4) Their size depends greatly on the DLTS bias voltage sequence. For example, peaks seen with -5,0,-5 V* are almost completely absent with a -17,-7,-17 V sequence; the reverse is also true.

To examine the stability of the DLTS curve, a diode was scribed from the parent wafer and annealed at 450°C for 1 h in nitrogen. The DLTS curves of this device before and after this heat treatment are shown in figure 2-1. The higher temperature positive peaks were essentially eliminated, but the lower temperature positive peaks were greatly enhanced. The negative peaks, some only a shallow depression in a large positive peak, showed no significant change. This is further evidence that the positive peaks represent process-sensitive surface states, whereas the negative peaks represent stable bulk states.

To change and possibly eliminate the positive peaks, chemical treatments were undertaken on another scribed-out device. The results before and after the treatments are shown in figure 2-2. The HF soak removed the silicon nitride passivation and the underlying silicon dioxide because of undercutting originating at the scribe lines. One positive peak was greatly reduced and another greatly increased by this HF treatment. The device was then boiled in deionized water to change the surface potential. This eliminated all of the positive peaks for the -5,0,-5 V bias sequence shown in figure 2-2 and greatly reduced the positive peaks formerly present with the -17,-7,-17 V sequence. No major change was seen in any of the negative peaks. Finally, the device was etched in an HF-HNO_3 solution to remove about 5 µm of silicon from exposed areas and then boiled in water. The DLTS curves were essentially the same as those following the boiling-water-only treatment. The results of these treatments strongly suggest that only the negative peaks are associated with bulk defects.

By optimizing conditions, it was found that reasonably precise activation energies could be obtained for the defect levels causing the negative DLTS peaks. A typical low-temperature DLTS curve, with the largest peak of the previous figures resolved into its two component peaks, is shown in figure 2-3. The following four steps were found to be helpful in resolving these component peaks: (1) Since the relative peak heights of the two levels depend on the reverse bias (the 0.29-eV level decreases with increasing bias), a -17,-7,-17 V sequence was used to enhance the contribution from the weaker level; (2) the densities of the levels are not uniform over the wafer, so a location was chosen where the weaker level was as large as possible relative to the stronger level; (3) measurements at low temperatures were emphasized to minimize interference from positive peaks and to enhance resolution of the

* Initial reverse bias of -5 V, trap-charging voltage of 0 V, and -5 V reverse bias during observation of DLTS transient.

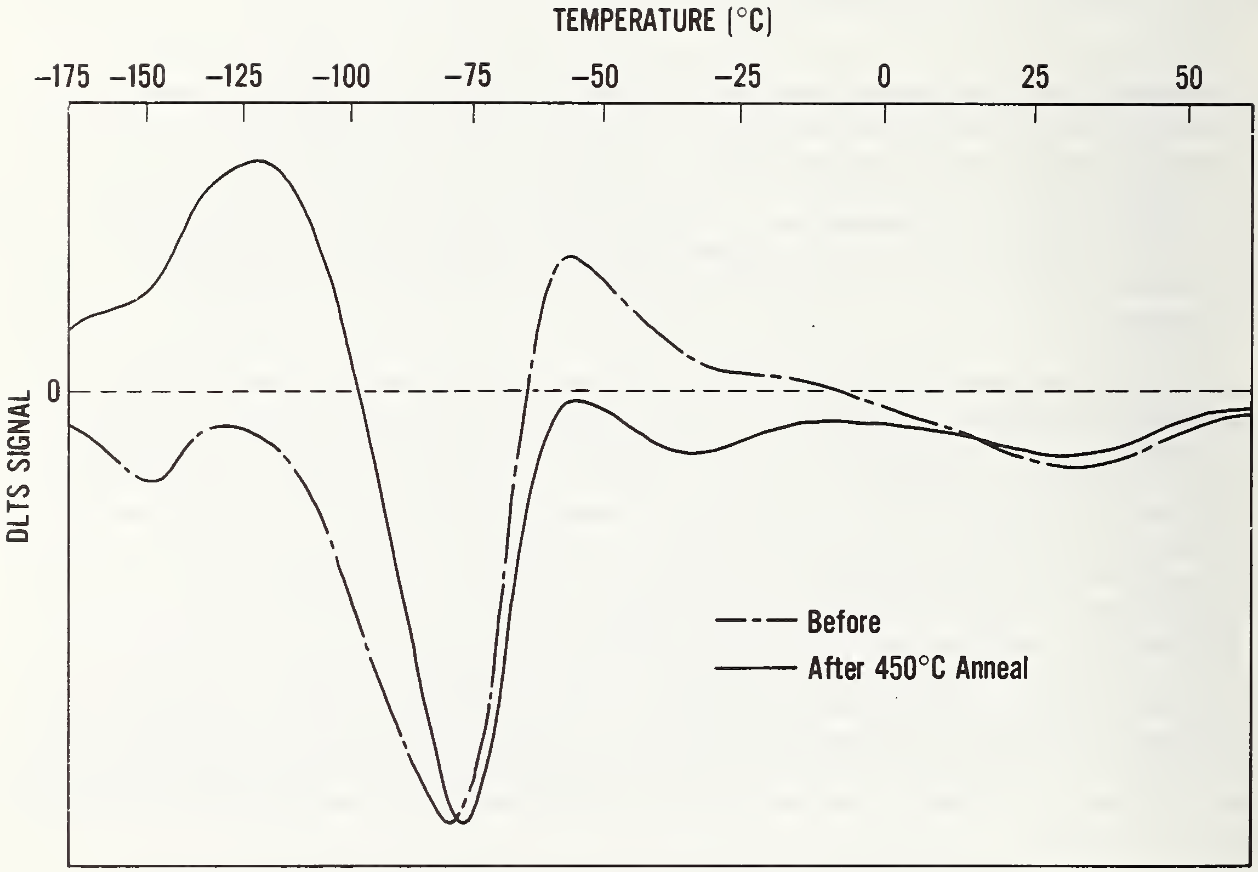

Figure 2-1. DLTS curves of a p^+n power rectifier diode showing the effects of a heat treatment at 450°C for 1 h in nitrogen. The gate delay times were t_1 = 452 µs and t_2 = 903 µs. The bias sequence was -5,0,-5 V.

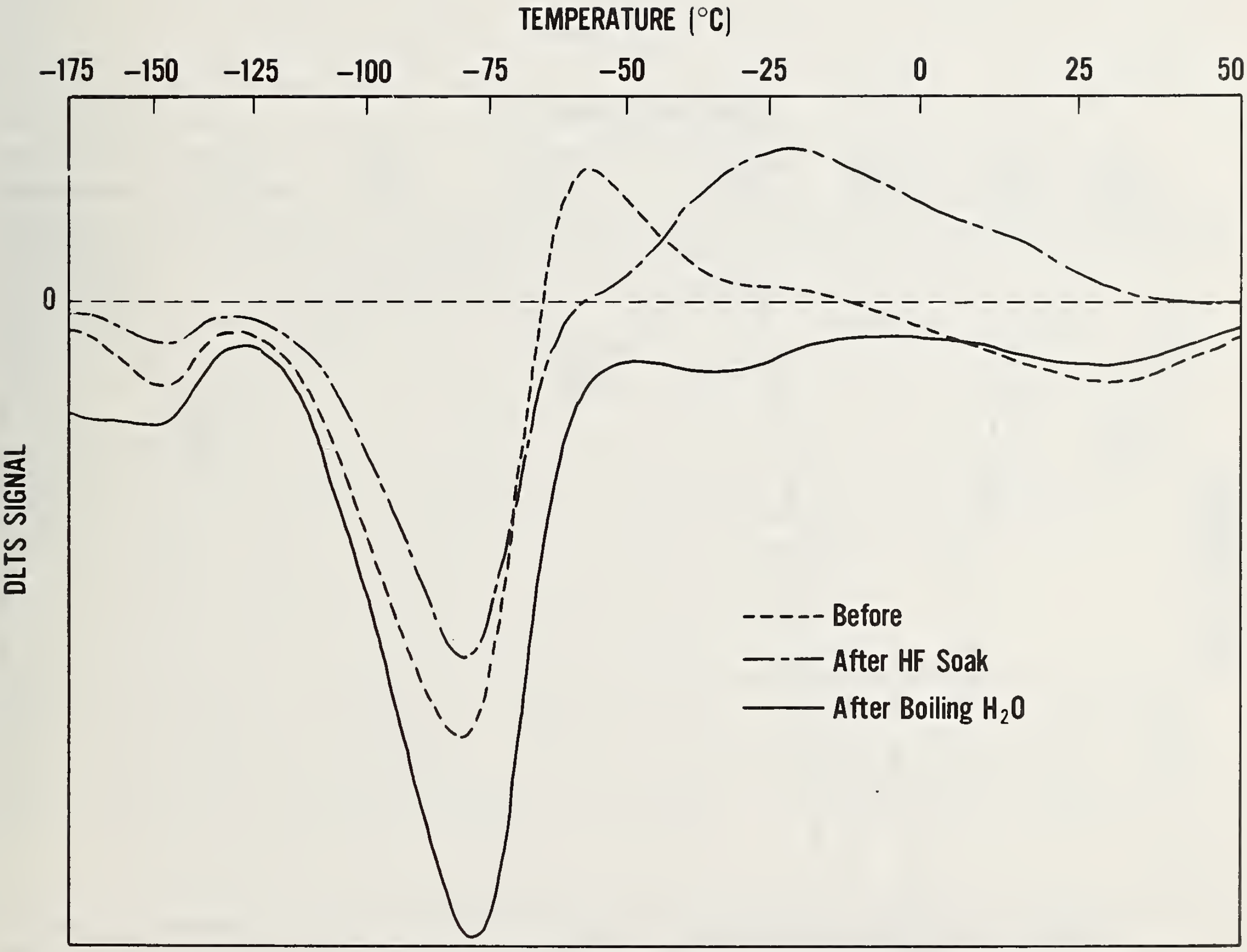

Figure 2-2. DLTS curves of a rectifier diode showing the effects of chemical treatments. Note that the positive peaks disappeared after the diode was boiled in water following the HF soak, which left the surface unprotected. The gate delay times were t_1 = 453 μs and t_2 = 905 μs. The bias sequence was -5,0,-5 V.

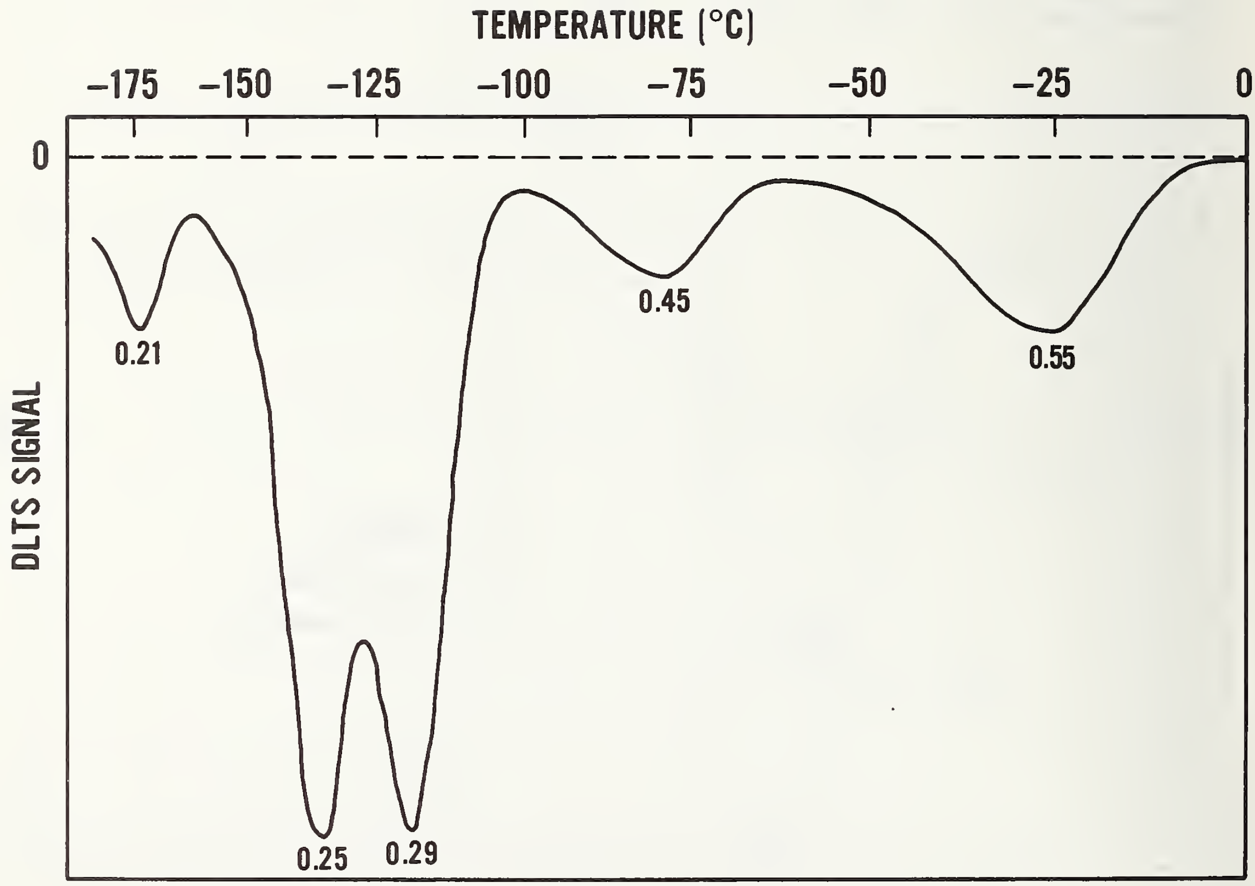

Figure 2-3. DLTS curve of a rectifier diode with experimental conditions optimized to resolve the large negative peak. The activation energy for each level was obtained from an Arrhenius plot of 5 to 10 points. The gate delay times were t_1 = 89.5 ms and t_2 = 191 ms. The bias sequence was -17,-7,-17 V.

two closely spaced peaks; and (4) the ratio of the two DLTS gate delay times was kept small to maximize resolution. A ratio of less than two was not practical because of signal-to-noise considerations.

It is not possible to identify with certainty the physical nature of any of the defects producing the peaks shown in figure 2-3. It is probable that the highest temperature peak with an activation energy of 0.55 eV is the gold acceptor. From the DLTS signal, the estimated density is only 5 to 10 × 10^9 cm^{-3}. Gold is present in most processing environments, and since it was used for metallization on these devices, it is an obvious suspect. In the fabrication of these diodes, a dichromate treatment was used to decrease the surface recombination velocity prior to the oxide growth step. Chromium has been shown [2-3,2-4] to give rise to a level at about E_C - 0.21 eV which matches the shallowest level in figure 2-3. However, this energy value also agrees with that from other possible impurities (i.e., the acceptor level of platinum). Borsuk and Swanson [2-5] made current transient spectroscopy measurements on normally processed (no intentional deep levels) silicon p^+n diodes and found levels at 0.23, 0.28, and 0.53 eV, which are close to those found in this work. They did not comment on the origin of their levels except to note that the gold acceptor was a possibility for the 0.53-eV level.

It is apparent that definite identification of levels with specific defects in an unintentionally doped specimen is extremely difficult without major auxiliary studies, but the electrical characterization can be accomplished by DLTS techniques even in difficult cases such as presented here.

2.3.2 Modeling Lifetime in Terms of DLTS Parameters

Many deep-level states can act as recombination centers by virtue of their ability to capture electrons and holes successively. Traditional deep-level transient-capacitance techniques measure a characteristic time constant for the thermal emission of carriers from deep-level recombination centers under high electric field carrier-depletion conditions and thus do not measure excess-carrier recombination lifetime directly.

However, the capture and emission properties of deep levels are related, because in thermal equilibrium the rates of capture and emission must be equal. Therefore, the traditional approach is to model this dependence [2-6,2-7] and use the resulting analytical relationships to convert the measured emission properties to the corresponding recombination properties (e.g., carrier capture cross section). Since the parameters of this model may vary for nonequilibrium conditions, there is no guarantee that the results of applying this model lead to an adequate characterization of the deep levels with respect to excess-carrier recombination.

One test of adequacy is to model the recombination properties of each deep level by using as input data the measured emission properties for each level. The contributions are summed to calculate the recombination from all such deep levels and thereby to predict the net excess-carrier lifetime. Comparison of the predicted excess-carrier lifetime with values actually measured on the same test devices then serves as a stringent test not only of the model used, but of the adequacy of the original transient-capacitance characterization parameters which were used as input parameters for the model. If the traditional DLTS parameters are found inadequate, it may be necessary to revise the model, reexamine our understanding of the interpretation of DLTS curves, or supplement the traditional DLTS technique with one or more direct measurements of recombination properties (e.g., measurement of the carrier capture cross section by analyzing the time dependence of the amplitude of the capacitance transient as a function of the duration of the trap-filling phase of the DLTS cycle).

The theoretical basis and proposed use of a computer program to predict excess-carrier recombination lifetime from measured deep-level parameters was discussed in last year's annual report [2-2]. The first operating version of this program has been written in FORTRAN IV (see table 2-1) and implements a direct interactive mode where the program prompts the user to enter the input data via the console keyboard and video display and then outputs both the requested input data and computed output data on a line printer. There is sufficient input and output information to fill almost completely one 8-1/2 by 11 inch page for each temperature selected (see table 2-2). The question now being addressed concerns the validity of these predicted results and, by inference, the value of the measured input deep-level characterization results. The program is currently being used to evaluate the existing DLTS specimens to determine which are predicted to have lifetime values that can be measured with existing facilities. Also, the various techniques of measuring lifetime are being reviewed to determine which are expected to measure values under conditions assumed for one or more of the parameters evaluated in the computer model (e.g., should high injection-level lifetime be measured, low injection-level lifetime, or both?). Subsequent comparison of the predicted and measured lifetime on the selected specimens will then serve as the initial test of the adequacy of deep-level techniques for characterizing the excess-carrier recombination properties of deep-level recombination centers.

2.3.3 Current Version of Lifetime-Predicting Computer Program

Deep levels, as carrier traps, facilitate the recombination of electrons and holes and therefore have a profound effect on the excess-carrier lifetime in silicon. Since the effectiveness of these deep levels as recombination centers is a function of a great number of variables, it is impractical to provide general tables listing all possible situations that may be encountered in practice. Therefore, it becomes necessary to calculate the lifetime for each situation and temperature of interest.

The present FORTRAN program was written to accomplish this task for the case of simple donor-like and acceptor-like impurity states in silicon. The density, activation energy, and degeneracy of all active donors and acceptors (i.e., both deep and shallow states) are initially provided as inputs to the program. These parameters for the shallow states can be obtained from Hall or capacitance-voltage measurements and for the deep levels by transient capacitance techniques. These data are then used by the program to calculate the position of the Fermi level by solving the detailed charge balance equation (i.e., the sum of the ionized donors and the positive charges in the valence band equals the sum of the ionized acceptors and the negative charges in the conduction band). After the position of the Fermi level has been found, the program computes some of the more interesting thermal equilibrium

Table 2-1. Listing of FORTRAN Program to Calculate Excess-Carrier Lifetime.

```
C    EXCESS-CARRIER LIFETIME IN SILICON
C
C    PROGRAM CAN HANDLE UP TO 3 DONOR AND 3 ACCEPTOR STATES
C
C
C    INPUT VARIABLE NAMES
C
C    LEVEL       NAME   DENSITY   ENERGY   DEGEN.
C
C    DONOR 1     NAME1  DN1       EN1      DG1
C    DONOR 2     NAME2  DN2       EN2      DG2
C    DONOR 3     NAME3  DN3       EN3      DG3
C    ACCEPTOR 1  NAME4  DN4       EN4      DG4
C    ACCEPTOR 2  NAME5  DN5       EN5      DG5
C    ACCEPTOR 3  NAME6  DN6       EN6      DG6
C
C    DONOR ENERGIES ARE REFERENCED TO CONDUCTION BAND
C    ACCEPTOR ENERGIES ARE REFERENCED TO VALENCE BAND
C
C
C                ELECTRON   HOLE
C    LEVEL       CAPTURE    CAPTURE
C                 CROSS-     CROSS-
C                SECTION    SECTION
C
C    DONOR 1       SE1        SH1
C    DONOR 2       SE2        SH2
C    DONOR 3       SE3        SH3
C    ACCEPTOR 1    SE4        SH4
C    ACCEPTOR 2    SE5        SH5
C    ACCEPTOR 3    SE6        SH6
C
C
C    A MODIFIED MKS SYSTEM OF UNITS IS USED
C       WITH CM REPLACING METERS
C
C    T = THE TEMPERATURE IN KELVIN
C    EG = THE ENERGY GAP OF SILICON IN ELECTRON VOLTS
C    EF = THE FERMI LEVEL IN EV ABOVE THE VALENCE BAND
C    CN = THE CONCENTRATION OF ELECTRONS IN THE CONDUCTION BAND IN CM-3
C    CP = THE CONCENTRATION OF HOLES IN THE VALENCE BAND IN CM-3
C    FNC = THE DENSITY OF STATES IN THE CONDUCTION BAND IN CM-3
C    FNV = THE DENSITY OF STATES IN THE VALENCE BAND IN CM-3
C    DI1 - DI6 = THE DENSITY OF IONIZED SPECIES NAME1 - NAME6 IN CM-3
C    SE1 - SE6 = THE ELECTRON CAPTURE CROSS SECTIONS
C       OF STATES NAME1 - NAME6 IN CM+2
C    SH1 - SH2 = THE HOLE CAPTURE CRSS SECTIONS
C       OF STATES NAME1 - NAME6 IN CM+2
C    TAUNO(I) = HIGH LEVEL ELECTRON LIFETIME PARAMETER OF LEVEL I
C    TAUPO(I) = HIGH LEVEL HOLE LIFETIME PARAMETER OF LEVEL I
C
C
C    SYSTEM CONFIGURATION
C
C    DEVICE NO. 2 = 80 COLUMN PRINTER
C    DEVICE NO. 3 = CRT CONSOLE AND KEYBOARD
C    ALPHANUMERIC STORAGE = 2 ASCII CHAR. PER INTEGER VARIABLE
C
C
```

```
C     REFERENCES
C
C     1. GHANDHI, S. K., SEMICONDUCTOR POWER DEVICES:
C        PHYSICS OF OPERATION AND FABRICATION TECHNOLOGY,
C        PP. 2-31 (JOHN WILEY AND SONS, NEW YORK, 1977)
C
C     2. LARRABEE. R. D., THURBER, W. R., AND BULLIS, W. M.,
C        SEMICONDUCTOR MEASUREMENT TECHNOLOGY: A FORTRAN
C        PROGRAM FOR CALCULATING THE ELECTRICAL PROPERTIES
C        OF EXTRINSIC SILICON, NBS SPECIAL PUBLICATION 400-63,
C        OCTOBER, 1980
C
C     3. LARRABEE. R. D., PHILLIPS. W. E., AND THURBER. W. R.,
C        MEASUREMENT TECHNIQUES FOR HIGH POWER SEMICONDUCTOR
C        MATERIALS AND DEVICES: ANNUAL REPORT, OCTOBER 1, 1979
C        TO SEPTEMBER 30, 1980, PP. 33-37.
C
C
C     MAIN PROGRAM HANDLES INPUT AND OUTPUT
C        AND CALLS THE FOLLOWING SUBROUTINES:
C           SUBROUTINE ZEROIN TO DETERMINE THERMAL EQUILIBRIUM CONDITIONS
C           SUBROUTINE TAU TO EVALUATE LIFETIME RELATED PARAMETERS
C
         EXTERNAL TEST
         DIMENSION NAME1(4),NAME2(4),NAME3(4)
         DIMENSION NAME4(4),NAME5(4),NAME6(4)
         DIMENSION TAUNO(6),TAUPO(6)
         COMMON NAME1,NAME2,NAME3,NAME4,NAME5,NAME6
         COMMON DN1,DN2,DN3,DN4,DN5,DN6
         COMMON DI1,DI2,DI3,DI4,DI5,DI6
         COMMON EN1,EN2,EN3,EN4,EN5,EN6
         COMMON DG1,DG2,DG3,DG4,DG5,DG6
         COMMON T,CN,CP,EG,FNC,FNV,ALPHA,BETA
         COMMON TAUNO,TAUPO
C
C     INPUT THE CHARACTERISTICS OF THE ENERGY LEVELS
C
1        CALL HOME
         WRITE (3,10)
10       FORMAT (1X,'ENTER PARAMETERS IN THE FOLLOWING TABLE')
         WRITE (3,20)
20       FORMAT (1X)
         WRITE (3,30)
30       FORMAT (1X,'    NAME     DENSITY  ENERGY   DEGEN.')
         WRITE (3,20)
         WRITE (3,40)
40       FORMAT (' ','D1  ')
         READ (3,50) NAME1,DN1,EN1,DG1
50       FORMAT (4A2,1X,E9.4,2F9.4)
         WRITE (3,60)
60       FORMAT ('+','D2  ')
         READ (3,70) NAME2,DN2,EN2,DG2
70       FORMAT (4A2,1X,E9.4,2F9.4)
         WRITE (3,80)
80       FORMAT ('+','D3  ')
         READ (3,90) NAME3,DN3,EN3,DG3
90       FORMAT (4A2,1X,E9.4,2F9.4)
         WRITE (3,100)
100      FORMAT ('+','A1  ')
         READ (3,110) NAME4,DN4,EN4,DG4
```

```
110     FORMAT (4A2,1X,E9.4,2F9.4)
        WRITE (3,120)
120     FORMAT ('+','A2  ')
        READ (3,130) NAME5,DN5,EN5,DG5
130     FORMAT (4A2,1X,E9.4,2F9.4)
        WRITE (3,140)
140     FORMAT ('+','A3  ')
        READ (3,150) NAME6,DN6,EN6,DG6
150     FORMAT (4A2,1X,E9.4,2F9.4)
C
C   IF DENSITY OF ANY STATE IS ZERO, RENAME IT TO '$$'
C      TO INDICATE THAT IT IS NOT PRESENT
C
        IF (DN1.EQ.0.) NAME1(1)='$$'
        IF (DN2.EQ.0.) NAME2(1)='$$'
        IF (DN3.EQ.0.) NAME3(1)='$$'
        IF (DN4.EQ.0.) NAME4(1)='$$'
        IF (DN5.EQ.0.) NAME5(1)='$$'
        IF (DN6.EQ.0.) NAME6(1)='$$'
C
        WRITE (3,20)
        WRITE (3,160)
160     FORMAT (1X,'ENTER CROSS SECTIONS IN THIS TABLE')
        WRITE (3,20)
        WRITE (3,170)
170     FORMAT (13X,'CROSS SECTIONS OF LEVELS')
        WRITE (3,180)
180     FORMAT (13X,'ELECTRON  HOLE')
        WRITE (3,20)
        IF (NAME1(1).EQ.'$$') GO TO 210
        WRITE (3,190) NAME1
190     FORMAT (' D1  ',4A2)
        READ (3,200) SE1,SH1
200     FORMAT (2E10.4)
210     IF (NAME2(1).EQ.'$$') GO TO 230
        WRITE (3,220) NAME2
220     FORMAT ('+D2  ',4A2)
        READ (3,200) SE2,SH2
230     IF (NAME3(1).EQ.'$$') GO TO 250
        WRITE (3,240) NAME3
240     FORMAT ('+D3  ',4A2)
        READ (3,200) SE3,SH3
250     IF (NAME4(1).EQ.'$$') GO TO 270
        WRITE (3,260) NAME4
260     FORMAT ('+A1  ',4A2)
        READ (3,200) SE4,SH4
270     IF (NAME5(1).EQ.'$$') GO TO 290
        WRITE (3,280) NAME5
280     FORMAT ('+A2  ',4A2)
        READ (3,200) SE5,SH5
290     IF (NAME6(1).EQ.'$$') GO TO 310
        WRITE (3,300) NAME6
300     FORMAT ('+A3  ',4A2)
        READ (3,200) SE6,SH6
310     WRITE (3,20)
C
C   ENTER TEMPERATURE RANGE OF INTEREST
C      START,END,STEP
C
320     FORMAT (1X,'TEMPERATURE RANGE TABLE')
```

```
      WRITE (3,20)
      WRITE (3,330)
330   FORMAT (1X,'ENTER TEMPERATURE RANGE IN THIS TABLE')
      WRITE (3,20)

      WRITE (3,340)
340   FORMAT (1X,'START      END        STEP')
      WRITE (3,20)
      WRITE (3,20)
      READ (3,350) TSTART,TEND,TSTEP
350   FORMAT (3F10.0)
      IF (TSTEP.EQ.0.) TSTEP = 10.
      IF (TEND.EQ.0.) TEND=TSTART
      NT=INT(ABS((TEND-TSTART)/TSTEP))+1
      DO 1000 N=1,NT
      T=TSTART+(N-1)*TSTEP
C
C   PRELIMINARY COMPUTATIONS
C
C   EFME AND EFMH ARE THE EFFECTIVE MASSES OF ELECTRON AND HOLES
C      FROM BARBER, H. D., SOLID-STATE ELECTRONICS 10, 1039 (1967)
C      FITTED OVER THE TEMPERATURE RANGE FROM 0 TO 600 KELVIN
      EFME=(((((4.54649E-17*T-9.66067E-14)*T+8.04032E-11)*T-3.320130
     2 E-8)*T+6.83008E-6)*T-0.000161708)*T+1.0627
      EFMH=(((((1.11997E-16*T-2.596730E-13)*T+2.30049E-10)*T-9.67212
     2 E-8)*T+1.85678E-5)*T-0.000523548)*T+0.590525
C
C   FNC AND FNV ARE THE DENSITIES OF STATES IN THE BANDS
C   CONST=2*(2*PI*K*(FREE ELECTRON MASS)/H**2)**(3/2)
      CONST=4.829E15
      FNC=CONST*(EFME**1.5)*(T**1.5)
      FNV=CONST*(EFMH**1.5)*(T**1.5)
C
C   EG IS THE BANDGAP OF SILICON AT THE TEMPERATURE T
C      EG FROM FIT OF DATA OF MACFARLANE, PHYS. REV. 111, 1245 (1958)
      EG=(((-3.80977E-13*T+9.95E-10)*T-8.70110E-7)*T+0.0000323741)
     2 *T+1.15556
C
C   SET UP SEARCH FOR FERMI LEVEL
C
      EF=0.
      EFG=1.2
      RE=1.0E-6
      AE=1.0E-6
      IFLAG=0
      WRITE (3,360) T
360   FORMAT (1X,'FINDING FERMI LEVEL AT ',F5.0,' KELVIN')
      CALL ZEROIN (TEST,EF,EFG,RE,AE,IFLAG)
      WRITE (3,20)
      IF (IFLAG.GT.2) GO TO 1010
C
C   PRINT OUT PRESENT RESULTS
C
      WRITE (2,370)
370   FORMAT ('0','  NAME',5X,'DENSITY     ENERGY    DEGEN.
     2 'CAPTURE CROSS SECTIONS')
      WRITE (2,380)
380   FORMAT (1X,39X,' ELECTRON      HOLE')
      WRITE (2,20)
      IF (NAME1(1).EQ.'$$') GO TO 390
```

```
      WRITE (2,450) NAME1,DN1,EN1,DG1,SE1,SH1
390   IF (NAME2(1).EQ.'$$') GO TO 400
      WRITE (2,450) NAME2,DN2,EN2,DG2,SE2,SH2
400   IF (NAME3(1).EQ.'$$') GO TO 410
      WRITE (2,450) NAME3,DN3,EN3,DG3,SE3,SH3
410   IF (NAME4(1).EQ.'$$') GO TO 420
      WRITE (2,450) NAME4,DN4,EN4,DG4,SE4,SH4
420   IF (NAME5(1).EQ.'$$') GO TO 430
      WRITE (2,450) NAME5,DN5,EN5,DG5,SE5,SH5
430   IF (NAME6(1).EQ.'$$') GO TO 460
      WRITE (2,450) NAME6,DN6,EN6,DG6,SE6,SH6
450   FORMAT (1X,4A2,2X,1PE10.3,0PF7.4,3X,0PF5.2,5X,2(1PE10.4,3X))
460   WRITE (2,470)
470   FORMAT ('0')
      WRITE (2,480)
480   FORMAT (1X,'THERMAL EQUILIBRIUM CONDITIONS')
      WRITE (2,20)
      WRITE (2,490)
490   FORMAT (1X,'  TEMP.    1000/T     EF',7X,'EG-EF',3X,
     2 ' CARRIER DENSITIES')
      WRITE (2,500)
500   FORMAT (1X,39X,' ELECTRON     HOLE')
      WRITE (2,20)
      RTEMP=1000./T
      EFV=EG-EF
      WRITE (2,510) T,RTEMP,EF,EFV,CN,CP
510   FORMAT (1X,F8.3,1X,F9.4,2X,F7.4,3X,F7.4,2X,2(1PE10.3,3X))
      WRITE (2,470)
C
C   COMPUTE TAUNO(I) AND TAUPO(I)
C
      DO 520 I=1,6
      TAUNO(I)=1.E30
520   TAUPO(I)=1.E30
C   CONST=(3*K/(FREE ELECTRON MASS))**0.5*(T/(EFFECTIVE MASS))**0.5
      CONST1=6.7421762E5*(T/EFME)**0.5
      CONST2=6.7421762E5*(T/EFMH)**0.5
      X=CONST1*SE1*DN1
      IF (X.EQ.0.) GO TO 530
      TAUNO(1)=1/X
530   X=CONST1*SE2*DN2
      IF (X.EQ.0.) GO TO 540
      TAUNO(2)=1/X
540   X=CONST1*SE3*DN3
      IF (X.EQ.0.) GO TO 550
      TAUNO(3)=1/X
550   X=CONST1*SE4*DN4
      IF (X.EQ.0.) GO TO 560
      TAUNO(4)=1/X
560   X=CONST1*SE5*DN5
      IF (X.EQ.0.) GO TO 570
      TAUNO(5)=1/X
570   X=CONST1*SE6*DN6
      IF (X.EQ.0.) GO TO 580
      TAUNO(6)=1/X
580   X=CONST2*SH1*DN1
      IF (X.EQ.0.) GO TO 590
      TAUPO(1)=1/X
590   X=CONST2*SH2*DN2
      IF (X.EQ.0.) GO TO 600
```

```
      TAUPO(2)=1/X
600   X=CONST2*SH3*DN3
      IF (X.EQ.0.) GO TO 610
      TAUPO(3)=1/X
610   X=CONST2*SH4*DN4
      IF (X.EQ.0.) GO TO 620
      TAUPO(4)=1/X
620   X=CONST2*SH5*DN5
      IF (X.EQ.0.) GO TO 630
      TAUPO(5)=1/X
630   X=CONST2*SH6*DN6
      IF (X.EQ.0.) GO TO 640
      TAUPO(6)=1/X
640   CONTINUE
C
C  CONTINUE PRINT-OUT OF THERMAL EQUILIBRIUM DATA
C
      WRITE (2,650)
650   FORMAT (1X,'  NAME     ION. DEN.  % IONIZED',
     2 '  TAUNO      TAUPO      TAUHIGH')
      WRITE (2,20)
C  HIGH LEVEL LIFETIME IS SUM OF TAUNO AND TAUPO FOR EACH STATE
C  NET HIGH LEVEL LIFETIME IS THE RECIPROCAL OF THE
C     SUM OF RECIPROCALS OF EACH STATE
      SUM=0
      IF (NAME1(1).EQ.'$$') GO TO 660
      X=TAUNO(1)+TAUPO(1)
      SUM=SUM+1/X
      Y=100*DI1/DN1
      WRITE (2,710) NAME1,DI1,Y,TAUNO(1),TAUPO(1),X
660   IF (NAME2(1).EQ.'$$') GO TO 670
      X=TAUNO(2)+TAUPO(2)
      SUM=SUM+1/X
      Y=100*DI2/DN2
      WRITE (2,710) NAME2,DI2,Y,TAUNO(2),TAUPO(2),X
670   IF (NAME3(1).EQ.'$$') GO TO 680
      X=TAUNO(3)+TAUPO(3)
      SUM=SUM+1/X
      Y=100*DI3/DN3
      WRITE (2,710) NAME3,DI3,Y,TAUNO(3),TAUPO(3),X
680   IF (NAME4(1).EQ.'$$') GO TO 690
      X=TAUNO(4)+TAUPO(4)
      SUM=SUM+1/X
      Y=100*DI4/DN4
      WRITE (2,710) NAME4,DI4,Y,TAUNO(4),TAUPO(4),X
690   IF (NAME5(1).EQ.'$$') GO TO 700
      X=TAUNO(5)+TAUPO(5)
      SUM=SUM+1/X
      Y=100*DI5/DN5
      WRITE (2,710) NAME5,DI5,Y,TAUNO(5),TAUPO(5),X
700   IF (NAME6(1).EQ.'$$') GO TO 720
      X=TAUNO(6)+TAUPO(6)
      SUM=SUM+1/X
      Y=100*DI6/DN6
      WRITE (2,710) NAME6,DI6,Y,TAUNO(6),TAUPO(6),X
710   FORMAT (1X,4A2,1X,5(1PE11.3))
720   WRITE (2,470)
      TAUHI=1/SUM
      WRITE (2,730) TAUHI
730   FORMAT (1X,'THE HIGH LEVEL TRAP RECOMBINATION LIFETIME ',
```

```
     2  'IS',1PE10.3,' SECONDS')
        WRITE (2,470)
C
C   EVALUATE LIFETIME UNDER DIFFERENT CONDITIONS
C      AND PRINT-OUT THE RESULTS
C
        CNE=CN
        CPE=CP
        R=CNE
        IF  (CPE.GT.CNE) R=CPE
        R1=0.01*R
        R2=0.1*R
        SUM1=0.
        SUM2=0.
        SUM3=0.
        SUM4=0.
        SUM5=0.
        TAUMAX=1.E30
C
C   TAU1=LIMITING LIFETIME AT ZERO INJECTION LEVEL
C   TAU2=LIFETIME AT INJECTION LEVEL OF 0.01
C   TAU3=LIFETIME AT INJECTION LEVEL OF 0.10
C   TAU4=LIFETIME AT INJECTION LEVEL OF 1.00
C   TAU5=LIFETIME IN A DEPLETION LAYER
C
        WRITE (2,740)
740     FORMAT (1X,'LIFETIME RELATED PARAMETERS')
        WRITE (2,20)
        WRITE (2,750)
750     FORMAT (1X,'  NAME     LOW LEVEL  I.R.=0.01   ',
     2  'I.R.=0.10  I.R.=1.00  DEPLETION LAYER')
        WRITE (2,20)
C
C   CONSIDER EACH BANDGAP STATE SEPARATELY
C
        IF (NAME1(1).EQ.'$$') GO TO 760
        IF (TAUNO(1).GE.TAUMAX) GO TO 760
        IF (TAUPO(1).GE.TAUMAX) GO TO 760
        CALL TAU(1,CNE,CPE,EN1,0.,TAU1)
        CALL TAU(1,CNE,CPE,EN1,R1,TAU2)
        CALL TAU(1,CNE,CPE,EN1,R2,TAU3)
        CALL TAU(1,CNE,CPE,EN1,R,TAU4)
        CALL TAU(1,0.,0.,EN1,0.,TAU5)
        SUM1=SUM1+1/TAU1
        SUM2=SUM2+1/TAU2
        SUM3=SUM3+1/TAU3
        SUM4=SUM4+1/TAU4
        SUM5=SUM5+1/TAU5
        WRITE (2,810) NAME1,TAU1,TAU2,TAU3,TAU4,TAU5
C
760     IF (NAME2(1).EQ.'$$') GO TO 770
        IF (TAUNO(2).GE.TAUMAX) GO TO 770
        IF (TAUPO(2).GE.TAUMAX) GO TO 770
        CALL TAU(2,CNE,CPE,EN2,0.,TAU1)
        CALL TAU(2,CNE,CPE,EN2,R1,TAU2)
        CALL TAU(2,CNE,CPE,EN2,R2,TAU3)
        CALL TAU(2,CNE,CPE,EN2,R,TAU4)
        CALL TAU(2,0.,0.,EN2,0.,TAU5)
        SUM1=SUM1+1/TAU1
        SUM2=SUM2+1/TAU2
```

```
      SUM3=SUM3+1/TAU3
      SUM4=SUM4+1/TAU4
      SUM5=SUM5+1/TAU5
      WRITE (2,810) NAME2,TAU1,TAU2,TAU3,TAU4,TAU5
C
770   IF (NAME3(1).EQ.'$$') GO TO 780
      IF (TAUNO(3).GE.TAUMAX) GO TO 780
      IF (TAUPO(3).GE.TAUMAX) GO TO 780
      CALL TAU(3,CNE,CPE,EN3,0.,TAU1)
      CALL TAU(3,CNE,CPE,EN3,R1,TAU2)
      CALL TAU(3,CNE,CPE,EN3,R2,TAU3)
      CALL TAU(3,CNE,CPE,EN3,R,TAU4)
      CALL TAU(3,0.,0.,EN3,0.,TAU5)
      SUM1=SUM1+1/TAU1
      SUM2=SUM2+1/TAU2
      SUM3=SUM3+1/TAU3
      SUM4=SUM4+1/TAU4
      SUM5=SUM5+1/TAU5
      WRITE (2,810) NAME3,TAU1,TAU2,TAU3,TAU4,TAU5
C
780   IF (NAME4(1).EQ.'$$') GO TO 790
      IF (TAUNO(4).GE.TAUMAX) GO TO 790
      IF (TAUPO(4).GE.TAUMAX) GO TO 790
      CALL TAU(4,CNE,CPE,EN4,0.,TAU1)
      CALL TAU(4,CNE,CPE,EN4,R1,TAU2)
      CALL TAU(4,CNE,CPE,EN4,R2,TAU3)
      CALL TAU(4,CNE,CPE,EN4,R,TAU4)
      CALL TAU(4,0.,0.,EN4,0.,TAU5)
      SUM1=SUM1+1/TAU1
      SUM2=SUM2+1/TAU2
      SUM3=SUM3+1/TAU3
      SUM4=SUM4+1/TAU4
      SUM5=SUM5+1/TAU5
      WRITE (2,810) NAME4,TAU1,TAU2,TAU3,TAU4,TAU5
C
790   IF (NAME5(1).EQ.'$$') GO TO 800
      IF (TAUNO(5).GE.TAUMAX) GO TO 800
      IF (TAUPO(5).GE.TAUMAX) GO TO 800
      CALL TAU(5,CNE,CPE,EN5,0.,TAU1)
      CALL TAU(5,CNE,CPE,EN5,R1,TAU2)
      CALL TAU(5,CNE,CPE,EN5,R2,TAU3)
      CALL TAU(5,CNE,CPE,EN5,R,TAU4)
      CALL TAU(5,0.,0.,EN5,0.,TAU5)
      SUM1=SUM1+1/TAU1
      SUM2=SUM2+1/TAU2
      SUM3=SUM3+1/TAU3
      SUM4=SUM4+1/TAU4
      SUM5=SUM5+1/TAU5
      WRITE (2,810) NAME5,TAU1,TAU2,TAU3,TAU4,TAU5
C
800   IF (NAME6(1).EQ.'$$') GO TO 820
      IF (TAUNO(6).GE.TAUMAX) GO TO 820
      IF (TAUPO(6).GE.TAUMAX) GO TO 820
      CALL TAU(6,CNE,CPE,EN6,0.,TAU1)
      CALL TAU(6,CNE,CPE,EN6,R1,TAU2)
      CALL TAU(6,CNE,CPE,EN6,R2,TAU3)
      CALL TAU(6,CNE,CPE,EN6,R,TAU4)
      CALL TAU(6,0.,0.,EN6,0.,TAU5)
      SUM1=SUM1+1/TAU1
      SUM2=SUM2+1/TAU2
```

```
      SUM3=SUM3+1/TAU3
      SUM4=SUM4+1/TAU4
      SUM5=SUM5+1/TAU5
      WRITE (2,810) NAME6,TAU1,TAU2,TAU3,TAU4,TAU5
C
810   FORMAT (1X,4A2,1X,5(1PE11.3))
820   WRITE (2,470)
      TAU1=1/SUM1
      TAU2=1/SUM2
      TAU3=1/SUM3
      TAU4=1/SUM4
      TAU5=1/SUM5
      WRITE (2,830) TAU1
830   FORMAT (1X,'LOW LEVEL LIFETIME IS ',1PE10.3,
     2 ' SECONDS')
      WRITE (2,20)
      WRITE (2,840) TAU2
840   FORMAT (1X,'LIFETIME AT 0.01 I.R. IS ',1PE10.3,
     2 ' SECONDS')
      WRITE (2,20)
      WRITE (2,850) TAU3
850   FORMAT (1X,'LIFETIME AT 0.10 I.R. IS '1PE10.3,
     2 ' SECONDS')
      WRITE (2,20)
      WRITE (2,860) TAU4
860   FORMAT (1X,'LIFETIME AT 1.00 I.R. IS ',1PE10.3,
     2 ' SECONDS')
      WRITE (2,20)
      WRITE (2,870) TAU5
870   FORMAT (1X,'LIFETIME IN A DEPLELTION LAYER IS ',
     2 1PE10.3,' SECONDS')
      WRITE (2,880)
880   FORMAT ('1')
1000  CONTINUE
      GO TO 1
1010  WRITE (3,1020) IFLAG
1020  FORMAT (1X,'ERROR FLAG = ',F3.0)
      PAUSE
      GO TO 1
      END
```

```
      SUBROUTINE TAU(I,CNE,CPE,EN,DN,TAUX)
C
C   SUBROUTINE TO COMPUTE SPACE-CHARGE NEUTRAL LIFETIMES
C
C   DESCRIPTION OF ARGUMENTS:
C      I      - INDEX RANGING FROM 1 TO 6 SPECIFYING THE ENERGY LEVEL
C      CNE    - THERMAL EQUILIBRIUM DENSITY OF ELECTRONS
C      CPE    - THERMAL EQUILIBRIUM DENSITY OF HOLES
C      EN     - POSITION OF THE FERMI LEVEL
C      DN     - DENSITY OF EXCESS ELECTRON-HOLE PAIRS
C      TAUX   - COMPUTED VALUE OF THE LIFETIME
C
      DIMENSION NAME1(4),NAME2(4),NAME3(4)
      DIMENSION NAME4(4),NAME5(4),NAME6(4)
      DIMENSION TAUNO(6),TAUPO(6)
      COMMON NAME1,NAME2,NAME3,NAME4,NAME5,NAME6
      COMMON DN1,DN2,DN3,DN4,DN5,DN6
      COMMON DI1,DI2,DI3,DI4,DI5,DI6
      COMMON EN1,EN2,EN3,EN4,EN5,EN6
      COMMON DG1,DG2,DG3,DG4,DG5,DG6
      COMMON T,CN,CP,EG,FNC,FNV,ALPHA,BETA
      COMMON TAUNO,TAUPO
C
C   COMPUTE "FICTITIOUS" CARRIER DENSITIES WITH EF AT TRAP LEVEL
C
      EF=EN
      IF (I.LE.3) EF=EG-EN
      X=TEST(EF)
C
C   EVALUATE LIFETIME EXPRESSION
C
      DENOM=CNE+CPE+DN
      IF (DENOM.EQ.0.) GO TO 10
      X=TAUNO(I)*(CPE+CP+DN)/DENOM
      TAUX=X+TAUPO(I)*(CNE+CN+DN)/DENOM
      RETURN
C
10    X=TAUNO(I)*CP+TAUPO(I)*CN
      Y=FNC*FNV*EXP(-EG/(8.6173E-5*T))
      TAUX=X/(2*Y**0.5)
      RETURN
C
      END
```

```
C    SUBROUTINE ZEROIN(F,B,C,RE,AE,IFLAG)
C
C    SANDIA MATHEMATICAL PROGRAM LIBRARY
C    MATHEMATICAL COMPUTING SERVICES DIVISION 5422
C    SANDIA LABORATORIES
C    P.O. BOX 5800
C    ALBUQUERQUE, NEW MEXICO 87115
C
C    CONTROL DATA 6600 VERSION 4.5, 1 NOVEMBER 1971
C
C    MODIFIED BY D. KAHANER, NBS DIVISION 713.
C
C    ABSTRACT:
C       ZEROIN SEARCHES FOR A ZERO OF A FUNCTION F(X) BETWEEN
C       THE GIVEN VALUES B AND C UNTIL THE WIDTH OF INTERVAL
C       (B,C) HAS COLLAPSED TO WITHIN A TOLERANCE SPECIFIED BY
C       THE STOPPING CRITERION, ABS(B-C).LE.2.*(RW*ABS(B)+AE).
C
C    DESCRIPTION OF ARGUMENTS:
C       F      - NAME OF THE REAL VALUED EXTERNAL FUNCTION.
C                THIS NAME MUST BE IN AN EXTERNAL STATEMENT
C                IN THE CALLING PROGRAM.
C                F MUST BE A FUNCTION OF ONE REAL ARGUMENT.
C       B      - ONE END OF THE INTERVAL (B,C).
C                THE VALUE RETURNED FOR B USUALLY IS THE
C                BETTER APPROXIMATION OF F.
C       C      - THE OTHER END OF THE INTERVAL (B.C).
C       RE     - THE RELATIVE ERROR USED FOR RW
C                IN THE STOPPING CRITERION.
C                IF THE REQUESTED RE IS LESS THAN THE MACHINE
C                PRECISION, THEN RW IS SET TO APPROXIMATELY
C                THE MACHINE PRECISION.
C       AE     - THE ABSOLUTE ERROR USED IN THE STOPPING
C                CRITERION.  IF THE GIVEN INTERVAL (B,C)
C                CONTAINS THE ORIGIN, THEN A NONZERO VALUE
C                SHOULD BE CHOSEN FOR AE.
C       IFLAG  - RETURNS A STATUS OF THE RESULTS INDICATING
C                WHICH OF THE FOLLOWING CONDITIONS HOLD:
C
C                    A - ABS(B-C).LE.2.*(RW*ABS(B)+AE).
C                    B - F(B)*F(C).LT.0.
C                    C - ABS(F(B)).LE.ABS(F(C)).
C                    D - ABS(F(B"OUT")).LE.
C                        MAX(ABS(F(B"IN")),ABS(F(C"IN"))).
C                    E - NUMBER OF EVALUATIONS OF F(X),LE.500.
C
C                 IFLAG=1 INDICATES NORMAL CASE
C                         ALL CONDITIONS ABOVE HOLD.
C                 IFLAG=2 INDICATES F(B)=0.
C                         CONDITION A MAY NOT HOLD.
C                 IFLAG=3 INDICATES CONDITIONS A, B, C, AND E
C                         HOLD, BUT CONDITION D DOES NOT.
C                         THE INTERVAL (B,C) PROBABLY CONTAINS
C                         A SINGLULAR POINT OF THE FUNCTION F.
C                 IFLAG=4 INDICATES CONDITIONS A AND E HOLD,
C                         BUT CONDITION B DOES NOT.
C                         A LOCAL MINIMUM OF F(X) IN (B,C)
C                         MAY HAVE BEEN FOUND.
C                 IFLAG=5 INDICATES SEARCH WAS ABORTED
```

```
C                              WHEN CONDITION E FAILED.
C
C     REFERENCES:
C        1.    L. F. SHAMPINE AND H. A. WATTS. ZEROIN,
C              A ROOT-SOLVING CODE, SC-TM-70-631, SEPT., 1970.
C        2.    T. J. DEKKER. FINDING A ZERO BY MEANS
C              OF SUCCESSIVE LINEAR INTERPOLATION,
C              *CONSTRUCTIVE ASPECTS OF THE FUNDAMENTAL THEORM
C              OF ALGEBRA*, EDITED BY D. DEJON AND P. HENRICI,
C              1969.
C        3.    L. F. SHAMPINE AND R. C. ALLEN, NUMERICAL
C              COMPUTING -- AN INTRODUCTION.
C
C     SEE NBS SPECIAL PUBLICATION 400-63, PP. 28-30
C
      SUBROUTINE ZEROIN(F,B,C,RE,AE,IFLAG)
C     INITIALIZE FOR MICROSOFT FORTRAN-80 ON Z-80 APPLE II
      DATA ER/6.0E-8/
C     INITIALIZE IN PORTABLE MANNER
C     DATA ER/0.0/
C     IF (ER.EQ.0.) ER=4.*(R1MACH(4))
C
      RW=AMAX1(RE,ER)
      IC=0
      ACBS=ABS(B-C)
      A=C
      FA=F(A)
      FB=F(B)
      FC=FA
      KOUNT=2
      FX=AMAX1(ABS(FB),ABS(FC))
C
1     IF (ABS(FC).GE.ABS(FB)) GO TO 2
C     PERFORM INTERCHANGE
      A=B
      FA=FB
      B=C
      FB=FC
      C=A
      FC=FA
C
2     CMB=0.5*(C-B)
      ACMB=ABS(CMB)
      TOL=RW*ABS(B)+AE
C
C     TEST STOPPING CRITERION
      IF(ACMB.LE.TOL) GO TO 10
C
C     CALCULATE NEW ITERATE IMPLICITLY AS B+P/Q
C     WHERE  P.GE.0. HAS BEEN GUARANTEED.
C     THE IMPLICIT FORM IS USED TO PREVENT OVERFLOW.
      P=(B-A)*FB
      Q=FA-FB
      IF (P.GE.0.) GO TO 3
      P=-P
      Q=-Q
C
C     UPDATE A AND CHECK FOR SATISFACTORY REDUCTION
C        IN THE SIZE OF OUR BOUNDING INTERVAL.
3     A=B
```

```
      FA=FB
      IC=IC+1
      IF (IC.LT.4) GO TO 4
      IF (8.*ACMB.GE.ACBS) GO TO 6
      IC=0
      ACBS=ACMB
C
C   TEST FOR TOO SMALL A CHANGE
4     IF (P.GT.ABS(Q)*TOL) GO TO 5
C
C   INCREMENT BY TOLERANCE
      B=B+SIGN(TOL,CMB)
      GO TO 7
C
C   ROOT OUGHT TO BE BETWEEN B AND (C+B)/2.
5     IF (P.GE.CMB*Q) GO TO 6
C
C   INTERPOLATE
      B=B+P/Q
      GO TO 7
C
C   BISECT THE INTERVAL
6     B=0.5*(C+B)
C
C   COMPUTATION FOR NEW ITERATE B HAS BEEN COMPLETED.
7     FB=F(B)
      IF (FB.EQ.0.) GO TO 11
      KOUNT=KOUNT+1
      IF (KOUNT.GT.500) GO TO 15
C
C   DECIDE IF NEXT STEP IS INTERPOLATION OR EXTRAPOLATION
      IF (SIGN(1.0,FB).NE.SIGN(1.0,FC)) GO TO 1
      C=A
      FC=FA
      GO TO 1
C
C
C   FINISHED.  PROCESS RESULTS FOR PROPER SETTING OF IFLAG.
C
10    IF (FB*FC.GT.0.) GO TO 13
      IF (ABS(FB).GT.FX) GO TO 12
      IFLAG=1
      RETURN
11    IFLAG=2
      RETURN
12    IFLAG=3
      RETURN
13    IFLAG=4
      RETURN
15    IFLAG=5
      RETURN
      END
```

```
C    FUNCTION TEST(EF)
C    THIS EXTERNAL FUNCTION DEFINES THE PARAMETER 'TEST'.
C    SUBROUTINE ZEROIN LOCATES THE VALUE WHICH MINIMIZES 'TEST'.
C
        FUNCTION TEST(EF)
        DIMENSION NAME1(4),NAME2(4),NAME3(4)
        DIMENSION NAME4(4),NAME5(4),NAME6(4)
        COMMON NAME1,NAME2,NAME3,NAME4,NAME5,NAME6
        COMMON DN1,DN2,DN3,DN4,DN5,DN6
        COMMON DI1,DI2,DI3,DI4,DI5,DI6
        COMMON EN1,EN2,EN3,EN4,EN5,EN6
        COMMON DG1,DG2,DG3,DG4,DG5,DG6
        COMMON T,CN,CP,EG,FNC,FNV,ALPHA,BETA
C
C    LEVELS NOT PRESENT HAVE FIRST TWO CHAR. OF NAME = '$$'
C
        CAYT=8.6173E-5*T
C
C    COMPUTATION OF CN
        CN=0.
        ALPHA=(EF-EG)/CAYT
        IF (ALPHA.GT.1.) GO TO 10
        IF (ALPHA.LE.-80.) GO TO 20
C    THE FOLLOWING EQUATION IS USED FOR ALPHA BETWEEN -80 AND +1
        CN=FNC/((EXP(-ALPHA))+0.27)
        GO TO 20
C    THE FOLLOWING EQUATION IS USED FOR ALPHA GREATER THAN +1
10      CN=FNC*0.752253*((ALPHA*ALPHA+1.7)**0.75)
C
C    COMPUTATION OF CP
20      CP=0.
        BETA=-EF/CAYT
        IF (BETA.GT.1.) GO TO 30
        IF (BETA.LE.-80.) GO TO 40
C    THE FOLLOWING EQUATION IS USED FOR BETA BETWEEN -80 AND +1
        CP=FNV/((EXP(-BETA))+0.27)
        GO TO 40
C    THE FOLLOWING EQUATION IS USED FOR BETA GREATER THAN +1
30      CP=FNV*0.752253*((BETA*BETA+1.7)**0.75)
C
C    COMPUTATION OF DI1
40      DI1=0.
        IF (NAME1(1).EQ.'$$') GO TO 60
        POWER=(EF-EG+EN1)/CAYT
        IF (POWER.GE.80.) GO TO 60
        IF (POWER.LE.-80.) GO TO 50
        DI1=DN1/(1.+(EXP(POWER)*DG1))
        GO TO 60
50      DI1=DN1
C
C    COMPUTATION OF DI2
60      DI2=0.
        IF (NAME2(1).EQ.'$$') GO TO 80
        POWER=(EF-EG+EN2)/CAYT
        IF (POWER.GE.80.) GO TO 80
        IF (POWER.LE.-80.) GO TO 70
        DI2=DN2/(1.+(EXP(POWER)*DG2))
        GO TO 80
70      DI2=DN2
```

```
C
C   COMPUTATION OF DI3
80       DI3=0.
         IF (NAME3(1).EQ.'$$') GO TO 100
         POWER=(EF-EG+EN3)/CAYT
         IF (POWER.GE.80.) GO TO 100
         IF (POWER.LE.-80.) GO TO 90
         DI3=DN3/(1.+(EXP(POWER)*DG3))
         GO TO 100
90       DI3=DN3
C
C   COMPUTATION OF DI4
100      DI4=0.
         IF (NAME4(1).EQ.'$$') GO TO 120
         POWER=(EN4-EF)/CAYT
         IF (POWER.GT.80.) GO TO 120
         IF (POWER.LE.-80.) GO TO 110
         DI4=DN4/(1.+(EXP(POWER)*DG4))
         GO TO 120
110      DI4=DN4
C
C   COMPUTATION OF DI5
120      DI5=0.
         IF (NAME5(1).EQ.'$$') GO TO 140
         POWER=(EN5-EF)/CAYT
         IF (POWER.GE.80.) GO TO 140
         IF (POWER.LE.-80.) GO TO 130
         DI5=DN5/(1.+(EXP(POWER)*DG5))
         GO TO 140
130      DI5=DN5
C
C   COMPUTATION OF DI6
140      DI6=0.
         IF (NAME6(1).EQ.'$$') GO TO 160
         POWER=(EN6-EF)/CAYT
         IF (POWER.GT.80.) GO TO 160
         IF (POWER.LE.-80.) GO TO 150
         DI6=DN6/(1.+(EXP(POWER)*DG6))
         GO TO 160
150      DI6=DN6
C
C   TESTING TO SEE HOW CLOSE TO NEUTRALITY WE HAVE COME
C   THE PARAMETER TEST IS THE NET DENSITY OF RESIDUAL CHARGES
C      WHEN THE FERMI LEVEL IS AT ITS PRESENT LOCATION
160      TEST=(CN+DI4+DI5+DI6)-(CP+DI1+DI2+DI3)
         RETURN
         END
```

Table 2-2. Typical Output Listing from Lifetime program of Table 2-1.

NAME	DENSITY	ENERGY	DEGEN.	CAPTURE CROSS SECTIONS ELECTRON	HOLE
PHOS.	1.200E+15	.0450	2.00	1.0000E-16	1.0000E-22
PT ACC.	1.200E+14	.9000	4.00	7.0000E-15	1.0000E-14

THERMAL EQUILIBRIUM CONDITIONS

TEMP.	1000/T	EF	EG-EF	CARRIER DENSITIES ELECTRON	HOLE
300.000	3.3333	.8470	.2638	1.196E+15	1.074E+05

NAME	ION. DEN.	% IONIZED	TAUNO	TAUPO	TAUHIGH
PHOS.	1.199E+15	9.996E+01	7.759E-07	6.411E-01	6.411E-01
PT ACC.	3.740E+12	3.116E+00	1.108E-07	6.411E-08	1.749E-07

THE HIGH LEVEL TRAP RECOMBINATION LIFETIME IS 1.749E-07 SECONDS

LIFETIME RELATED PARAMETERS

NAME	LOW LEVEL	I.R.=0.01	I.R.=0.10	I.R.=1.00	DEPLETION LAYER
PHOS.	2.896E+03	2.868E+03	2.633E+03	1.448E+03	1.527E+08
PT ACC.	5.624E-07	5.585E-07	5.272E-07	3.687E-07	2.628E-02

LOW LEVEL LIFETIME IS 5.624E-07 SECONDS

LIFETIME AT 0.01 I.R. IS 5.585E-07 SECONDS

LIFETIME AT 0.10 I.R. IS 5.272E-07 SECONDS

LIFETIME AT 1.00 I.R. IS 3.687E-07 SECONDS

LIFETIME IN A DEPLELTION LAYER IS 2.628E-02 SECONDS properties of the silicon insofar as lifetime-related questions are concerned. The program requires that the capture cross sections of the levels for electrons and holes also be provided as input data. The program then uses these cross-section values and the results of the thermal equilibrium computations to compute a variety of lifetime-related parameters. Finally, the values of all of the input parameters and of the computed parameters are provided on the printed output listing (see table 2-2).

The present version of this program will accommodate up to six shallow or deep levels in the bandgap of silicon. Three of these levels are assumed to be donors, to be neutral when occupied by an electron, and to have a temperature-independent activation energy referenced to the conduction band edge. The remaining three levels are assumed to be acceptors, to be neutral when occupied by a hole, and to have a temperature-independent activation energy referenced to the valence band edge. These assumptions are appropriate for the shallow dopant impurities from columns 3 and 5 of the periodic table (e.g., boron and phosphorus) and may, or may not, be appropriate for other impurities with larger activation energies or multiple ionization states.

The key algorithms in this program are the routines for calculating the position of the Fermi level and the routine for evaluating lifetime-related parameters. These two algorithms have been written in subroutine format so that they can be used as a starting point in the development of other programs that require these algorithms. Notice, however, that the subroutine for computing excess-carrier lifetime requires knowledge of the parameters calculated by the Fermi level routine, and thus it cannot be used without first executing the Fermi level routine.

The Fermi level routine comprises two subroutines called TEST and ZEROIN and is based on solving the charge balance equation. Subroutine TEST computes the density of electrons in the conduction band, the density of holes in the valence band, and the density of charge on each bandgap state for any given position of the Fermi level. Subroutine ZEROIN is a root-finding routine that determines that particular position of the Fermi level that gives a net zero total charge as determined by subroutine TEST. These subroutines have been fully documented in an NBS Special Publication [2-8].

Subroutine TAU is a routine for evaluating several lifetime-related parameters for a selected state in the bandgap. It requires knowledge of the thermal equilibrium situation as evaluated in advance by the Fermi level routine. The algorithm of subroutine TAU is basically an evaluation of the Shockley-Read-Hall recombination mechanism following the development summarized in last year's annual report [2-2]. The net effective lifetime representing the effect of all the states in the bandgap (assumed to be all acting independently) is computed as the reciprocal of the sum of the reciprocals of the lifetimes of each separate state.

All of these routines have been written in FORTRAN IV and are listed in table 2-1. The program prompts the user for input data on the console video display (output device 3) and accepts this input from the console keyboard (input device 3) and then documents these input data along with the computer lifetime information on the line printer (output device 2). The program listing is complete except for subroutine HOME which is a routine for clearing the console CRT and returning the cursor to its "home" position in the upper left-hand corner of the screen. If this program is to be implemented on a system that does not supply this routine, simply omit the call to this routine and the program will function satisfactorily, but it will not clear the screen at the start of each new run when input data are being requested. The program listing is copiously documented with comments to guide the user through the details of the program. Since the program is still under development and is being modified as experience is gained through its use, it will not be further documented at this time.

A typical output listing is shown in table 2-2. The uppermost section of this listing documents the characterization parameters which were supplied to the program by the user. The next section labeled "THERMAL EQUILIBRIUM CONDITIONS" lists a number of parameters computed under the assumption of thermal equilibrium conditions at the temperature indicated. This includes: the position of the Fermi level relative to the valence band (EF); the position of the Fermi level relative to the conduction band (EG-EF); the thermal equilibrium values of the electron and hole concentrations; the actual density of each bandgap state that is ionized (ION. DEN.); the percentage ionization of each bandgap state (% IONIZED); the computed values of τ_{N_O} and τ_{P_O} which are the reciprocals of the product of the capture cross section, and density of each bandgap state, and the thermal velocity [2-2]; and the sum of τ_{N_O} and τ_{P_O} which is the high injection level lifetime [2-9]. The reciprocal of the sum of the reciprocals of these values of TAUHIGH for each bandgap state is the effective high injection level lifetime in this material and is listed next. The final section of this output listing labeled "LIFETIME RELATED PARAMETERS" gives the computed lifetimes for each state in the bandgap considered independently for the case of low level injection levels, and for injection levels corresponding to 0.01, 0.10, and 1.00 times the minority carrier thermal equilibrium density. The lifetime of an electron-hole pair in a depletion layer [2-9] is given in the last column of this table. Finally, values for all of these quantities are given for the combination of all states in the bandgap by taking the reciprocal of the sum of the reciprocals of the values for each of the states considered independently. A complete page of data of this type is generated for each temperature and for each set of input characterization parameters specified by the user.

This program has been implemented on a 48K Apple computer equipped with a Microsoft Z-80 Softcard and F-80 FORTRAN.* The floating-point real variables were 32 bits long with 8 bits of characteristic and 24 bits of mantissa, leading to a precision of about 7 decimal digits. The time to compute and list the information in table 2-2 was about 20 s. Thus, it is very practical to have a program of this sort running on a relatively inexpensive computer placed right on the laboratory bench where deep-level and lifetime measurements are being performed and to do the comparison between measured and predicted lifetime in real time, thus facilitating better interaction

* Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the materials or equipment identified are necessarily the best available for the purposes.

between the development of the computer model and the experimental measurements.

2.3.4 Conclusions and Recommendations

It has been shown that the positive peaks in the DLTS curves of the power rectifier diodes are due to surface traps. The largest negative peak was shown to be composed of contributions from two levels whose relative densities depended on depth below the junction. The activation energy of each negative level was determined from an Arrhenius plot, and possible origins of the levels were discussed. The density of each level can be determined from the amplitude of its DLTS transient. Before proceeding with lifetime correlations, a more thorough search for levels in the lower half of the bandgap should be made, because with five electron traps in the upper half it is unlikely that the lower half is vacant. Finally, it will be necessary to measure the electron and the hole capture cross section of all the states as a function of temperature. These data can then be input to the lifetime prediction program and the predictions compared to experimentally measured lifetime values.

A FORTRAN computer program has been written that uses measured bandgap state characterization parameters as its input and predicts a number of lifetime-related parameters. The next step is to determine how good these predictions are when compared to experiment. Are the techniques of measuring the properties of the bandgap states adequate for this purpose? Does the program take into account all significant interactions and variations? Has the measurement of the lifetime-related parameters been done in an accurate and meaningful way for the intended purpose? These are the issues that need to be addressed before it can be concluded that the program is producing meaningful results and that the characterizing parameters used as its input are adequately measured. It is anticipated that a successful demonstration of this kind will help to confirm the quality of understanding about deep levels and help promote more widespread use of deep-level characterization techniques in areas outside the research laboratory.

REFERENCES

2-1. Larrabee, R. D., Phillips, W. E., and Thurber, W. R., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1979 to September 30, 1980, NBSIR 81-2325 (September 1981), pp. 28-32.

2-2. Larrabee, R. D., Phillips, W. E., and Thurber, W. R., Reference [2-1], pp. 32-36.

2-3. Graff, K., and Pieper, H., The Behavior of Transition and Noble Metals in Silicon, *Semiconductor Silicon 1981*, Proceedings Volume 81-5, H. R. Huff, R. J. Kriegler, and Y. Takeishi, Eds., pp. 331-343 (Electrochemical Society, Princeton, N. J., 1981).

2-4. Kunio, T., Jr., Nishino, T., Ohta, E., and Sakata, M., Energy Levels and Degeneracy Ratios for Chromium in Silicon, *Solid-State Electron.* 24, 1087-1091 (1981).

2-5. Borsuk, J. A., and Swanson, R. M., Current Transient Spectroscopy: A High-Sensitivity DLTS System, *IEEE Trans. Electron Devices* ED-27, 2217-2225 (1980).

2-6. Shockley, W., and Read, W. T., Jr., Statistics of the Recombination of Holes and Electrons, *Phys. Rev.* 87, 835-842 (1952).

2-7. Oettinger, F. F., Ed., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1 to December 31, 1977, DoE Report HCP/T 6010/A021-02 (September 1978), pp. 40-46.

2-8. Larrabee, R. D., Thurber, W. R., and Bullis, W. M., *Semiconductor Measurement Technology:* A FORTRAN Program for Calculating the Electrical Parameters of Extrinsic Silicon, Nat. Bur. Stand. (U.S.), Spec. Publ. 400-63 (U.S. Department of Commerce/National Bureau of Standards, Washington, D.C., 1980).

2-9. Ghandhi, S. K., *Semiconductor Power Devices: Physics of Operation and Fabrication Technology*, pp. 2-31 (John Wiley and Sons, New York, (1977).

3. INTRODUCTION OF SPECIFIC IMPURITIES INTO SILICON AND THEIR CHARACTERIZATION BY DEEP-LEVEL AND PHYSICAL CHARACTERIZATION TECHNIQUES

3.1 Task Objectives

The ability to detect both intentional and unintentional impurities in order to take corrective action when necessary would greatly enhance the manufacturer's capability to control the quality (yield, reliability, and cost) of his product. The rapid identification and quantification of deep-level states requires prior knowledge of the characteristics of each energy level. However, there are often a number of different values of activation energy reported in the literature for material doped with the same impurity. It is probable that some of the discrepancies can be attributed to measurement problems in general (e.g., nonexponential transients, inaccurate thermometry) and to variability unintentionally introduced by differences in the processing of test devices or in experimental conditions during the measurement.

The emphasis of this continuing task is to (1) improve measurement methods to obtain more accurate values for the parameters of deep-level states and (2) introduce known impurities into silicon and measure their characterization parameters, with the ultimate goals of developing a catalog of well-characterized deep-level states and a deep-level-doped standard reference specimen.

3.2 Approaches Being Pursued

Transient-capacitance spectroscopy has emerged as a very useful method for determining the parameters of deep impurity levels in semiconductors. However, parameters are often derived from experimental capacitance transients without testing for their exponentiality. It follows that erroneous values for activation energies and cross sections may be reported when the standard analysis, correct only for exponential transients, is used.

A novel method to detect nonexponential transients using a conventional double-boxcar deep-level transient-spectroscopy system was investigated and found to be sufficiently sensitive to examine typical cases of interest. It relies only on the reproducibility of the instrumentation, not on its absolute accuracy.

A more rigorous analysis was also made of the capacitance transient in a space charge layer due to thermal emission from charged defect centers in a semiconductor depletion region. This analysis extends the range of applicability of capacitance-transient defect characterization techniques to nonexponential transient conditions such as those found in heavily doped diodes and those occurring when defect centers are charged in only a part of the depletion region. Examples of the improvement are shown for capacitance transients recorded under isothermal conditions for silicon diodes heavily doped with platinum.

This analysis was also applied to the more widely used DLTS method. This results in a correction term to the conventional DLTS time constant. Application of this more general analysis to a specimen heavily doped with platinum is in progress.

Precision thermometry continues to be an essential concern for the accurate identification and characterization of electrically active defect centers in semiconductors by deep-level measurement techniques. The use of a platinum resistance thermometer to calibrate the temperature-sensing diodes, which measure the temperature of the device under test, was investigated and found to be a major improvement over previous calibrations using a thermocouple.

DLTS investigations of the deep levels introduced by sulfur in silicon continued in order to gain a better understanding of ways to resolve a very complex DLTS spectra. The DLTS response as a function of trap-charging time was investigated, and this approach clearly resolved two peaks that otherwise appeared as an unresolved shoulder on a main peak.

3.3 Accomplishments During Reporting Period

3.3.1 A Novel Method to Detect Nonexponential Transients in DLTS*

There are several ways that one can obtain a nonexponential current or capacitance transient, each of them with a different underlying cause. The most obvious is the case in which more than one defect contributes to the transient and each defect has its own exponential decay with different decay parameters. A single defect with a multiple-step decay process, such as a negative-U defect [3-1] under photoexcitation, can also give a nonexponential transient. The fact that the change in free carrier density at the edge of the depletion region is not abrupt gives rise to a distribution of transients [3-2] from the transition region at the interface between the depletion layer and the neutral semiconductor. If the density of deep levels is not small compared to the dopant density, the capacitance transient no longer has an exponential form [3-3]. Also, the emission rate may depend on electric field which results in a continuous distribution of time constants coming from different depths of the depletion region. Finally, charging the traps in only part of the depletion region (a transient capacitance in series with a constant capacitance) will also yield nonexponential transients.

We have excluded from consideration instrumental artifacts such as system response times [3-4] which could produce nonexponential transients, but could do so independent of the actual sample under study. Also, we have excluded effects of large sample resistance, either bulk or contact, which could give a circuit R-C time constant that, when combined with the emission time constant, would produce a nonexponential output.

In the case of an isothermal spectroscopic method, one could simply measure the transient directly and then test that transient for exponentiality [3-5]. From a survey of the literature, it appears that most DLTS systems are not designed for isothermal measurements. For the transients normally examined in a DLTS experiment, a fast transient recording system with high precision would also be required. Consequently, we have investigated a relatively simple test which can be performed by varying the gate delay times on a con-

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* This section largely comprises the text of a paper having the same title, by W. R. Thurber, R. A. Forman, and W. E. Phillips, to be published in *J. Appl. Phys.*, October 1982.

ventional double-boxcar DLTS system. Elaborate temperature control is not required, only run-to-run reproducibility.

3.3.1.1 Analysis

In the following analysis of a capacitance transient by the double-boxcar procedure, the electron emission rate, e_n, is given by:

$$e_n = g^{-1} v_{th} \sigma_n N_c \exp(-\Delta E_n/kT) ,$$

where g is the degeneracy factor, v_{th} is the electron thermal velocity, σ_n is the capture cross section for electrons, N_c is the density of states in the conduction band, ΔE_n is the change of Gibbs free energy when an electron is emitted into the conduction band from the deep level in question, k is the Boltzmann constant, and T is the absolute temperature. An analogous equation holds for holes.

The capacitance transient of interest arises from the emission of trapped electrons from the deep level when the reverse bias is reestablished after a charging pulse. The transient can be modeled by:

$$C(t, T) = \left[C_f - \left(C_f - C_i\right) \exp\left(-e_n t\right)\right]_T ,$$

where C(t,T) is the measured capacitance as a function of time, t, at the essentially constant temperature, T, and C_i and C_f are the initial and final capacitances of the transient response. The double boxcar determines the difference in capacitance at gate delay times of t_1 and t_2. The output signal is:

$$\Delta C = C\left(t_1,T\right) - C\left(t_2,T\right) = \left[\left(C_i - C_f\right)\left[\exp\left(-e_n t_1\right) - \exp\left(-e_n t_2\right)\right]\right]_T .$$

A peak in this signal as a function of temperature occurs when [3-6]

$$e_n = \frac{\ln\left(t_1/t_2\right)}{t_1 - t_2} .$$

It is more convenient to use this relationship in its reciprocal form, which is:

$$\tau_{max} = \frac{1}{e_n} = \frac{t_1 - t_2}{\ln\left(t_1/t_2\right)} ,$$

where τ_{max} is the time constant of the DLTS transient at the temperature where the signal is a maximum; $1/\tau_{max}$ is often called the rate window.

If the measured transient is exponential, then the individual values of t_1 and t_2 which produce a given τ_{max} are unimportant for the analysis of the data. In fact, many papers give only the rate window and not the individual gate times. A given value of τ_{max} can, however, be obtained by widely differing pairs of t_1 and t_2 values. We have attempted to use this property of τ_{max} to test for exponentiality the responses of selected samples measured in a conventional double-boxcar DLTS apparatus. We have examined samples in which the transient is known to be a good exponential, where incomplete collapse of the depletion region produces a nonexponential transient, where high doping effects distort the transient, and where emission from more than one defect level is contributing to the transient. In each of the nonexponential cases, the temperature of the DLTS peak was found to depend on the values of t_1 and t_2 even though τ_{max} was unchanged.

3.3.1.2 Results

The measurements reported here have been performed on wafers using a variable temperature wafer chuck with a temperature range from -196°C to 350°C [3-7]. Thermal scan rates were typically 0.1°C/s in the heating direction only. The capacitance bridge is a specially designed variable frequency type with rf phase-sensitive detection performed using a balanced mixer [3-8]. For the measurements described in this work, the bridge was operated at 20 MHz.

Figure 3-1 shows a family of DLTS curves obtained on a p^+n diode fabricated on platinum-doped, n-type silicon (wafer 93A). The peak of all of the curves occurs at the same temperature suggesting that the capacitance transient has a single exponential decay. Indeed, this conclusion is supported by careful examination of a complete transient recorded under isothermal conditions. The parameters of the wafers used in this investigation are given in table 3-1, and for wafer 93A, the deep impurity density is only 10 percent of the shallow impurity density; consequently, a good exponential would be expected. The curves were made with t_1 and t_2 settings which gave τ_{max} = 500 µs. The individual t_1 and t_2 values are listed in table 3-2. Experimentally, one usually finds that there is a minimum value of t_1 that is feasible, which depends upon the recovery time of the system from the reverse bias transient. Very large values of t_2 are normally impractical as these would then limit the duty cycle and thus necessitate slow thermal scan rates to obtain reasonable signal-to-noise ratios. Consequently, t_2/t_1 ratios of greater than 50 are usually not feasible. At the other extreme, t_2/t_1 ratios of less than 2 result in an output signal which is too low for satisfactory operation. The duration of the sampling gates was 5 µs, and one-half of this, or 2.5 µs, is included in the listed t_1 and t_2 values. To be certain that this gate duration had no effect on the conclusion, scans were made with a gate duration of 0.5 µs and no change was seen in the DLTS peak positions. The wider gates give better signal-to-noise ratios and are preferred for this reason. To show the sensitivity of τ_{max} to the individual t_1 and t_2 values, table 3-2 gives changes in these values ($\delta t_1, \delta t_2$) which would produce a 5-percent change in τ_{max} corresponding to a shift of 0.35°C in the position for the DLTS peaks in figure 3-1. This shift is about equal to the repeatability of the curves shown.

The bias-voltage sequence used for the curves in figure 3-1 was -5,0,-5 V* which resulted in essentially complete collapse of the depletion region dur-

* Initial reverse bias of -5 V, trap-charging voltage of 0 V, and -5 V reverse bias during observation of DLTS transient.

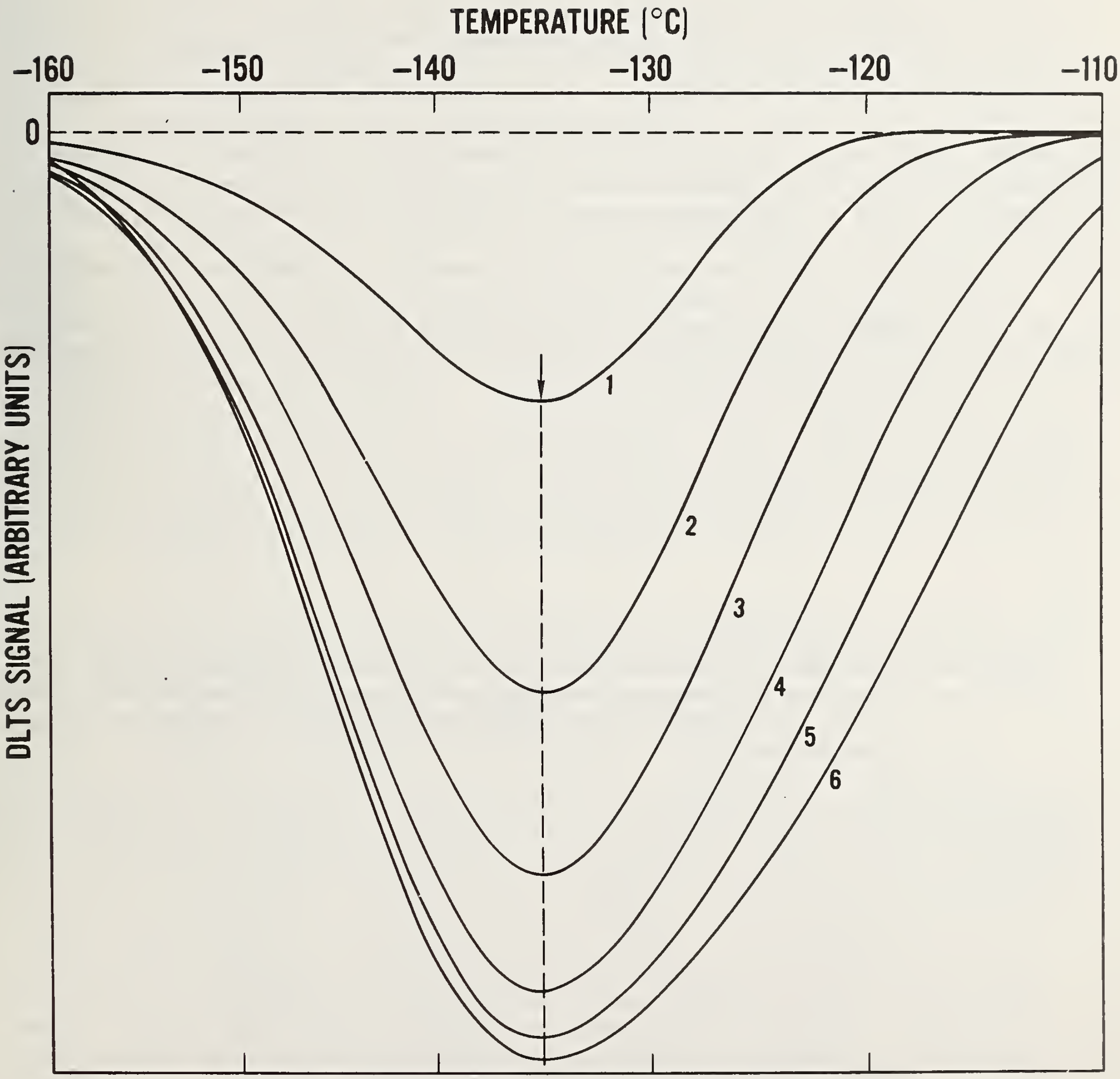

Figure 3-1. DLTS curves for a p^+n diode on wafer 93A with a bias sequence of -5,0,-5 V. The t_1 and t_2 values are given in table 3-2. The curve with the smallest ratio of t_2/t_1 is at the top and the one with the largest ratio is at the bottom. Note that the peak temperature is the same for all curves. A negative DLTS peak corresponds to majority carrier (electron) emission.

Table 3-1. Parameters of the Wafers Used for This Work.

Fig. No.	Wafer No.	Shallow Impurity Species	Shallow Impurity Density	Deep Impurity Species	Deep Impurity Density
3-1, 3-2	93A	Phosphorus	1.2×10^{15}	Platinum	1.5×10^{14}
3-3	94C	Boron	3.5×10^{15}	Platinum	3.2×10^{15}
3-4	R32NB	Phosphorus	6×10^{13}	?	5×10^{10}

Table 3-2. Gate Delay Times in Microseconds Used for the DLTS Curves in Figures 3-1 through 3-3 (τ_{max} = 500 μs for all pairs) and Change in t_1 and t_2 Which Separately Would Produce a 5% Change in τ_{max} (to 475 μs).

Curve No.	t_1	t_2	t_2/t_1	δt_1	δt_2
1	342.3	700	2.0	-38.0	-61.8
2	203.2	1000	4.9	-26.5	-78.9
3	123.6	1300	10.5	-18.6	-94.6
4	75.9	1600	21.1	-13.0	-110.0
5	54.9	1800	32.8	-10.2	-120.2
6	39.7	2000	50.4	-8.0	-130.6

ing the zero applied voltage trap-charging pulse, as is conventional for this type of DLTS. However, there are applications, such as depth profiling, where the depletion region is only partially collapsed during the charging pulse to observe the defect properties in a narrow spatial region. This gives rise to a fixed capacitance in series with that capacitance due to the region of defect emission, and the resultant transient is no longer truly exponential. When this series capacitance is large compared to the capacitance of the transient, the perturbation is insignificant, but when this is not true, the resultant transient is nonexponential. Also, with incomplete charging, emission from the edge of the depletion region is relatively more important, and this is a source of additional nonexponentiality. To investigate these effects, a family of DLTS curves was obtained for the above wafer using a bias sequence of -5,-4,-5 V. The results in figure 3-2 show that the DLTS peak position varies by almost 2°C depending systematically on the values of t_1 and t_2 even though all pairs have the same τ_{max}. As the spread between t_1 and t_2 is reduced, the DLTS peak shifts successively smaller amounts. This is expected since the pairs are converging on a measurement of the tangent to the transient at $t = \tau_{max}$. This case was also examined by careful isothermal measurements. It was found that the time constant at the beginning of the transient was 11 percent shorter than it was after one time constant. Although these isothermal measurements are made at substantially lower temperatures and consequently longer decay times than the DLTS measurements, the underlying cause of the nonexponential behavior is the same for both cases. Thus, these results can be compared.

In figure 3-3 the nonexponentiality introduced by heavy doping is examined by this method using wafer 94C which was diffused with platinum at 1000°C. The ratio of deep levels to shallow levels was determined to be about 0.9 from a fit of low temperature capacitance-voltage measurements. With a ratio this large, the capacitance transient should not be exponential in form. The results in figure 3-3 confirm this expectation as the DLTS peak shifts a total of 3°C for the scans obtained with the t_1 and t_2 pairs used in the measurement (see table 3-2). The presence of considerable nonexponentiality was also seen in isothermal measurements from which the time constant at the beginning of the transient was found to be 9 percent shorter than that after one time constant and 31 percent shorter than that after two time constants.

Another common cause of nonexponential transients is the overlap of transients from two (or more) different centers. Figure 3-4 shows DLTS curves obtained on a commercial power rectifier diode containing trace amounts of unknown impurities. The curves were made with a τ_{max} of 5 ms; thus the t_1 and t_2 values are ten times those given in table 3-2. With the larger τ_{max}, the peaks occur at lower temperatures and are consequently better resolved. For large ratios of t_2/t_1, there is little obvious evidence of two peaks in figure 3-4. However, for small t_2/t_1 ratios, two peaks are clearly seen, as analysis would predict [3-9]. From more extensive measurements, the two levels were found to have activation energies of 0.25 and 0.29 eV below the conduction band. Energy levels this far apart can usually be detected when curves are run with the wide range of τ_{max} values needed for an Arrhenius plot. However, levels somewhat closer in energy (specifically in emission rate) might go undetected unless scans are made with small ratios of t_2/t_1.

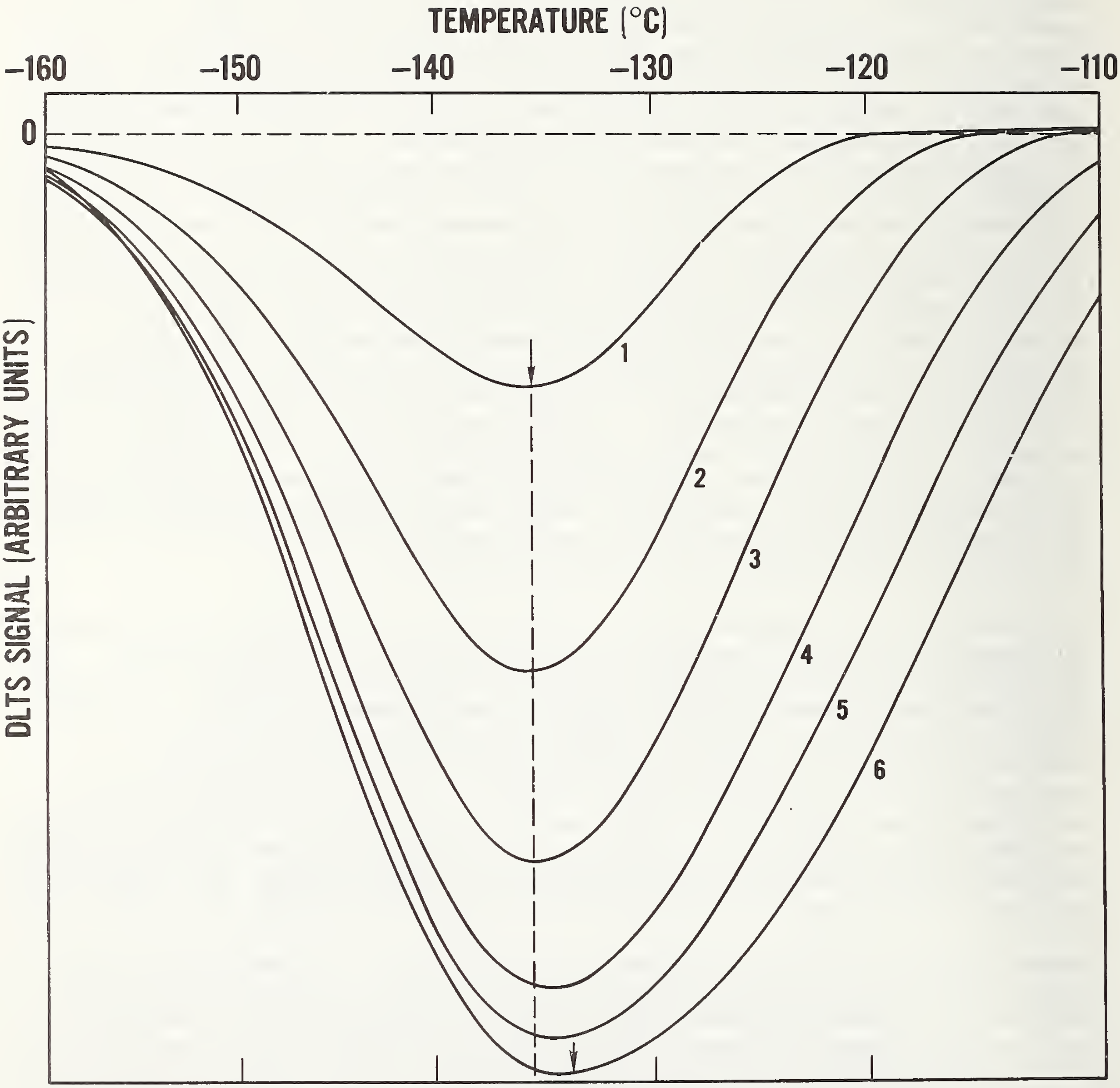

Figure 3-2. DLTS curves for the same diode and gate times as figure 3-1, but with a bias sequence of -5,-4,-5 V. The DLTS peak shifts 2°C because of the nonexponentiality introduced by the relatively large contribution from the depletion edge region and by the capacitance in series with that of the active region.

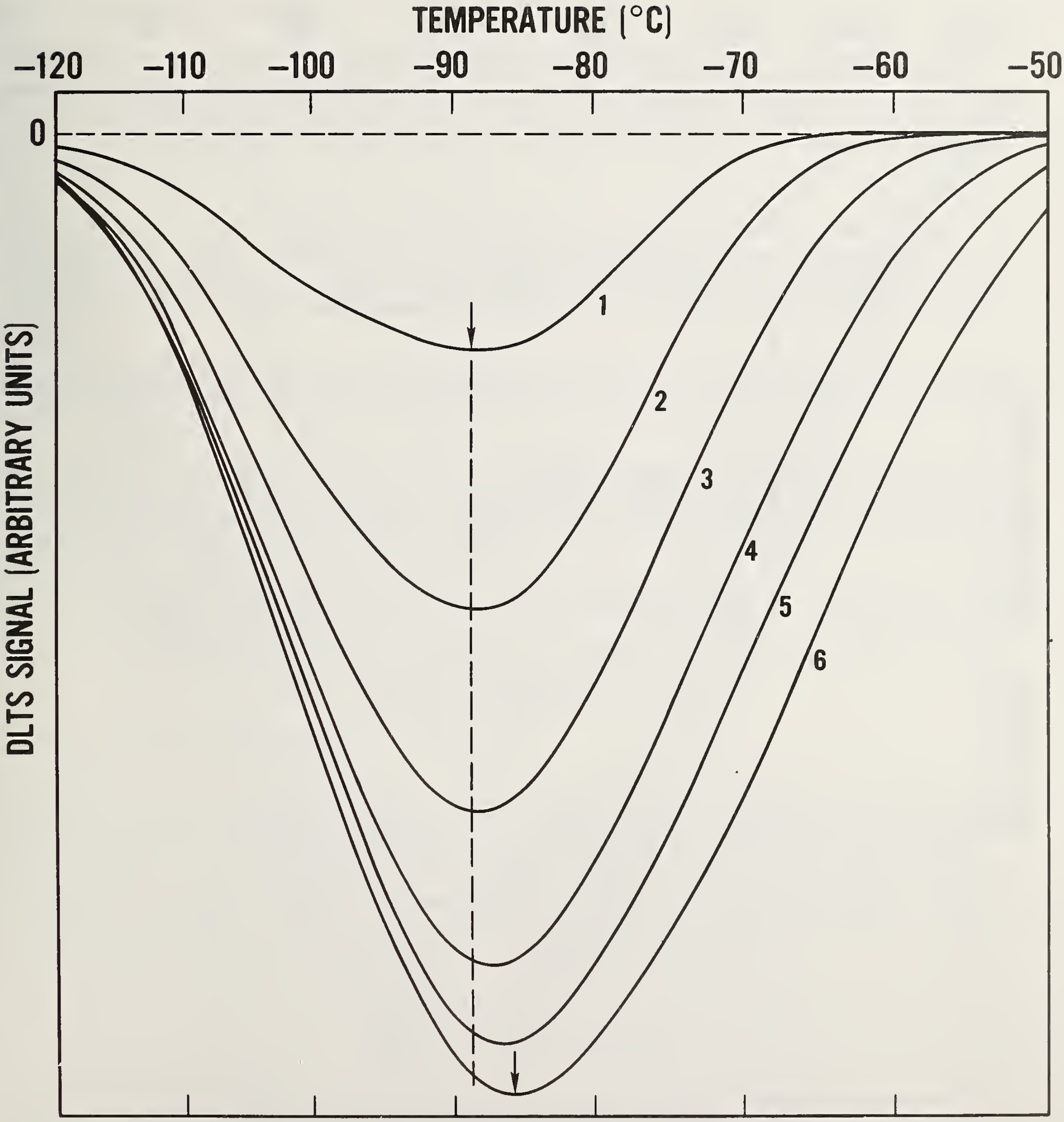

Figure 3-3. DLTS curves for an n^+p diode on wafer 94C with a bias sequence of +5,0,+5 V. The gate delay times are given in table 3-2. The peak shifts 3°C because the transient is nonexponential due to the non-negligible deep-level density compared to the shallow boron density.

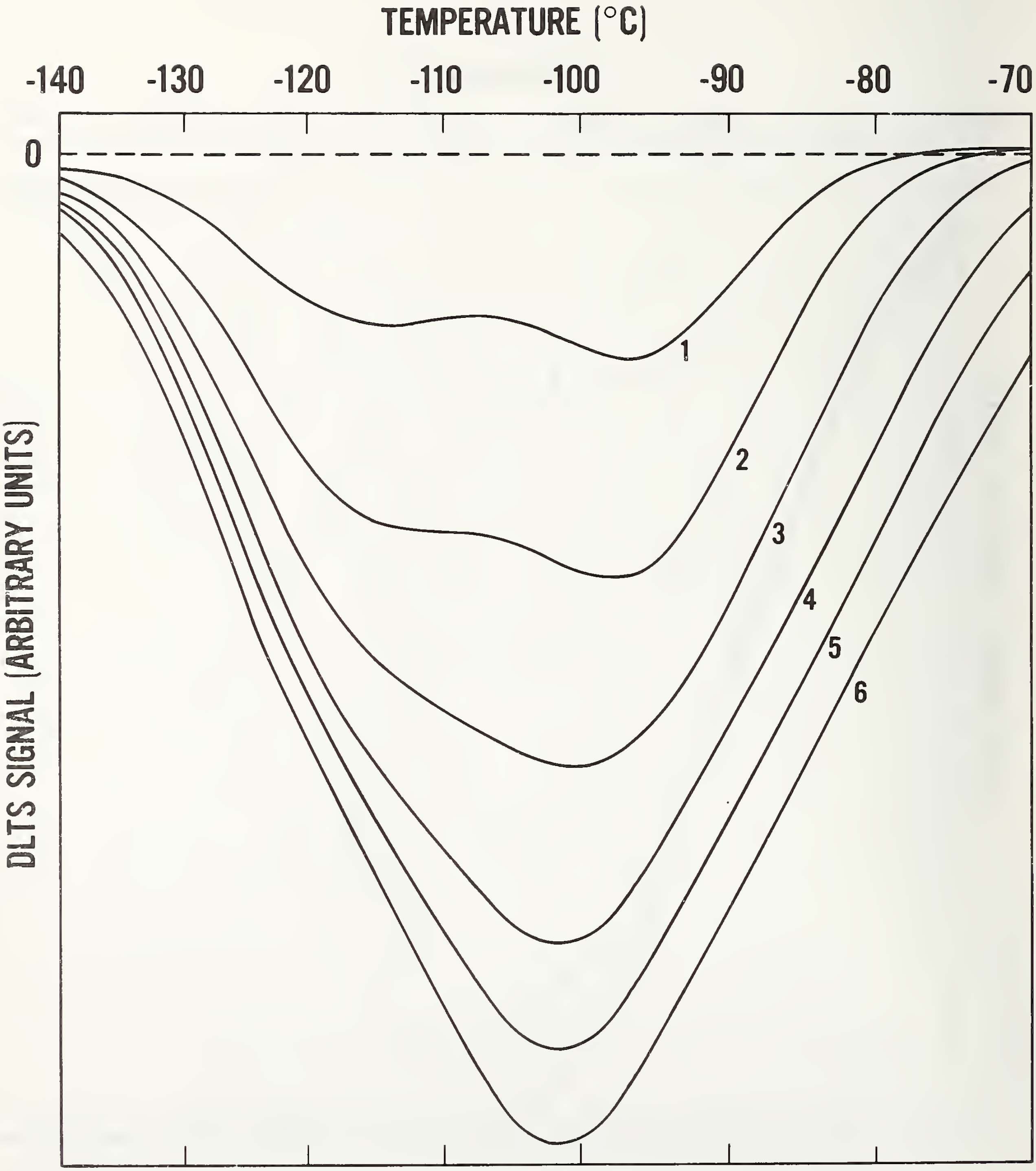

Figure 3-4. DLTS curves from overlapping transients measured on a commercial p^+n power rectifier diode. The bias sequence was -10,0,-10 V and the gate times were ten times larger than those in table 3-2 (τ_m = 5 ms for all curves). The smaller ratios of t_2/t_1 clearly show two peaks which might go unresolved if only large ratios of t_2/t_1 were used.

Once it is established that only one level is contributing to the emission peak, scans can be made with a larger ratio for increased DLTS signal.

3.3.1.3 Conclusions

This test for exponentiality is sufficiently sensitive to examine typical cases of interest and relies only on the reproducibility of the instrumentation, not on its absolute accuracy. When the method is used routinely, only two or three curves, at widely spaced ratios of t_2/t_1, are needed to implement the test.

We expect that the use of this technique (or some equivalent technique) may significantly improve the interlaboratory agreement on the parameters of a given defect [3-10]. In this way, DLTS may more closely approach its early promise as a means for analysis of unknown trace impurities in semiconductors.

3.3.2 <u>Nonexponential-Capacitance ITCAP Transients in Platinum-Doped Silicon Diodes</u>

As discussed in section 3.3.1, there are many causes of nonexponential current or capacitance transients. In the work reported here, a rigorous analysis was used to investigate the capacitance transients in abrupt-junction platinum-doped silicon diodes in which:

1) densities of deep levels were not small compared to the density of the dominant shallow level and
2) trap charging was done over only a portion of the depletion layer (e.g., as occurs in profiling measurements).

3.3.2.1 Theory of Analysis

An analysis of a transient which does not exhibit an exponential behavior in transient capacitance measurements for the reasons stated above can be made as follows. The transient behavior of the junction capacitance when the trap-charging bias is changed to a larger reverse bias, V_r, is controlled in n-type silicon by the electron emission rate from defect centers. The net time rate of change of n_t, the concentration per unit volume of electrons on the defect centers (i.e., traps), is given by [3-11]:

$$\frac{dn_t}{dt} = e_p\, p_t - e_n\, n_t\ , \tag{3-1}$$

where e_n is the electron emission rate, e_p is the hole emission rate, and p_t is the concentration of holes on the defect centers. Because the trap must hold either an electron or a hole, the totality condition is satisfied:

$$n_t + p_t = N_t, \tag{3-2}$$

where N_t is the total defect center density. A differential equation in n_t can be obtained from eqs (3-1) and (3-2):

$$\frac{dn_t}{dt} + (e_n + e_p)n_t = e_p N_t \ . \qquad (3\text{-}3)$$

The general solution of eq (3-3) is

$$n_t = C_1 \exp[-(e_n + e_p)t] + C_2 \ . \qquad (3\text{-}4)$$

The constants C_1 and C_2 can be evaluated at times zero and infinity as $C_1 + C_2 = n_t(0) = n_{ti}$ and $C_2 = n_t(\infty) = n_{tf}$. Equation (3-4) can be written

$$n_t = n_{tf} + (n_{ti} - n_{tf}) \exp[-(e_n + e_p)t] \ . \qquad (3\text{-}5)$$

Under one-sided step-junction conditions, the junction capacitance, C, at reversed bias, V_r, in the complete depletion approximation, is [3-12]

$$C^{-2} = C_b^{-2} + \frac{2(V_r - V_c)}{q\varepsilon A^2(N_d - n_t)} \qquad (3\text{-}6)$$

where C_b is the junction capacitance at some reduced trap-charging bias, V_c, A is the junction area, ε is the absolute dielectric constant (permittivity) of silicon, N_d is the shallow dopant density (assumed to be constant), and q is the electronic charge. Equation (3-6) is also a valid approximation when the reverse bias is large relative to the built-in voltage.

Equation (3-6) can be solved for n_t to give

$$n_t = N_d - \frac{2(V_r - V_c)C_b^2 C^2}{q\varepsilon A^2(C_b^2 - C^2)} \ . \qquad (3\text{-}7)$$

At the initial time (t = 0), the reverse bias is reapplied (at the end of the trap-charging period). Then, n_t is n_{ti} and C is C_i. In the infinite time limit, or final steady-state condition, n_t is n_{tf} and C is C_f. Substitution of n_t, n_{ti}, and n_{tf} into eq (3-5) and solution for the exponential term gives:

$$\exp\left[-(e_n + e_p)t\right] = \frac{(C_b^2 - C_i^2)(C_f^2 - C^2)}{(C_b^2 - C^2)(C_f^2 - C_i^2)} \equiv C_r \ . \qquad (3\text{-}8)$$

The right side of eq (3-8) is a capacitance ratio and will be called C_r. The same equation can also be expressed in terms of C as:

$$\frac{C^2}{C_b^2 - C^2} = \frac{C_f^2}{C_b^2 - C_f^2} + \left[\frac{C_i^2}{C_b^2 - C_i^2} - \frac{C_f^2}{C_b^2 - C_f^2}\right] e^{-t/\tau} \qquad (3\text{-}9)$$

where $\tau = 1/(e_n + e_p)$.

For the special case where the depletion region is almost entirely collapsed, C_b is relatively large so that $C_b^2 >> C_i^2$ and C_f^2, and C is bracketed in value by C_i and C_f. Then the denominators in eq (3-9) are approximately equal so that

$$C^2 - C_f^2 \simeq \left(C_i^2 - C_f^2\right) e^{-t/\tau} .$$

The difference of squares can be factored and for $C_i \approx C_f \approx C$ (i.e., N_t/N_d small), the sums $(C + C_f)$ and $(C_i + C_f)$ are approximately $2C_f$ so that

$$C \simeq C_f + \left(C_i - C_f\right) e^{-t/\tau} . \qquad (3\text{-}10)$$

Therefore, the conventional analysis in which an exponential transient is assumed is valid for N_t/N_d small and for C_b large (depletion region almost entirely collapsed during the trap-charging phase). Under such conditions, the conventional DLTS plot of $\log \dfrac{C - C_f}{C_i - C_f}$ against time would be linear with a slope proportional to $1/\tau$. However, when these conditions are violated, as is shown below in the devices studied here, it is necessary to use the more rigorous analysis leading to eq (3-8) which predicts that a plot of $\log C_r$ against time would be linear with a slope proportional to $-1/\tau$ (equal to $-1/\tau$ if the natural logarithm is used).

3.3.2.2 Device Fabrication

The devices used in this study are gated p^+n and n^+p diodes (device no. 10 of test pattern NBS-3 [3-13] and were fabricated on 3 to 5 Ω•cm <111> *n*- or *p*-type silicon wafers. On the *n*-type wafer, boron predeposition and diffusion through 0.432-mm diameter openings in 500 nm of field oxide formed 450-nm deep p^+ regions. The back side of this device was stripped and coated with a spun-on platinum emulsion followed by a drive in at 900°C for 1 h in a dry nitrogen ambient. The residual platinum was etched from the back side. Contact opening, top metallization (aluminum), back metallization (gold plus 0.6-percent antimony), top metal definition, and a 10-min 500°C microalloy in dry nitrogen completed the fabrication of the structure. The structure was hermetically packaged in a TO-100 header on a ceramic chip along with an electrically isolated temperature-sensing diode which was in good thermal contact with the test device. The n^+p diodes were fabricated in a complementary manner with a platinum diffusion temperature of 1000°C for 1 h.

3.3.2.3 Device Characteristics

The spatial dependence of the emission rate for a p^+n diode was investigated by isothermal transient capacitance (ITCAP) measurements [3-14] in incremental depletion layers of uniform width and electric field distributions. These tests were accomplished by 1) applying a reverse bias of 2 V to the specimen diode, 2) waiting for equilibrium conditions, 3) partially collapsing the depletion region by reducing the bias to 0 V, 4) waiting a few seconds for the traps in the previously depleted region to fill with majority carriers, and 5) then restoring the reverse bias to 2 V. The capacitance transient response was recorded on an x-y recorder during and following these bias changes (see fig. 3-5). The transient response was analyzed to obtain the emission rate. The measurements were repeated at a greater average distance from the junction by increasing the initial 2 V of reverse bias, but maintaining the same width of the active region (i.e., the portion of the space-charge region which upon reduction of bias fills with majority carriers). This was accomplished by making the charging bias, V_c, in volts and the reverse bias during the transient, V_r, in volts obey the equation: $\sqrt{V_r} - \sqrt{V_c} = \sqrt{2}$. This equation assumes an abrupt junction for which the total depletion depth varies with the square root of the reverse bias voltage. The constant difference of square roots produces an active region of constant width but at various distances from the junction. The voltage across this active portion of the depletion region remains constant at 2 V as V_r and V_c (and thus the depth) changes.

The series of measurements described above gave transients with a constant emission rate in the range of 2 to 20 V reverse bias. The tests were repeated with a larger average electric field ($\sqrt{V_r} - \sqrt{V_c} = \sqrt{5}$, i.e., 5 V across the active region) with the same resultant emission rate. A completely independent experiment with sulfur-doped silicon showed variations with both electric field and position of the active region. Therefore, for the case of the platinum-doped device, it was concluded that the emission rate is independent of these electric field variations in the depletion region and the position of the active region relative to the junction. If this lack of electric field or spatial dependencies found for the emission rate of the devices studied here is a general property of platinum-doped silicon, such devices would be good candidates for studies of deep levels.

3.3.2.4 Results

A typical as-measured isothermal capacitance variation is shown in figure 3-5. The absence of a transient in C_b (the capacitance under trap-charging conditions) indicates that a slow-capture region resulting from spatially nonuniform capture rate [3-15,3-16] is not a problem. Should a transient be observed, one can wait until the traps in the slow-capture region are filled. This is feasible in ITCAP measurements but might be more difficult to achieve in DLTS measurements. In figure 3-6, the transient response of figure 3-5 has been replotted as open circles from digitized data as log $\left[(C - C_f)/(C_i - C_f)\right]$ against time. The plot is seen to be nonlinear indicating that the measured capacitance transient is nonexponential. The instantaneous time constant (reciprocal of the emission rate) is proportional to the slope of the line and is dependent upon the time at which it is measured. The initial slope is shown as a dashed line and has a time constant of 12.7 s. The nonexponentiality of the capacitance transient is attributed to violation of the small N_t/N_d approximation $(N_t/N_d = 0.4)$ and to charging of traps in only part (~1/3) of the depletion region.

In contrast, a plot of the logarithm of C_r of eq (3-8) against time for the transient of figure 3-5 is shown as solid dots in figure 3-6. The solid line

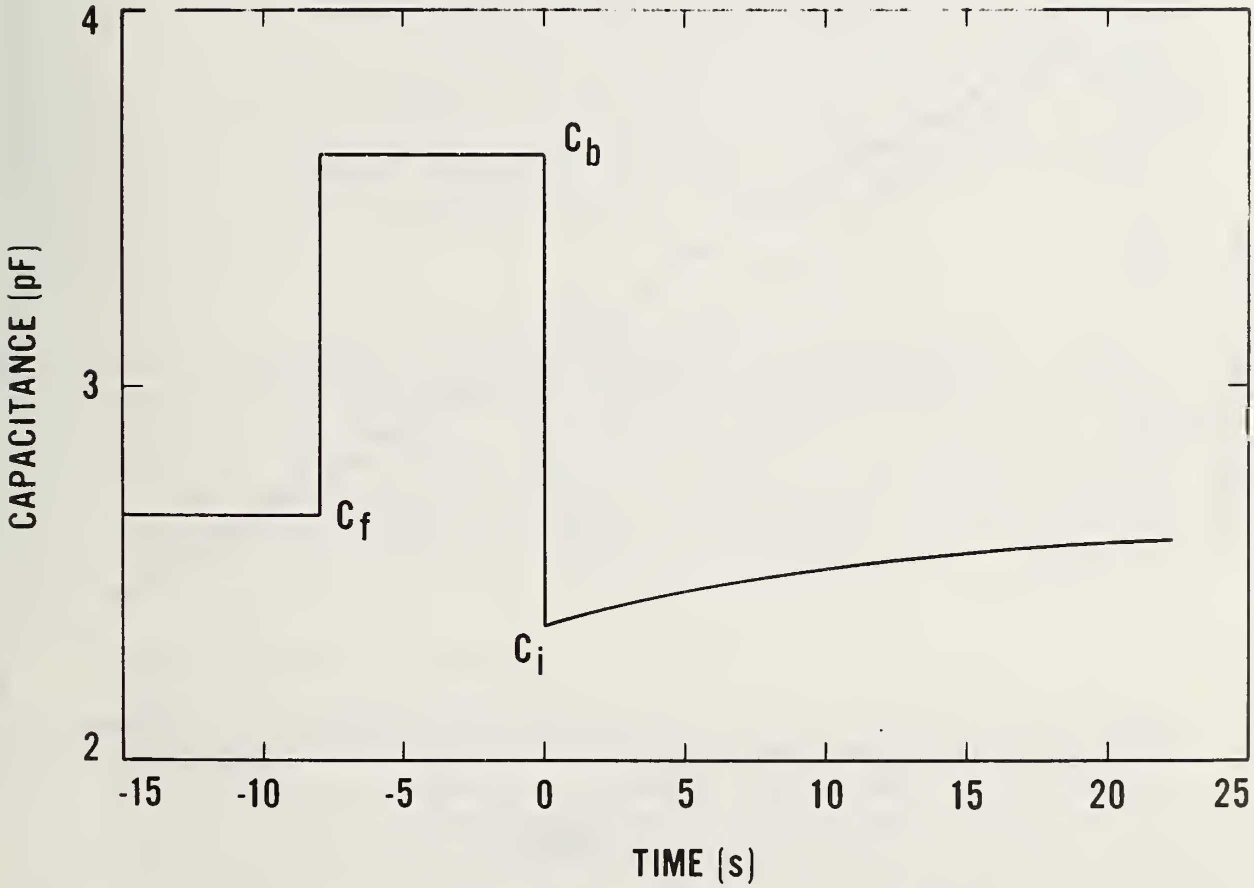

Figure 3-5. Transient capacitance response against time of a p^+n silicon diode heavily doped with platinum ($N_t/N_d \approx 0.4$). Initial reverse bias is 20 V, charging reverse bias is 9.351 V, and the temperature is 88 K. C_i = 2.36 pF, C_f = 2.65 pF, and C_b = 3.62 pF.

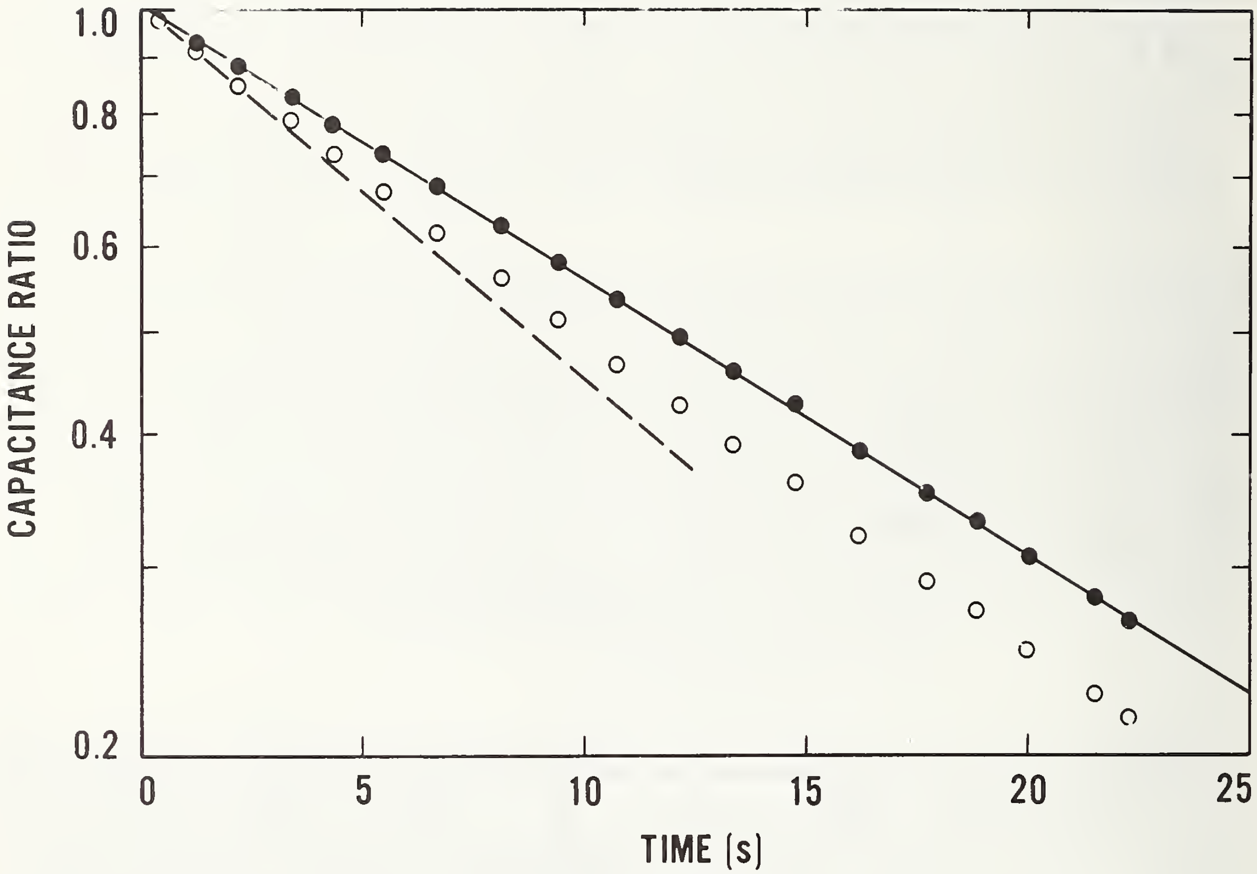

Figure 3-6. Semilogarithmic digitized and normalized replot of the transient capacitance ratio of figure 3-5 (shown as open circles) against time. The dashed line is the initial slope. The solid circles are the same data with the more rigorous analysis which leads to the capacitance ratio C_r given by eq (3-8). The solid line is a weighted linear regression fit to the data of log C_r against time.

is a weighted linear regression fit to the data with a weighting factor of C_r.

A more dramatic difference is shown in figure 3-7 for the more heavily doped p^+n diode $\left(N_t/N_d = 0.9\right)$ with about 18 percent of the depletion region charged. The significance of the linearity of the log C_r plots in both figures 3-6 and 3-7 is that the present analysis correctly accounts for the large trap density and for the unchanging capacitance in the uncharged depletion region in series with the transient capacitance in the charged portion of the depletion region. In figure 3-6, the time constant was found to be 16.88 ± 0.03 s, which is about 34 percent greater than the time constant indicated by the initial slope of the uncorrected capacitance data and about 16 percent greater than that of a straight line fitted to all of the uncorrected data. In figure 3-7, the time constant is 16.85 ± 0.02 s, which is about 150 percent greater than the time constant indicated by the initial slope of the uncorrected capacitance data.

3.3.2.5 Conclusions

It is concluded that the use of the present more rigorous analysis can correct for the nonexponentiality introduced by the heavy density of defect centers and for trap charging in only a part of the depletion region. It was shown that for small density of traps and for charging these traps over the entire depletion region, the conventional exponential approximation should be adequate. The present analysis extends the range of applicability of transient capacitance techniques to conditions encountered in practical devices $\left(\text{e.g., } N_t/N_d \text{ not} \ll 1\right)$ and in more detailed measurements (e.g., deep-level profiling).

3.3.3 A More General DLTS Analysis

The widespread use and the great convenience of the deep-level transient spectroscopy method [3-6] have motivated an effort to extend the advantages of the more inconvenient isothermal transient capacitance [3-14] method to DLTS. The DLTS method assumes an exponential capacitance transient when filled trapping centers of a depletion region are thermally emptied. This is a good approximation (see sec. 3.3.2.1) only for a light density of trapping centers compared to the backgound doping level and for the filling of trapping centers throughout the depletion region. If either condition is violated, a more complete analysis (as in the above ITCAP method) is required. The purpose of this section is to provide such an analysis and to show that it adds a correction term to the conventional DLTS time constant.

3.3.3.1 Theory

Equation (3-8) can be rearranged as

$$C = \left[\frac{1}{C_b^{\,2}} + \frac{1}{\dfrac{C_b^{\,2}C_f^{\,2}}{C_b^{\,2} - C_f^{\,2}} + \left(\dfrac{C_b^{\,2}C_i^{\,2}}{C_b^{\,2} - C_i^{\,2}} - \dfrac{C_b^{\,2}C_f^{\,2}}{C_b^{\,2} - C_f^{\,2}}\right)e^{-t/\tau}}\right]^{-1/2}, \tag{3-11}$$

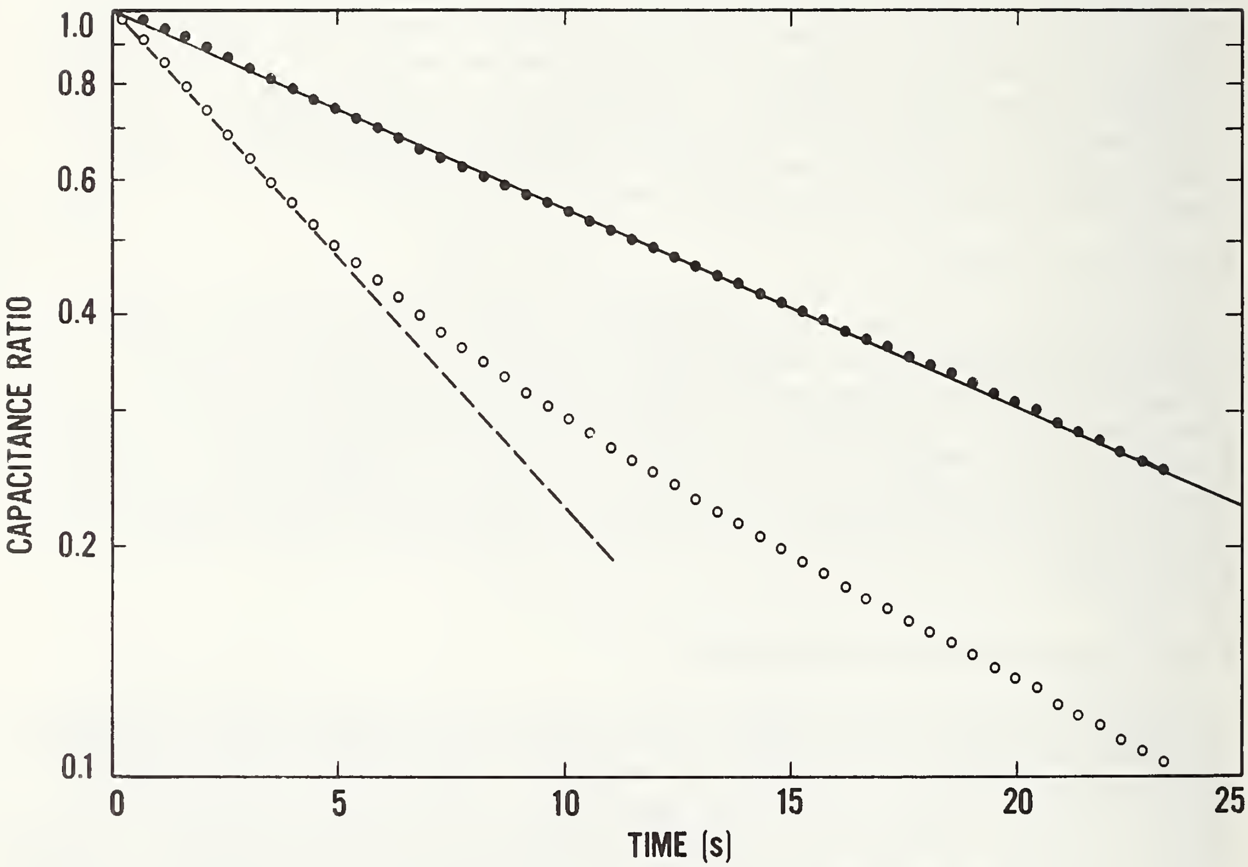

Figure 3-7. Same as figure 3-6 except the diode is n^+p and is more heavily doped with platinum ($N_t/N_a \approx 0.9$). Initial reverse bias is 9 V, charging reverse bias is 3 V, and the temperature is 124 K. C_i = 2.00 pF, C_f = 3.25 pF, and C_b = 3.95 pF.

where C is the time-dependent junction capacitance, C_f is the equilibrium junction capacitance under reverse bias conditions, C_b is the junction capacitance when the reverse bias has been reduced to collapse the depletion region in order to charge the traps with majority carriers in the collapsed depletion region, C_i is the junction capacitance at time zero when the reverse bias is restored, t is time, and τ is the time constant for emptying the traps (the reciprocal of the sum of electron and hole emission rates e_n and e_p).

The DLTS signal peak occurs when its derivative with respect to τ is zero, i.e., when $\frac{dC}{d\tau}$ values at the two selected DLTS sampling times t_1 and t_2 are equal. The derivative of eq (3-11) with respect to τ is

$$\begin{aligned}\frac{dC}{d\tau} &= \frac{d}{d\tau}\left(a + \frac{1}{b + ce^{-t/\tau}}\right)^{-1/2} \\ &= \frac{te^{-t/\tau}}{2\tau^2}\, c\left(b + ce^{-t/\tau}\right)^{-2}\left(a + \frac{1}{b + ce^{-t/\tau}}\right)^{-3/2},\end{aligned} \tag{3-12}$$

where

$$a = \frac{1}{C_b{}^2},\quad b = \frac{C_b^2\, C_f^2}{C_b{}^2 - C_f{}^2},\quad \text{and } c = \frac{C_b{}^4\left(C_i{}^2 - C_f{}^2\right)}{\left(C_b{}^2 - C_i{}^2\right)\left(C_b{}^2 - C_f{}^2\right)}\,.$$

Because dC/dτ involves fractional powers, eq (3-12) is squared to give

$$\frac{t_1{}^2 e^{-2t_1/\tau}}{\left(b + ce^{-t_1/\tau}\right)^4\left(a + \dfrac{1}{b + ce^{-t_1/\tau}}\right)^3} = \frac{t_2{}^2 e^{-2t_2/\tau}}{\left(b + ce^{-t_2/\tau}\right)^4\left(a + \dfrac{1}{b + ce^{-t_2/\tau}}\right)^3} \tag{3-13}$$

and rearranged as

$$\begin{aligned}&\frac{e^{2t_1/\tau}}{t_1{}^2}\left(D_0 + D_1 e^{-t_1/\tau} + D_2 e^{-2t_1/\tau} + D_3 e^{-3t_1/\tau} + D_4 e^{-4t_1/\tau}\right) = \\ &\frac{e^{2t_2/\tau}}{t_2{}^2}\left(D_0 + D_1 e^{-t_2/\tau} + D_2 e^{-2t_2/\tau} + D_3 e^{-3t_2/\tau} + D_4 e^{-4t_2/\tau}\right),\end{aligned} \tag{3-14}$$

where the D's are polynomials of a, b, and c. Rearrangement and taking the square root of eq (3-14) yields:

$$e^{\frac{t_1 - t_2}{\tau}} = \frac{t_1}{t_2}\sqrt{\frac{B_2}{B_1}} , \qquad (3\text{-}15)$$

where

$$B_1 = 1 + A_1 e^{-t_1/\tau} + A_2 e^{-2t_1/\tau} + A_3 e^{-3t_1/\tau} + A_4 e^{-4t_1/\tau} ,$$

$$B_2 = 1 + A_1 e^{-t_2/\tau} + A_2 e^{-2t_2/\tau} + A_3 e^{-3t_2/\tau} + A_4 e^{-4t_2/\tau} ,$$

$$A_1 = \frac{D_1}{D_0} = \frac{(C_i^2 - C_f^2)(C_b^2 + 3C_f^2)}{C_f^2(C_b^2 - C_i^2)} ,$$

$$A_2 = \frac{D_2}{D_0} = \frac{3(C_i^2 - C_f^2)^2(C_b^2 + C_f^2)}{C_f^2(C_b^2 - C_i^2)^2} ,$$

$$A_3 = \frac{D_3}{D_0} = \frac{(C_i^2 - C_f^2)^3(3C_b^2 + C_f^2)}{C_f^2(C_b^2 - C_i^2)^3} , \text{ and}$$

$$A_4 = \frac{D_4}{D_0} = \frac{(C_i^2 - C_f^2)^4 C_b^2}{C_f^2(C_b^2 - C_i^2)^4} .$$

Rearrangement of eq (3-15) after taking the natural logarithm gives:

$$\tau = \frac{t_1 - t_2}{\ln\left(\frac{t_1}{t_2}\right) + \ln\sqrt{\frac{B_2}{B_1}}} . \qquad (3\text{-}16)$$

Because τ appears in B_1 and B_2, an iterative solution is required. The exponential solution $\tau = (t_1 - t_2)/\ln (t_1/t_2)$ is a good initial value. The iteration converges rapidly by substitution of successively calculated values. Application of this analysis to DLTS data obtained on a platinum-doped diode is in progress and will be reported at a later date.

3.3.4 Improvements in ITCAP Thermometry

The present temperature-measurement procedures for the ITCAP method have been previously described [3-17]. A forward-biased, gold-doped silicon diode is used as the temperature-sensing device, and it is compact enough to be placed in good thermal contact with the specimen under test on a ceramic chip attached to a 10-pin TO-100 package. The sensitivity of the temperature-sensing diode makes it ideal for this application. However, its stability with time is not yet established and calibration before and after each precision use is required.

Each temperature-sensing diode mounted in a TO-100 package as discussed above is calibrated individually against a platinum resistance thermometer which has been calibrated by the Temperature and Pressure Measurement and Standards Division of the National Bureau of Standards. The TO-100 package is in good thermal contact with a high-conductivity copper heat sink in which are embedded the platinum thermometer and dual Type K [3-18] thermocouples. One thermocouple is connected to a temperature regulator which controls the power input to an electrical heater which is attached to the copper heat sink. The other thermocouple is connected to a temperature indicator which electronically compensates for the reference junction potential, linearizes the thermocouple output, and digitally displays the temperature with 0.1-K resolution. The nominal 25-Ω platinum resistance thermometer is connected to an ohmmeter which reads its resistance with a milliohm resolution (a round-off error of 0.5 mΩ corresponds to about 5 mK).

The copper heat sink containing the temperature-sensing diode, the thermocouples, and the platinum thermometer is surrounded by an evacuated metal jacket and immersed in liquid nitrogen in a Dewar.

The system is allowed to reach quasi-temperature equilibrium by cooling at an approximate rate of one-fifth a degree per minute through the temperature range to be calibrated. The digital thermocouple reading, the temperature-sensing diode voltage, and the resistance of the platinum thermometer are recorded at a number of temperatures. A plot of 300 individual data points of temperature-sensing diode forward voltage against the platinum reference temperature, T_R, is shown in figure 3-8. The temperature, T_R, is derived from the platinum thermometer resistance [3-19]. The calibration curve is seen to be approximately piecewise linear with a change of slope at about 227 K. A piecewise third order regression fit to the calibration data was made over six segments of 50 points each. The equation of each calibration curve segment is then used within its range to calibrate the temperature-sensing diode. Higher order regressions did not improve the fit significantly. Except for the two segments adjacent to the change of slope, a third order fit was no better than the linear fit. The stability of the temperature regulation system in achieving and maintaining a fixed temperature, the 10-μV precision with which the relatively large temperature-sensing diode forward voltage drop (about 0.5 V) can be read, and the greater sensitivity of the temperature-sensing diodes (2780 μV/K compared to 34 μV/K for a thermocouple) make it possible to achieve a two-sigma precision of ±8 mK which is an elevenfold improvement over the corresponding thermocouple precision of ±88 mK.

An example of this improvement is illustrated in figure 3-9 for a typical temperature-sensing diode. The dots show the error of the temperature T_D obtained from the temperature-sensing diode $(T_D - T_R)$ as plotted against the reference temperature, T_R, derived from the resistance of the calibrated platinum thermometer as discussed above. The dashed horizontal lines are the two standard deviation limits (±8 mK) of $T_D - T_R$ and correspond to a change

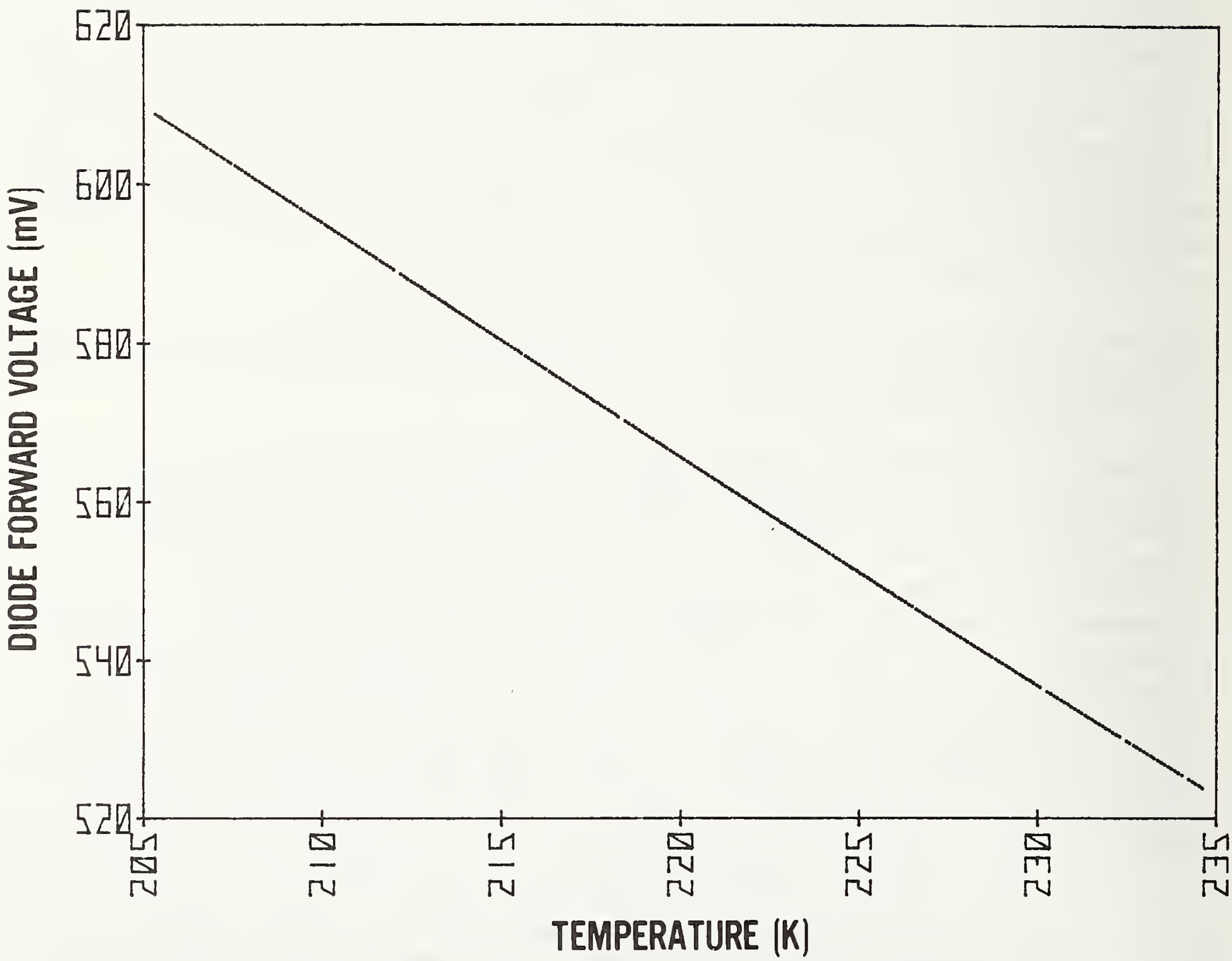

Figure 3-8. Calibration curve of forward diode voltage drop plotted against calibrated platinum resistance thermometer temperature for a representative temperature-sensing diode.

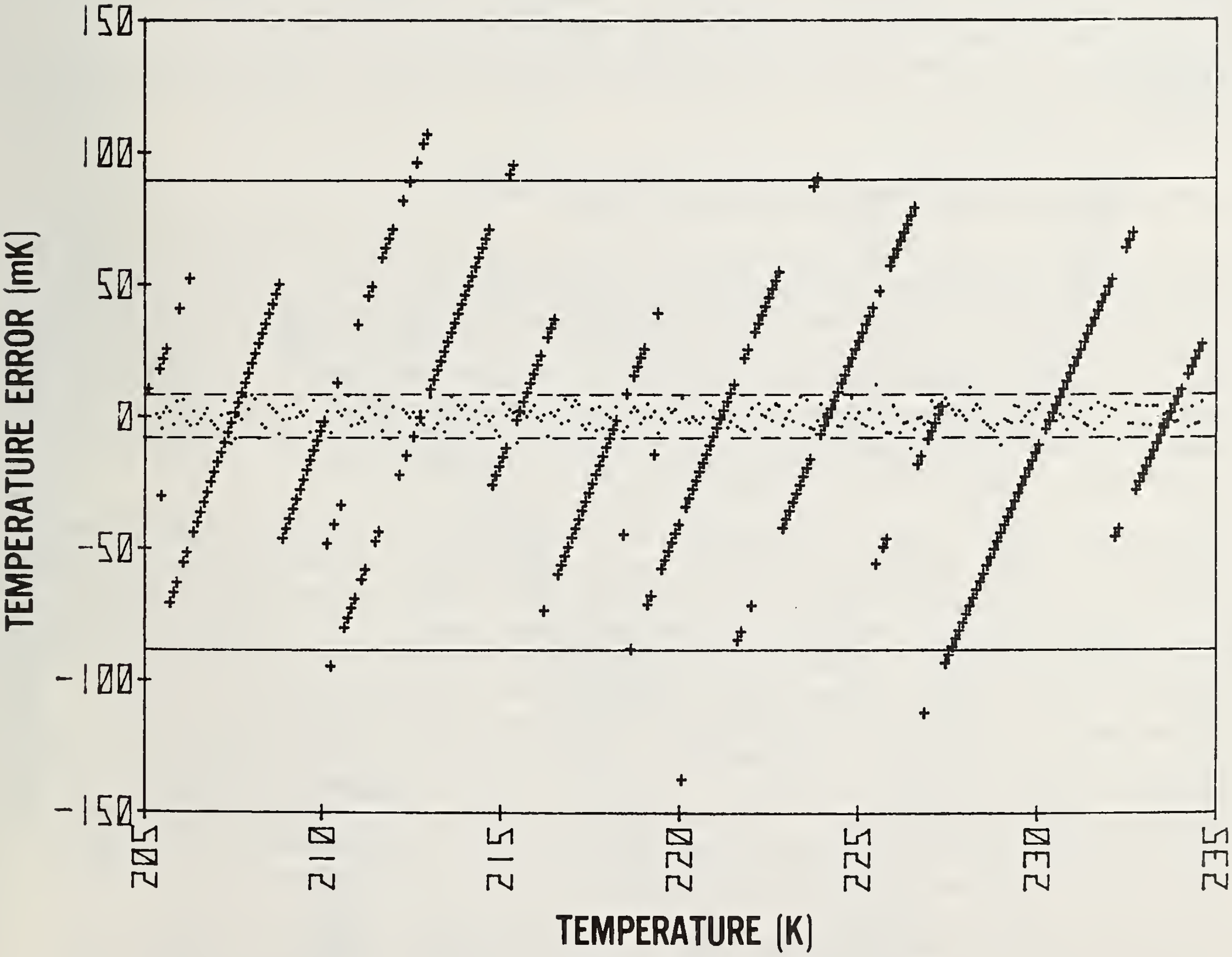

Figure 3-9. Temperature error of the thermocouple temperature, T_{TC}, and the temperature-sensing diode temperature, T_D, from a reference temperature, T_R, derived from a calibrated platinum resistance thermometer by the technique illustrated in figure 3-8. The solid lines and crosses correspond to the thermocouple measurements, and the dashed line and dots are for the diode measurements. The horizontal lines are two-standard-deviation limits of these two sets of data.

of ±23 μV in diode voltage. The crosses show the error $(T_{TC} - T_R)$ of the thermocouple temperature, T_{TC}, and the solid horizontal lines are the two standard deviation limits (±88 mK) of $T_{TC} - T_R$ and correspond to a change of ±3 μV in thermocouple voltage. The thermocouple temperature error plot is seen to be dominated by a systematic 0.1-deg round-off error which would yield, without random instrumentation uncertainties, a two-sigma calculated uncertainty of ±67 mK and accounts for more than half of the observed total mean-square uncertainty of ±88 mK. The temperature-sensing diode voltage is thus much more sensitive to temperature changes and was observed to be much less subject to noise than the thermocouple voltage, but is potentially unstable with time and must be recalibrated before and after each precision use.

3.3.5 Resolution of Peaks in Sulfur-Doped Silicon

Silicon heavily doped with sulfur has four or five energy levels which give a very complex DLTS curve as a function of temperature [3-20]. In recent work, Brotherton *et al.* [3-21] saw five DLTS peaks which were attributed to three types of sulfur donors. In order to detect the presence of weak peaks and to obtain accurate values for the activation energies of peaks with interferences, it is important to be able to enhance or suppress a given peak. This section discusses an approach which is applicable when the two interfering levels have significantly different capture cross sections.

In previous work [3-20], the DLTS curve of wafer 87C (implanted with ^{32}S at a dose of 7×10^{15} cm^{-2}) showed three large DLTS peaks. A shoulder was present on the low temperature side of the largest peak which has an activation energy of about 0.25 eV. No similar shoulders were seen on the corresponding peak of more lightly sulfur-implanted wafers. As part of an effort to obtain capture cross-section values from trap-charging time measurements, DLTS curves were run on wafer 87C for charging times in the range 0.1 to 50 μs. The results are shown in figure 3-10. Because of the large difference in the capture cross sections of the main level and the "shoulder" level, the two peaks are resolved at short charging times. Thus, even though the shoulder level is much lower in density than the main level, it produces the larger peak at the shortest charging time because of its much higher capture rate.

Following up on this approach, DLTS curves were also obtained on a more lightly implanted wafer where no hint of an unresolved peak was seen. The results for wafer 87B, implanted with 10^{15} cm^{-2} ^{32}S, are shown in figure 3-11. It is evident from the systematic shift of the peak position with fill time and the flatness of the curve at the shortest fill time that a second peak is present at about the same temperature as seen in wafer 87C. This suggests that the relative concentration of this sulfur-related level depends upon the implanted dose as both wafers received the same thermal treatments after implantation [3-20]. The midgap sulfur level was measured at the same time as the shallow level for both wafers, and no shifts were seen for that level.

These experiments show that trap-charging time is an effective probe in resolving and detecting closely spaced levels in sulfur-doped silicon and ma' be similarly useful in other situations where overlapping peaks occur.

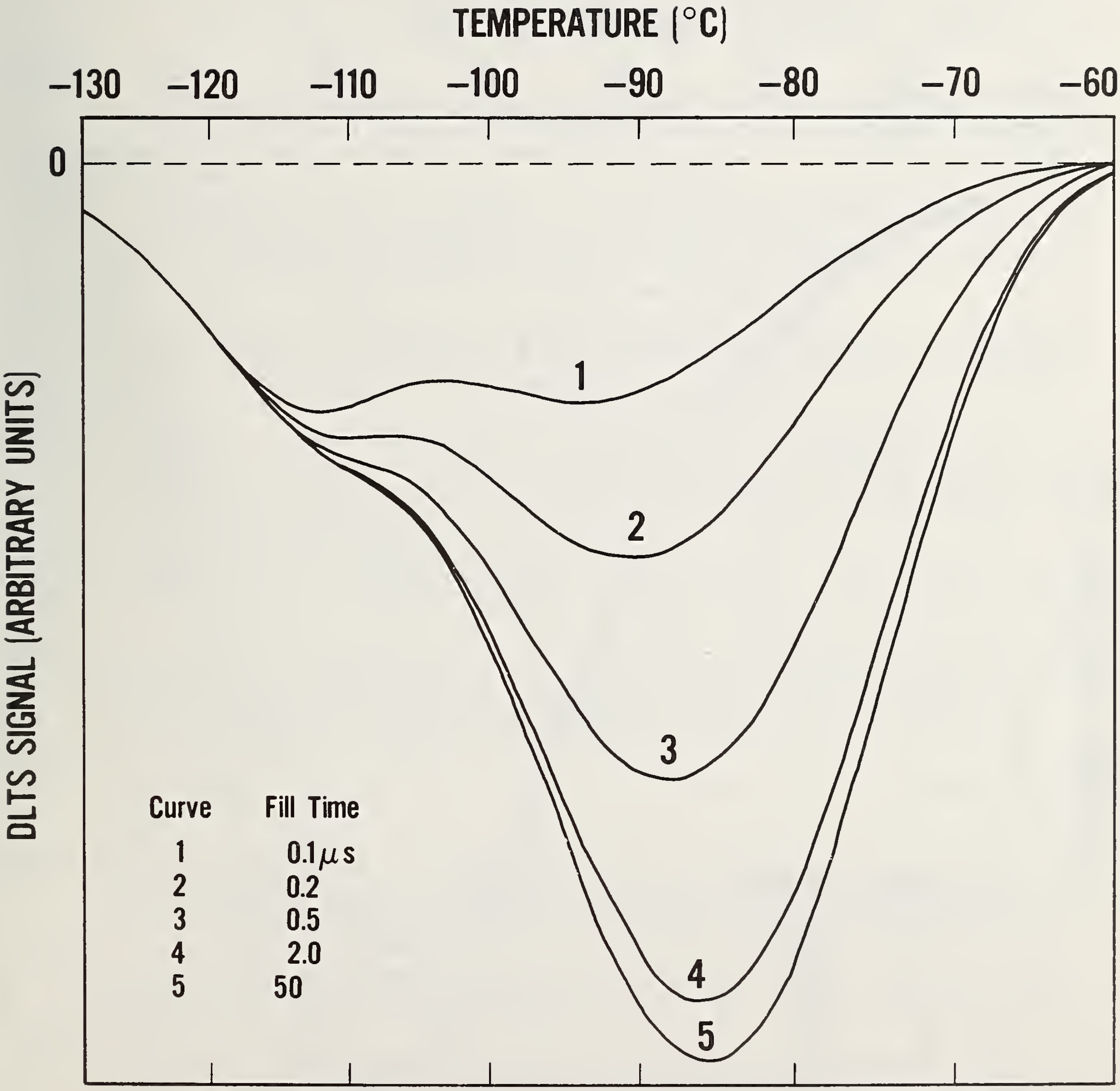

Figure 3-10. DLTS curves for silicon wafer 87C (implanted with ^{32}S to a dose of 7×10^{15} cm^{-2}) with trap charging time as a parameter. The reverse bias was -10 V and the gate delay times were t_1 = 2500 μs and t_2 = 5000 μs. A negative DLTS signal corresponds to majority carrier (electron) emission.

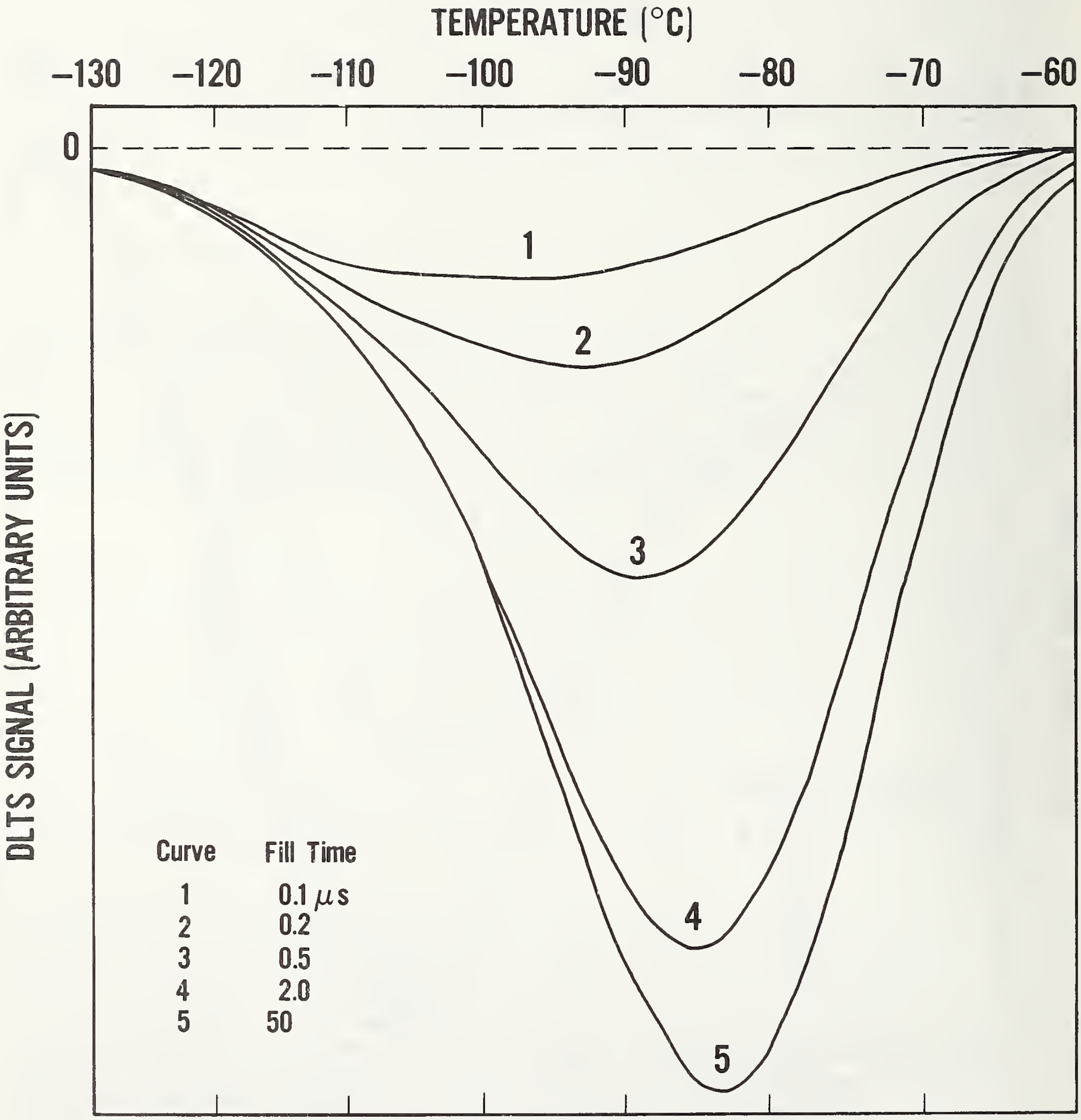

Figure 3-11. DLTS curves for silicon wafer 87B (implanted with ^{32}S to a dose of 10^{15} cm^{-2}) with trap charging time as a parameter. The reverse bias and gate delay times were the same as those used for wafer 87C in figure 3-10. Note that the peak position shifts 10°C with charging times even though two peaks do not appear as for wafer 87C.

REFERENCES

3-1. Watkins, G. D., Negative-U Properties for Point Defects in Silicon, *Proc. Defects in Semiconductors Symp.*, Materials Res. Soc. Annual Meeting, November 16-20, 1980, Boston, Massachusetts, J. Narayan and T. Y. Tan, Eds., (North-Holland, New York, 1981), pp. 21-30.

3-2. Kimerling, L. C., Influence of Deep Traps on the Measurement of Free-Carrier Distributions in Semiconductors by Junction Capacitance Techniques, *J. Appl. Phys.* 45, 1839-1845 (1974).

3-3. Crowell, C. R., and Alipanahi, S., Transient Distortion and nth Order Filtering in Deep Level Transient Spectroscopy (D^nLTS), *Solid-State Electron.* 24, 25-36 (1981).

3-4. Ballard, B., Marchand, I. J., Briot, R., and Grange, G., X-Y Plotter Capacitance Meter Interface for Deep Level Spectroscopy, *J. Phys. E:* 14, 367-372 (1981) and references cited therein.

3-5. Kirchner, P. D., Schaff, W. J., Maracas, G. N., Eastman, L. F., Chappell, T. I., and Ransom, C. M., The Analysis of Exponential and Nonexponential Transients in Deep-Level Transient Spectroscopy, *J. Appl. Phys.* 52, 6462-6470 (1981).

3-6. Lang, D. V., Deep-Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors, *J. Appl. Phys.* 45, 3023-3032 (1974).

3-7. Koyama, R. Y., and Buehler, M. G., Novel Variable-Temperature Chuck for Use in the Detection of Deep Levels in Processed Semiconductor Wafers, *Rev. Sci. Instrum.* 50, 983-987 (1979).

3-8. Larrabee, R. D., Phillips, W. E., and Thurber, W. R., reference [2-1], pp. 8-9.

3-9. White, A. M., Day, B., and Grant, A. J., Influence of Deep Traps on the Measurement of Free-Carrier Distributions in Semiconductors by Junction Capacitance Techniques, *J. Phys. C:* 12, 4833-4838 (1979).

3-10. Chen, J. W., and Milnes, A. G., Energy Levels in Silicon, *Annu. Rev. Mater. Sci.* 10, 157-228 (1980).

3-11. Buehler, M. G., Impurity Centers in PN Junctions Determined from Shifts in the Thermally Stimulated Current and Capacitance Response with Heating Rate, *Solid-State Electron.* 15, 69-79 (1972).

3-12. Shockley, William, The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors, *Bell Sys. Tech. J.* 28, 435-489 (1949).

3-13. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, Nat. Bur. Stand. (U.S.), Spec. Publ. 400-22 (U.S. Department of Commerce/National Bureau of Standards, Washington, D.C., 1976).

3-14. Phillips, W. E., and Buehler, M. G., Semiconductor Measurement Technology: Progress Report, July 1 to September 30, 1976, edited by W. M. Bullis and J. F. Mayo-Wells, Nat. Bur. Stand. (U.S.), Spec. Publ. 400-36 (U.S. Department of Commerce/National Bureau of Standards, Washington, D.C., 1978), pp. 20-22.

3-15. Grimmeiss, H. G., Ledebo, L. A., and Meijer, E., Capture from Free-Carrier Tails in the Depletion Region of Junction Barriers, *Appl. Phys. Lett.* 36, 307-308 (1980).

3-16. Borsuk, J. A., and Swanson, R. M., Capture-Cross-Section Determination by Transient-Current Trap-Filling Experiments, *J. Appl. Phys.* 52, 6704-6712 (1981).

3-17. Larrabee, R. D., Phillips, W. E., and Thurber, W. R., reference [2-1], p. 20.

3-18. Powell, R. L., Hall, W. J., Hyink, C. H., Jr., Sparks, L. L., Burns, G. W., Scroger, M. G., and Plumb, H. H., Thermocouple Reference Tables Based on the IPTS-68, Nat. Bur. Stand. (U.S.), Monogr. 125 (1974).

3-19. Riddle, J. L., Furukawa, G. T., and Plumb, H. H., Platinum Resistance Thermometry, Nat. Bur. Stand. (U.S.), Monogr. 126 (1973).

3-20. Larrabee, R. D., Phillips, W. E., and Thurber, W. R., reference [2-1], pp. 8-19.

3-21. Brotherton, S. D., King, M. J., and Parker, G. J., The Electrical Properties of Sulphur in Silicon, *J. Appl. Phys.* 52, 4649-4658 (1981).

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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. Emphasis is on the development of measurement methods for power-device grade silicon. Major accomplishments during this reporting period were: (1) characterizing by deep level transient spectroscopy (DLTS) the energy levels in silicon power rectifier diodes, (2) writing of a computer program to predict lifetime-related parameters using as input the measured properties of the deep energy levels, (3) developing a novel method to detect nonexponential transients using a conventional double-boxcar DLTS system, (4) analyzing transient capacitance measurements to extend the techniques to nonexponential decays, (5) using a platinum resistance thermometer to calibrate temperature sensing diodes to obtain the precision needed for careful isothermal capacitance measurements, and (6) utilizing trap changing time as a technique to resolve overlapping DLTS peaks in sulfur-doped silicon.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

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