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Production-Compatible Microelectronic Test Structures for the Measurement of Interface State Density and Neutral Trap Density

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
National Engineering Laboratory
Center for Electronics and Electrical Engineering
Semiconductor Devices and Circuits Division
Washington, DC 20234

January 1982

Prepared for
Air Force Wright Aeronautical Laboratories
Wright-Patterson AFB, OH 45433

and

Naval Air Systems Command
Arlington, VA 20360

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T. J. Russell

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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Production-Compatible Microelectronic Test Structures for the Measurement of Interface State Density and Neutral Trap Density

by

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Abstract

Interface states and oxide neutral traps are defects in metal-oxide-semiconductor (MOS) structures which adversely affect the operation of integrated circuits (ICs). For very large scale integration (VLSI), the advanced techniques which are used to fabricate circuits with devices of submicrometer geometries expose the devices to ionizing radiation which can create these defects or alter the number of defects and their charge state and thus modify device operating characteristics. The physical identities of the defects which trap charge at the interface and in the bulk oxide are not well established. This means that one cannot *a priori* predict the behavior of the defects to a stress or fabrication process. Thus, it is desirable that the density of these defects be monitored routinely and that the measurement method used be easy to perform and fast and that it provide unambiguous results and be compatible with a production environment. The purpose of this study is to identify production-compatible measurement methods which can be used for routine measurement of neutral trap density and interface trapped charge. This study reviews the application of existing methods for quantifying the number of these defects. Methods determined to be most appropriate for the stated purpose are discussed in detail.

Key words: avalanche injection; capacitance-voltage curves; charge injection; charge pumping; gated diodes; interface states; metal-oxide-semiconductor devices; microelectronic test structures; MOSFETs; neutral traps; oxide-semiconductor interface; test structures.

1. INTRODUCTION

The presence of oxide/semiconductor interface trapped charge, oxide trapped charge, oxide fixed charge, mobile oxide charge, and the spatial nonuniformity of physical parameters of the oxide or the semiconductor can adversely affect the operation of metal-oxide-semiconductor (MOS) devices and can lead to the failure of MOS integrated circuits (ICs). Traditionally, these imperfections were of interest principally when the ICs were required to operate in a radiation environment, since ionizing radiation can produce defects and can create free carriers to charge them [1-3]. For very large scale integration (VLSI), the advanced techniques [4-6] which are used to fabricate cir-

cuits with devices of submicrometer geometries make use of electron and ion beams, x-rays, and plasmas; thus, the effect of radiation on the number and charge state of these defects must be considered [7-12]. An additional problem arises because the devices will operate with large internal electric fields which result from the use of thinner oxides required to scale submicrometer devices. MOS device operation under high field conditions may result in the injection into the oxide of energetic or "hot" carriers [13-16]. The exposure of devices to ionizing radiation and operation at high electric fields can alter the number of defects and can change the charge state of the defects and modify the device operating characteristics.

The physical identities of the defects which trap charge at the interface and in the bulk oxide are not well established. This means that one cannot *a priori* predict the behavior of the defects to a stress or to a fabrication process change. The density of these defects should be monitored routinely. Thus, it is desirable that the measurement method used to quantify the presence of the traps be easy to perform and fast and that it provide unambiguous results and be compatible with a production environment.

Microelectronic test structures for computer-automated electrical measurements [17] are appropriate for this measurement problem. Test structures are microelectronic devices fabricated by the same design rules and by the same process used to fabricate ICs. They are used to measure selected material [18,19], process [20-28], and device [28] properties and to evaluate semiconductor equipment performance [29-34] by means of computer-controlled electrical tests [35].

The purpose of this study is to identify production-compatible measurement methods which can be used for routine measurement of neutral trap density and interface trapped charge. In-depth discussion of the physical nature of the defects is not a goal of this study. This study emphasizes the application of existing measurement methods for quantifying the number of neutral traps and interface states, but these measurement methods also can be applied to the detection and quantification of oxide trapped charge, oxide fixed charge, and mobile ionic charge. Methods determined to be the most appropriate for this purpose are discussed in detail. However, other measurement methods for quantifying the number of these defects will be mentioned, referenced, and briefly discussed. There are excellent review papers on the measurement of interface states on semiconductor/insulator surfaces by Goetzberger *et al.* [36] and DeClerck [37] and a review of the defects and impurities in thermally grown silicon dioxide by DiMaria [38]. These reviews provide additional references to the literature on the identity of these defects. In addition, the Proceedings of the American Physical Society Topical Conferences on "The Physics of MOS Insulators" [39] and "The Physics of SiO_2 and Its Insulators" [40] which were held in 1980 and 1978, respectively, are excellent resources for information on these topics.

2. THE METAL-OXIDE-SEMICONDUCTOR STRUCTURE

The different charges which alter the electrical behavior of an MOS structure and the names recommended by Deal *et al.* [41] are illustrated using an energy band diagram in figure 1. Interface trapped charge is physically located at

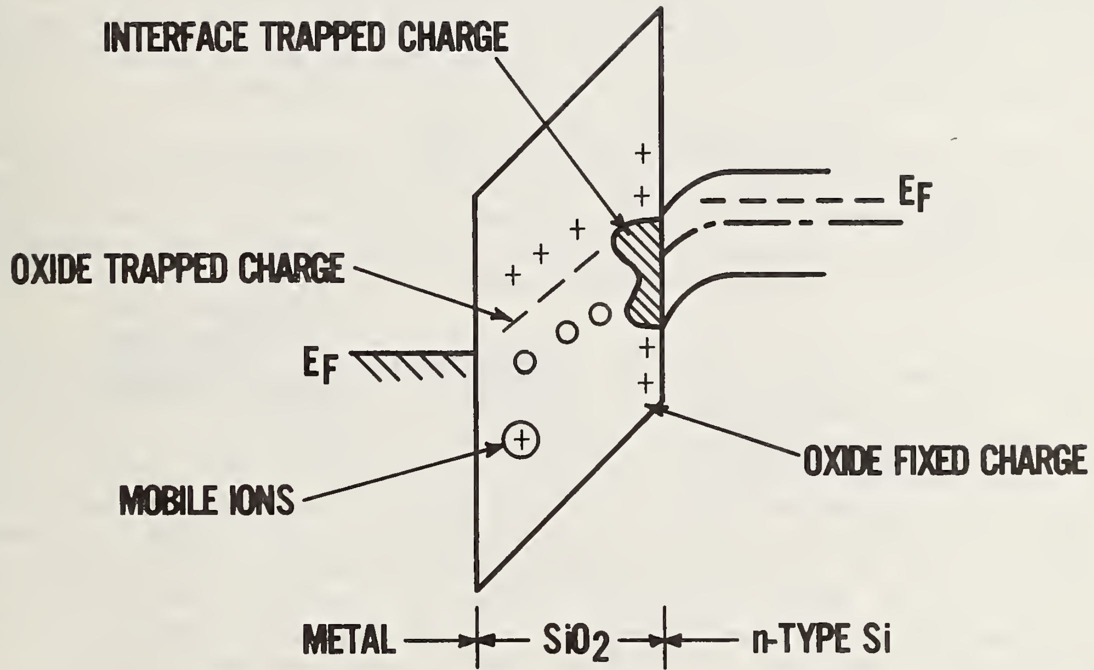


Figure 1. Energy band diagram of an MOS system showing the names and location of charges.

the silicon dioxide/silicon interface. The trap energies are distributed across the band gap of silicon. As the bias across an MOS structure is changed, these states readily exchange charge with the semiconductor. They may be *n*- or *p*-type states. The number per square centimeter is designated as N_{it}. Oxide-trapped charge is related to defects in the silicon dioxide and resides on states energetically within the oxide band gap. The defects can be coulombic [38] and trap either positive or negative charge or can be neutral [38]. Neutral traps can be detected by electrical techniques only after free carriers have been introduced into the oxide to populate the traps. The number of states per square centimeter is designated as N_{ot}. Mobile ionic charge [42-43] and oxide fixed charge [42-43] also cause deviations from ideal behavior in MOS structures. Mobile ionic charge, N_m, is due to ionic impurities in the oxide; generally, these impurities are mobile only at elevated temperatures. Oxide-fixed charge, N_f, is positive and is related to the details of the process by which the oxide was grown.

The term lateral nonuniformity (LNU) is used to represent the spatial variations of the oxide charge or trap parameters, including the interface trapped charge, oxide trapped charge, oxide fixed charge [44-51], and mobile ionic charge [52-54]. Lateral nonuniformities may also result from nonuniform oxide thickness or substrate dopant density [55].

To illustrate the effects charged oxide and interface defects have on the behavior of MOS devices, consider what happens to the MOS capacitor in figure 2 when a positive gate voltage with respect to the substrate is applied to the metal gate. The structure forming the MOS capacitor is a metal gate on a silicon dioxide layer on an *n*-type silicon substrate. When positive gate voltage with respect to the substrate is applied, majority carriers, electrons, are accumulated at the silicon dioxide/silicon interface as shown in figure 2a. If the applied gate voltage is made negative, the electrons are forced away from this interface and a depletion region is formed (fig. 2b). If a large enough negative voltage is applied, the bands bend past the intrinsic Fermi level and the surface is said to be inverted (fig. 2c). (This behavior is considered in more detail by Grove [56] and Sze [57].)

For negative gate voltages smaller than that required to invert the semiconductor surface, the applied gate voltage, V_G, appears as a voltage across the oxide, V_{ox}, and as a potential at the surface of the semiconductor, ψ_{Si}. Thus,

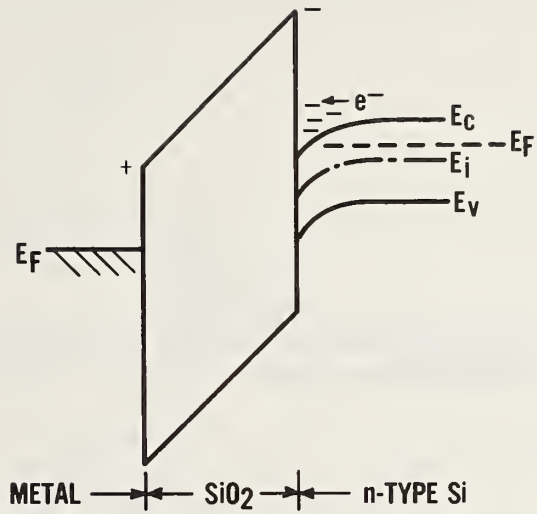
$$V_G = V_{ox} + \psi_{Si} \; . \tag{1}$$

In the absence of any oxide fixed or trapped charge, mobile charge and any interface trapped charge, eq (1) can be written as

$$V_G = -\frac{Q_{Si}}{C_{ox}} + \psi_{Si} \; , \tag{2}$$

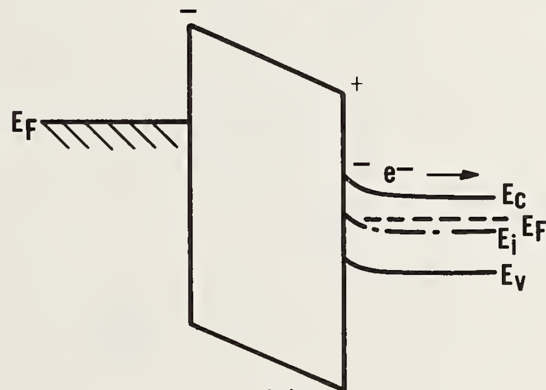
where Q_{Si} is the charge per unit area contained in the semiconductor surface depletion region and C_{ox} is the gate oxide capacitance. If a small change in the voltage is applied to the metal gate of the system, any change

MAJORITY CARRIERS ACCUMULATED AT SiO_2/Si INTERFACE



2 (a)

SiO_2/Si INTERFACE DEPLETED OF MAJORITY CARRIERS



2 (b)

INVERTED SiO_2/Si INTERFACE

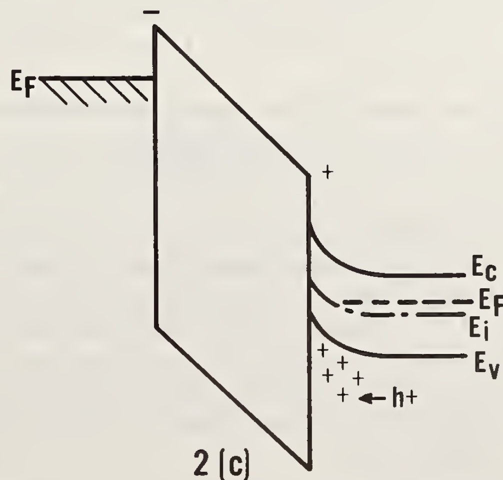


Figure 2. Energy band diagram of an MOS (*n*-type silicon) in (a) accumulation, (b) depletion, and (c) inversion.

in gate charge, dQ_G, will induce an equal but opposite change in the charge, dQ_{Si}, in the silicon surface depletion region and can be written as

$$dQ_G = - dQ_{Si} \ , \tag{3}$$

and

$$C = \frac{dQ_G}{dV_G} = - \frac{dQ_{Si}}{dV_G} \ , \tag{4}$$

where C is the total capacitance of the MOS system. Using eq (2), the capacitance can be written as

$$C = \frac{-dQ_{Si}}{-\dfrac{dQ_{Si}}{C_{ox}} + d\psi_{Si}} \tag{5}$$

or

$$C = \frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_{Si}}} \ , \tag{6}$$

where

$$C_{Si} = - \frac{d\psi_{Si}}{dQ_{Si}} \tag{7}$$

is the capacitance of the silicon space charge region. Thus the capacitance of an ideal MOS system when a space charge region exists is the oxide capacitance in series with the depletion layer capacitance.

In the above, it was assumed that any small change in the charge on the metal gate resulted in a small change in the charge at the edge of the depletion width. This is true only when the silicon surface is depleted. When the surface is inverted, it is true only at high frequencies where the recombination generation of minority carriers cannot keep up with the small gate voltage variation. The resulting capacitance *versus* voltage (C-V) curve is represented in figure 3 by the curve labeled "high frequency." At low frequency, when the minority carrier recombination-generation rate is greater than the signal frequency, the charge in the inversion layer can change quickly enough to keep up with the small gate voltage variation. Now, the measured capacitance in inversion is just that of the oxide and in figure 3 the curve is labeled "low frequency."

The deviations in the ideal MOS capacitor C-V curve caused by interface trapped charge and oxide trapped charge, or lateral nonuniformity of oxide trapped charge are illustrated in figure 4. Curve A in figure 4 is the

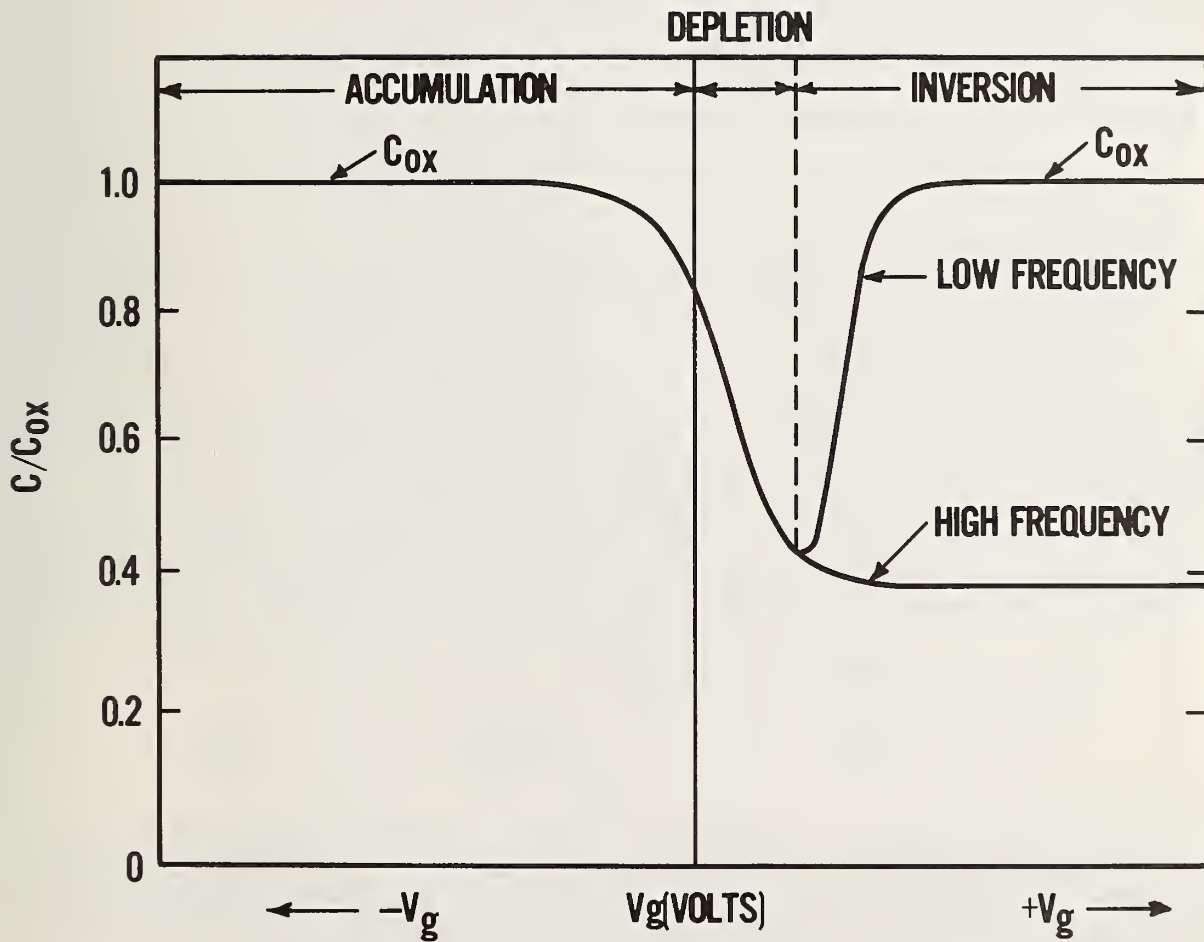


Figure 3. Capacitance *versus* gate voltage (V_g) curve, C-V for an MOS (*p*-type silicon) system. The portion of the curves where the silicon surface is accumulated, depleted, and inverted and the high and low frequency measurements are shown.

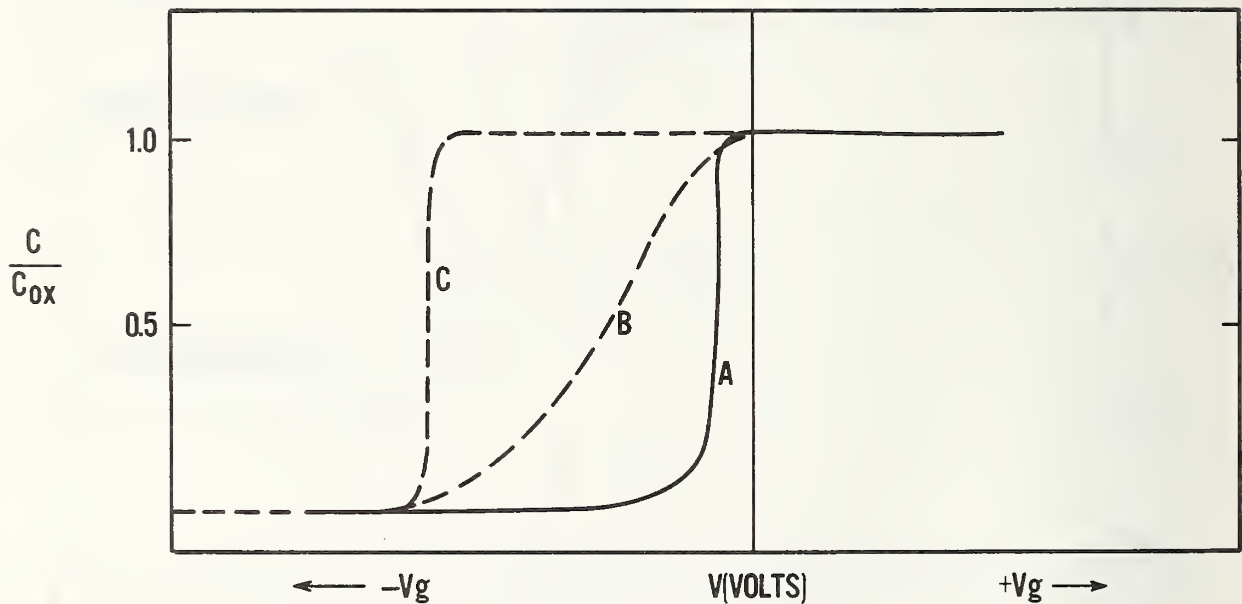


Figure 4. The C-V curves for (A) an ideal MOS (n-type silicon) system with interface trapped charge or laterally nonuniform oxide trapped charge, which (B) causes the curve to "stretch out," and (C) an MOS system with positive oxide trapped charge which causes the curve to be shifted to the left of the ideal curve.

"ideal." The "stretch out" of curve B can result from either interface trapped charge or a nonuniform charge in the oxide under the metal gate [57]. As the applied gate voltage is changed to a more negative value, the Fermi level is swept across the silicon band gap causing the interface states to alter their charge state. This appears as a variable capacitor in series with the oxide capacitance and in parallel with the depletion capacitance. The "stretch out" can also result if there are regions which have different amounts of oxide trapped charge and can be thought of as a number of different capacitors connected in parallel with the semiconductor depletion capacitance, C_{Si}, and in series with the oxide capacitance, C_{ox}. If one were able to measure the C-V curve of each capacitor separately, each would be displaced from zero voltage by a different amount depending on the amount of oxide charge. But the capacitors are measured simultaneously; thus, the total capacitance is the sum of the capacitors in parallel, and the result is a stretched-out C-V curve.

Oxide fixed charge, trapped charge, and mobile charge alter the ideal C-V curve by causing it to shift to a more positive or a negative value depending on whether net oxide charge is negative or positive. When the metal and semiconductor of an MOS structure are connected together, electrons flow from the metal to the semiconductor until equilibrium is reached. The Fermi level in the metal and in the semiconductor are lined up, but there will be an electrostatic potential difference between the two regions, and the energy bands in the semiconductor are bent close to the surface. In the ideal case, i.e., no oxide fixed, trapped, or mobile charge, the amount of band bending is given by the work function difference between the metal gate and the semiconductor, ϕ_{MS}. The gate voltage required to counteract the electrostatic potential difference and make the bands flat again is called the flat band voltage, V_{FB}. If there is charge in the oxide, for example, oxide trapped charge, then the flatband voltage is given by

$$V_{FB} = \phi_{MS} - \frac{1}{C_{ox}} \int_{o}^{x_o} \frac{x}{x_o} N_{ot}(x)\, dx \ . \qquad (8)$$

In this expression, the metal-semiconductor work function difference is ϕ_{MS}, the oxide capacitance per unit area is C_{ox}, the thickness of the oxide is x_o, and the centroid of the oxide trapped charge is x and its distribution is N_{ot}. The second term in this expression accounts for the additional oxide trapped charge and means that V_{FB} depends not only on the magnitude of oxide trapped charge, but also on its location within the oxide. If N_{ot} is a discrete layer of charge, it will have a minimum effect on the flat-band voltage when it is located at the metal-oxide interface and a maximum effect when located at the oxide/silicon interface. Since the charge location and magnitude are not usually known, the term $(x/x_o)N_{ot}$ is sometimes replaced by the effective density, N_{eff}, at the oxide/silicon interface. The effective oxide trapped charge density, N_{eff}, and the actual oxide charge density are related by the expression

$$N_{eff} = \frac{x}{x_o} N_{ot} . \quad (9)$$

The presence of positive or negative interface or oxide trapped charge causes V_{FB} to be shifted from its ideal value in the negative or positive direction, respectively. (The curve shifts in a direction opposite to the sign of charge trapped in the oxide.) A shift in the C-V curve to a more negative flat band voltage is illustrated in figure 4 by curve C. This shift is consistent with trapped positive charge.

Using the shift in flat-band voltage, ΔV_{FB}, and eq (8) and assuming that this trapped oxide charge is uniformly distributed across the oxide, it can be shown that the net amount of oxide trapped charge (number of charges per square centimeter) is given by the following expression

$$N_{ot} = \frac{C_{ox} \Delta V_{FB}}{2q} . \quad (10)$$

3. THE DETECTION OF NEUTRAL TRAPS

Although silicon dioxide (SiO_2) is considered here to be amorphous, short range order is generally preserved; silicon atoms are tetrahedrally bonded to the oxygen atoms as in crystalline SiO_2, but the bond angles are slightly different from the crystalline case. This distorted lattice and the possible stoichiometric variations are the basis of the coulombic and neutral traps. Unlike the coulombic oxide traps, until a charge is in a neutral trap in the gate oxide of an MOS system, its presence is not detected by electrical C-V techniques. If the MOS system is part of a MOSFET, this trapped charge causes the threshold voltage (the on/off voltage of the transistor) to change and thus alters circuit operating characteristics.

To study the neutral traps electrically, free charge carriers must be created in the oxide or introduced into the oxide to charge the traps. To create free carriers in the oxide, ionizing radiation with energy greater than the band gap energy (>9 eV) of silicon dioxide can be used. The radiation creates electrons and holes which can occupy the neutral traps. Radiation which has been used includes gamma radiation or x-rays [58-62], electrons [62-67], and vacuum ultraviolet (VUV) and ultraviolet (UV) light [68-71]. However, irradiation of wafers is not currently amenable to production-compatible automated wafer level measurements for a variety of reasons such as size, complexity, and cost of equipment required.

Alternately, strong electric fields can be used to introduce carriers into the oxide. The high fields cause the semiconductor surface to be in deep depletion or strong accumulation. Enough energy is imparted to either minority carriers or majority charge carriers for them to either surmount the energy barrier at the silicon dioxide-silicon interface or tunnel through this barrier. These charge carriers can then occupy the trapping site or can create hole-electron pairs in the oxide by impact ionization and the additional carriers can be trapped. Electric field-induced carrier injection is attractive for automated measurement.

One high electric field technique is avalanche injection [72-83]. To avalanche inject charge into the oxide of an MOS capacitor, the capacitor must be pulsed into deep depletion. The minority carriers are accelerated toward the oxide/silicon interface by the electric field which results from the applied gate voltage. If the amplitude of the gate voltage pulse is large enough and the mean free path of the carrier is long enough, then avalanche multiplication of charge carriers occurs in the depletion region of the silicon substrate. If the kinetic energy of the resulting "hot" carriers is sufficient, some of the carriers overcome the energy barrier at the oxide/silicon interface (3.25 eV) and are injected into the oxide. Some of these carriers are then trapped at defects in the oxide and their presence detected [84] using conventional electrical C-V techniques.

The energy band diagram of an MOS structure in figure 5 illustrates the mechanism of strong electric field avalanche injection of minority carriers, "hot" electrons, from a *p*-type silicon substrate. This phenomenon was treated [76,85-88] using first order kinetics to derive the trapping parameters from the change in the flat-band voltage, ΔV_{FB}, for a constant avalanche injection current, j_{inj}. The evolution of flat-band voltage as a function of time, t, is given by the expression

$$\Delta V_{FB}(t) = \frac{q\, N_{eff}}{C_{ox}} \left[1 - \exp - \left(\frac{\sigma_c\, j_{inj}\, t}{q} \right) \right]. \tag{11}$$

In this expression q is the electronic charge, C_{ox} is the oxide capacitance per unit area, σ_c is the capture cross section of oxide traps, and N_{eff} is the effective density of oxide traps at the silicon-silicon dioxide surface. The natural logarithm of the time derivative of this equation results in a linear equation:

$$\ell n \frac{d}{dt} \Delta V_{fb}(t) = \ell n \left[\frac{N_{eff}}{C_{ox}} \sigma_c\, j_{inj} \right] - \frac{\sigma_c\, j_{inj}}{q}\, t\ . \tag{12}$$

If the experimental values of the right side of eq (12) are plotted *versus* time, the effective density of oxide traps is the y-axis intercept of the straight line and their capture cross section is the slope of the line.

To illustrate the measurement method, the technique was implemented using an MOS capacitor test structure from the NBS-4 test pattern [89]. The capacitor was delineated on a *p*-type, 0.3-Ω•cm silicon substrate with a (111) orientation. The nominal gate oxide thickness was 0.1 μm and the nominal area of the gate was 1.14×10^{-3} cm^2. The circuit used is illustrated in figure 6. With the switches in position A, carriers were avalanche injected into the oxide using a 60-V 10-kHz square wave which created a 6×10^6 V/cm electric field strength at the silicon surface. Inset 7a in figure 7 shows that the C-V curve shifted to more positive values after each period of avalanche injection. This shift is consistent with trapped negative charge. The C-V curve is obtained with the switches in position B in figure 6. Using the analysis technique described earlier, the V_{FB} *versus* t data (inset 7b) are best fit by two straight lines, shown in figure 7c, indicating two types

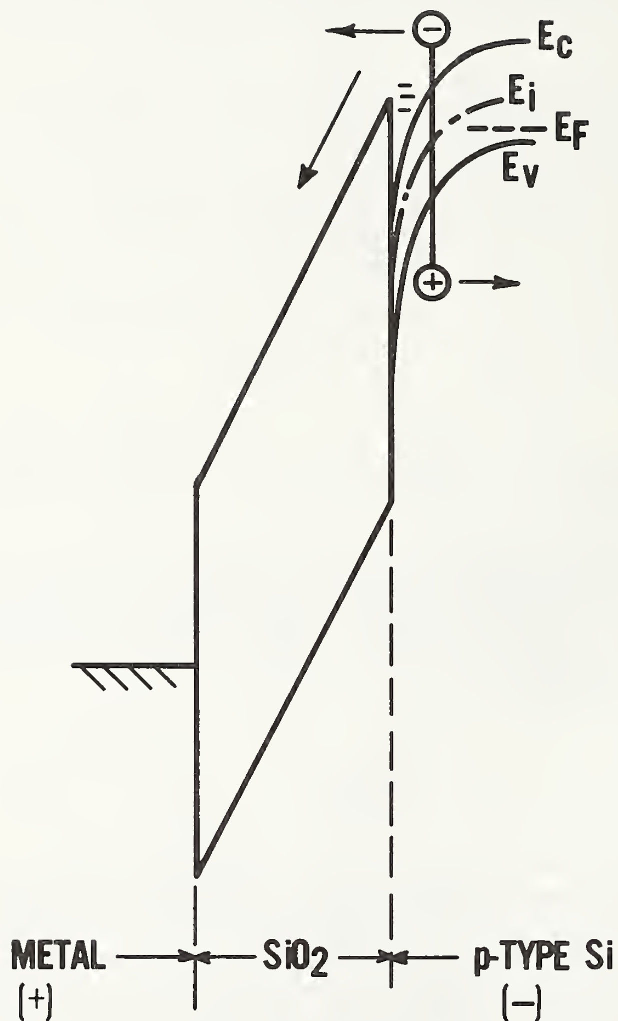


Figure 5. Energy band diagram illustrating avalanche injection of electrons from *p*-type silicon.

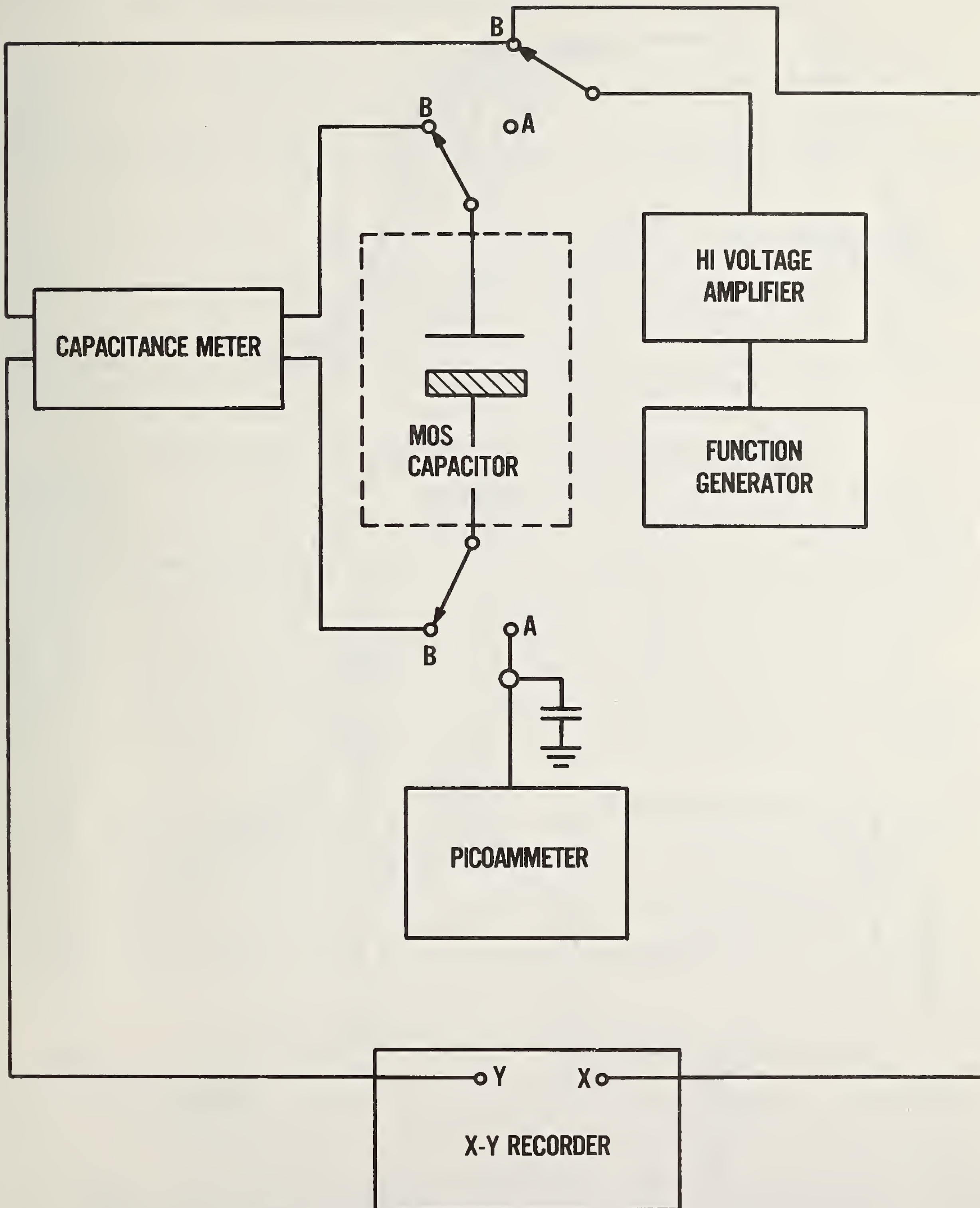
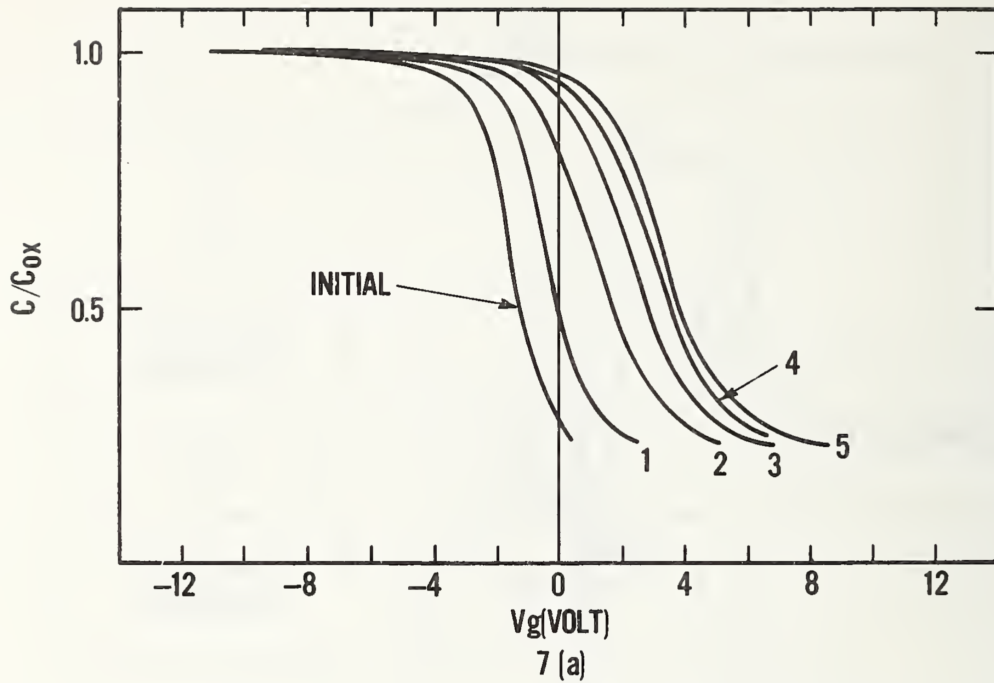
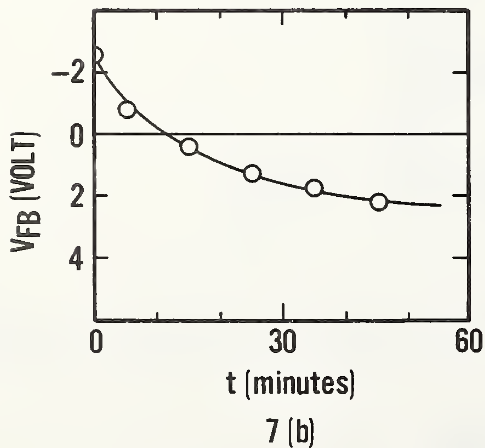


Figure 6. Block diagram of a circuit used for C-V, I-V, and high field injection experiments.





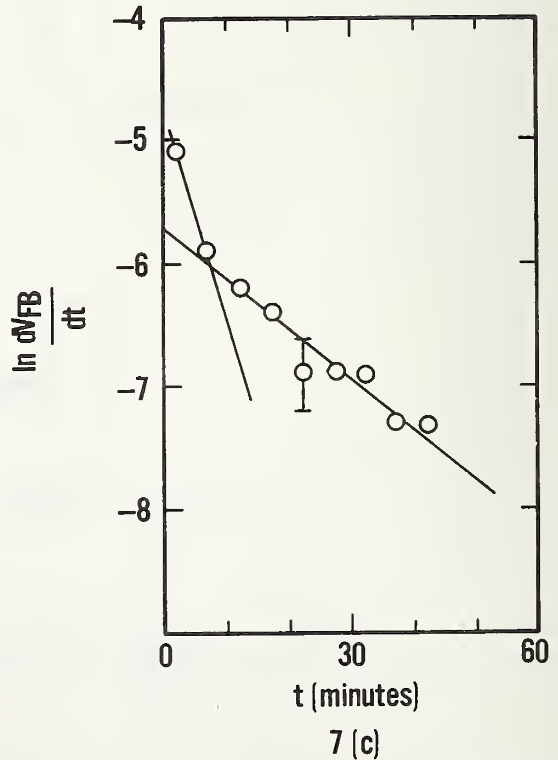


Figure 7. Display of data after avalanche injection of electrons. (a) C-V curve shift from left to right. (b) illustration of shift in V_{FB} *versus* time. (c) $\ell n(dV_{FB}/dt)$ *versus* t plotted and used to calculate capture cross section of neutral traps. The two straight lines indicate that there are two sets of traps with different capture cross sections.

of traps with capture cross sections of 1.36×10^{-17} cm^2 and 1.62×10^{-17} cm^2 and densities 1×10^{12} cm^{-2} and 6.27×10^{11} cm^{-2}, respectively.

A limitation of the avalance injection technique is the need for the large electric field necessary to cause avalanching in the silicon depletion region. For a given gate voltage, the magnitude of the electric field in the depletion region is related to the resistivity of the silicon. In this study, the range of resistivities over which the avalanche injection of electrons from p-type substrates is practical was not determined.

Hole injection from a p-type silicon substrate is more complicated. The negative voltage pulse that must be applied to the gate of an MOS capacitor causes holes to avalanche in the silicon depletion region, as shown in figure 8, and to be injected into the oxide. However, the probability is almost equal that electrons tunnel from the aluminum gate into the oxide. These electrons may then recombine with the injected holes so that no net change in the oxide trapped charge is detected. It has been reported [89] that a triangular waveform for the voltage pulse overcomes this problem.

Another high electric field technique [90,91] for injecting charge into the gate oxide of an MOS structure, called Field-Induced Injection by Impact Ionization (F4I), is illustrated in figure 9. Instead of using high voltage to inject minority carriers from the depletion region in the semiconductor into the oxide, the electric field created by the gate voltage increases the probability that majority carrier electrons tunnel from the n-type substrate into the oxide via a Fowler-Nordheim mechanism. Some of the injected electrons create electron-hole pairs in the oxide by impact ionization. The applied gate voltage separates the electron-hole pairs. The very mobile [58,59] electrons are swept toward the metal gate where they are removed from the oxide; the less mobile [61] holes are swept toward the silicon substrate where some fraction is trapped [68] near the silicon diode/silicon interface.

An MOS capacitor on a 0.1-Ω•cm n-type silicon substrate with a 0.095-μm thick oxide was used to demonstrate the field-induced injection by impact ionization technique. A positive gate-to-substrate pulse amplitude of 90 V and duration of 150 ms was used, resulting in electric field strengths in the oxide of 9×10^6 V/cm. After four such pulses, figure 10 shows that the V_{FB} has shifted from an initial value of -0.8 V to a final value of -2.0 V. This negative shift in the flat-band voltage is consistent with trapped positive charge.

4. THE DETECTION OF INTERFACE TRAPPED CHARGE

The transition region of vitreous silicon dioxide thermally grown on crystalline silicon contains defects which can trap electrical charge. Energetically, these interface states are distributed across the band gap of the semiconductor. At the present, their exact physical identity is not established, but they may be related to unsatisfied bonds in this region [92] or to strain due to the lattice mismatch between silicon dioxide and silicon [93]. In an n-type MOS structure, if an applied bias is smoothly varied such that the silicon surface is swept from accumulation to inversion, the Fermi level moves across the silicon band gap. As this happens, donor-like interface states emit electrons to become positively charged, and acceptor-like inter-

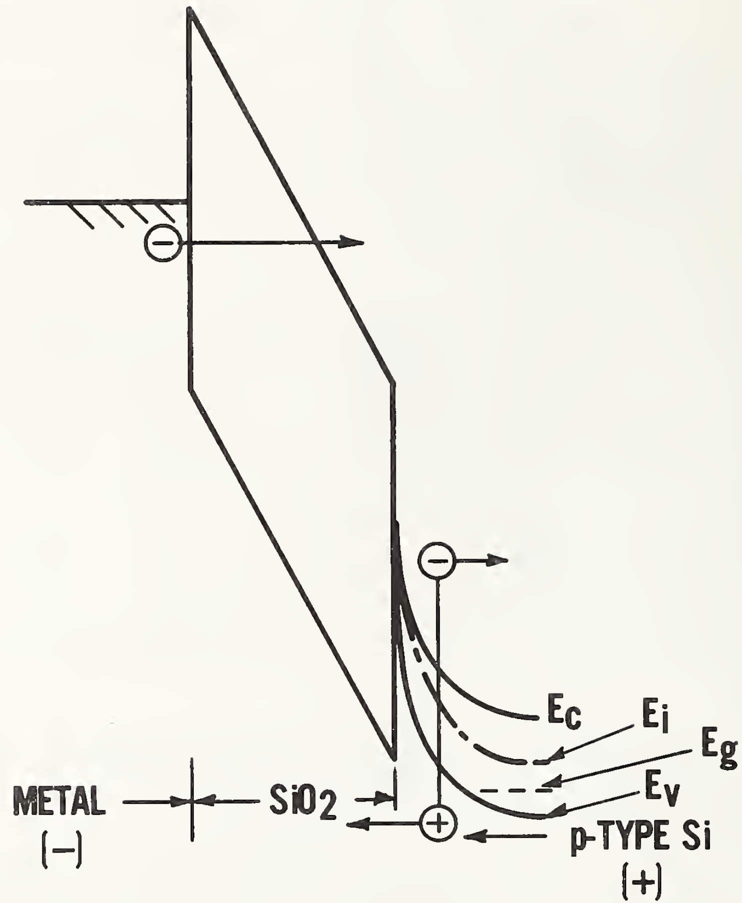


Figure 8. Energy band diagram illustrating hole injection from *p*-type silicon. It is almost equally probable that electrons can be injected from the gate metal and that they may recombine with the injected holes.

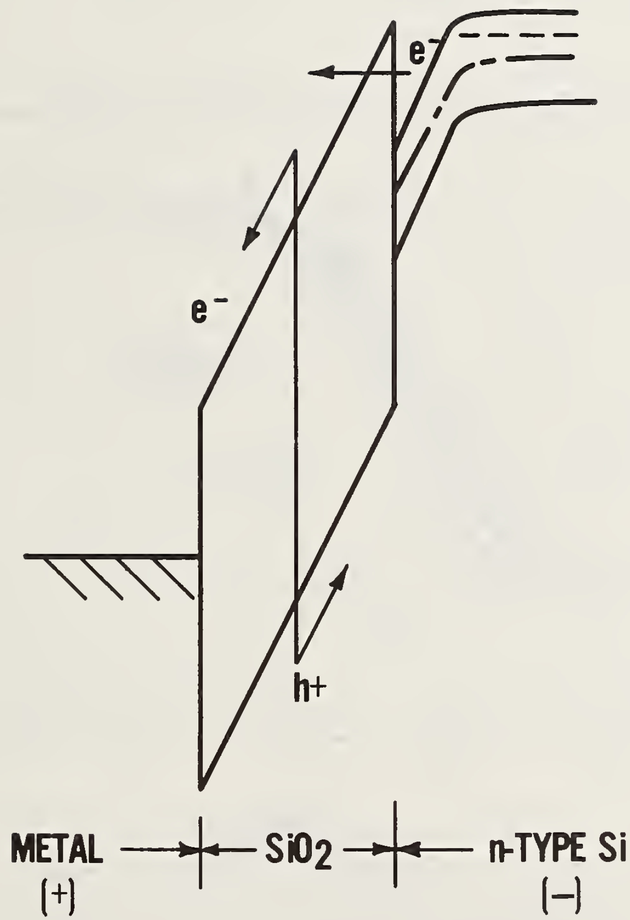


Figure 9. Energy band diagram illustrating field-induced injection by impact ionization (F4I).

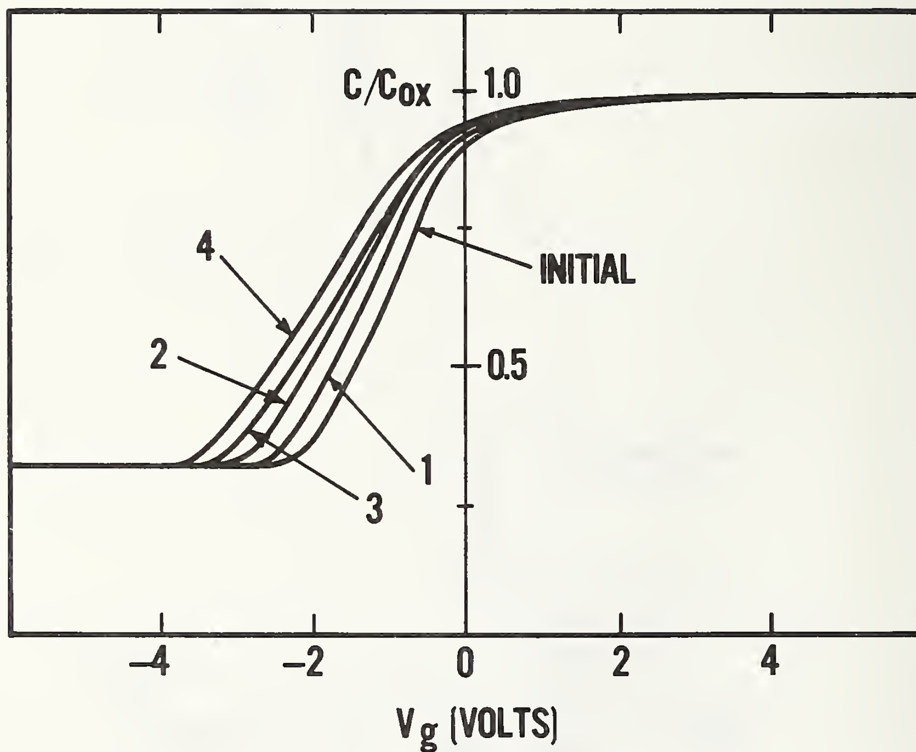


Figure 10. C-V curve after four F4I pulses. The shift of the curve is from right to left.

face states capture holes to become neutral. Both types of states may be present in the same structure [94]. In a MOSFET, the result of increasing interface trapped charge is a threshold voltage shift and a reduced switching speed. In surface channel charge-coupled devices (CCDs), the result is lower charge transfer efficiency (CTE).

A number of techniques involving the use of MOS structures have been proposed to determine the amount of interface trapped charge. One technique suggested by Terman [95] is to compare the theoretical and measured high frequency C-V curves. The difference in the two curves is proportional to interface trapped charge density. A shortcoming of this technique is that the measured C-V curve can be distorted by defects other than interface trapped charge, as explained earlier (sec. 2). For the Gray-Brown technique [96], an MOS structure is cooled to near liquid nitrogen temperature, and the high-frequency C-V curve is measured for comparison to the room temperature C-V curve. At low temperatures the high frequency C-V curve will be shifted in voltage because at low temperatures the Fermi level is shifted toward the majority carrier band edge. A disadvantage of this measurement method is that only interface states with energies in a narrow region within the band gap near the Fermi level are measured. The technique of Nicollian and Goetzberger [97,98] is probably the most sensitive of the measurement methods for interface state density. It involves the measurements of capacitance and conductance *versus* bias voltage at different frequencies. The number of measurements that are required makes this technique very tedious. Another measurement method for interface state density is the quasi-static technique [99]. The essence of this technique is that the charging current of an MOS capacitor test structure is measured in response to a linear voltage ramp and the resulting curve compared to the result calculated for an ideal structure with no interface trapped charge. Roitman [46] has demonstrated how this technique can be implemented using a computer to assist in measurements and on-line computation, but this technique is also slow. In fact, none of these methods is particularly attractive for application as a routine measurement technique to be used on a wafer prober for high-speed data accumulation and analysis in a production environment.

However, a charge-pumping method introduced by Brugler and Jespers [100] and more recently examined in greater depth by Elliot [101] and Backensto [102-104] is an interface trapped charge measurement method that is attractive for use with microelectronic test structure techniques. Consider the cross section of a *p*-channel MOSFET in the left column of figure 11a. The source and drain are connected together and reverse biased. When the gate voltage is greater than zero such that the *n*-type silicon surface is accumulated, the interface states are neutral if they are donor-like as illustrated by the energy band diagram in the right column in figure 11a. Under this condition, the current measured in the external circuit is just the junction reverse-bias leakage current I_L which appears as a negative current when measured in an external circuit between substrate and ground, as shown at left in figure 11a. The areas of the MOSFET marked with diagonal lines in the left column of figure 11 represent the depletion region of the transistor for the voltage levels of the square waves shown in the center column of the figure. The gate voltage is repetitively pulsed from accumulation to inversion and back to accumulation, figure 11c; a "charge-pumping current" whose sign is opposite the sign of the reverse-bias leakage current appears in the external

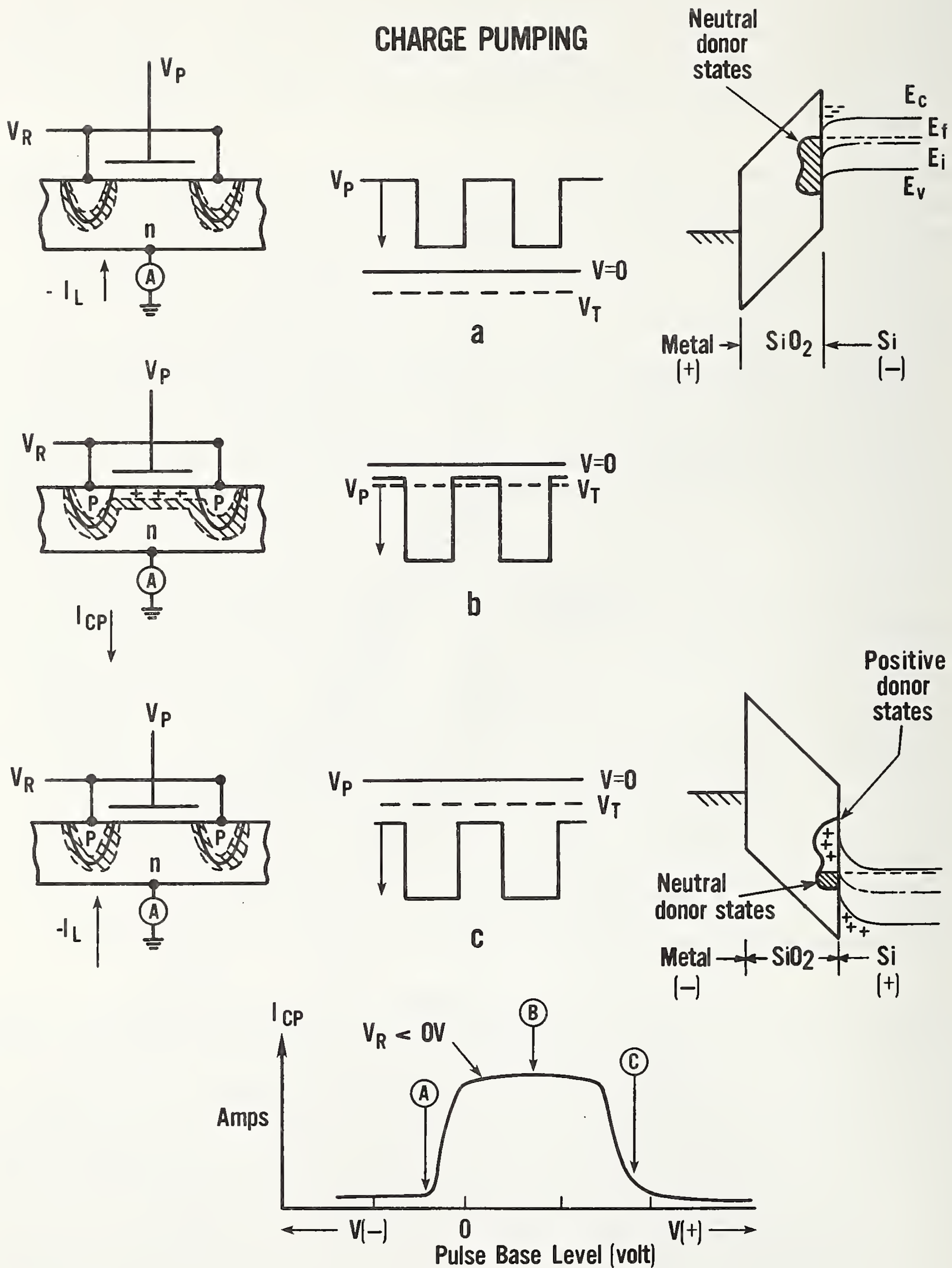


Figure 11. Charge pumping. The left column is a cross-sectional view of a MOSFET with its source and drain connected together and reverse biased. The diagonally shaded area illustrates how the depletion region changes as the voltage pulse level is changed, as illustrated in the center column. The column on the right is an energy band diagram showing the response of interface states to the voltage pulse level.

circuit. To understand this current, consider the positively charged holes which form the inversion layer when the semiconductor surface under the gate is pulsed into inversion. The neutral donor-like interface states capture these holes (emit electrons) to become positively charged. A similar argument can be made for acceptor-like interface states, except that they become neutral. The magnitude of the voltage pulse is now returned to a value such that the silicon surface is accumulated. It is assumed that all the inversion layer holes return to the source and drain. The electrons accumulated at the surface are now captured by the positively charged donor-like interface states which become neutral. In the external circuit, this appears as a positive current. At the same time the neutral acceptor-like interface states capture electrons (emit a hole) and become negatively charged. These emitted holes lead to a current in the external circuit, and it is in the same direction as that from the donor states. The measured average steady-state current, since the MOS structure is repetitively pulsed, is called "charge-pumping current."

As just explained, the charge-pumping current, I_{cp}, measured in the external circuit is the sum of the current from the donor-like interface states, I_{cp}^d, and the current from the acceptor-like states, I_{cp}^a, and is given by the following equation:

$$I_{cp} = I_{cp}^d + I_{cp}^a \; . \tag{13}$$

The magnitude of this current is related to the numbers of interface states by the equation:

$$I_{cp} = f\, q\, A_g \left(N_{it}^d + N_{it}^a\right) = f\, q\, A_g\, N_{it} \; . \tag{14}$$

In this expression, f is the repetition rate of the gate pulse train; A_g is the area of the gate; q, the electronic charge; and N_{it}^d and N_{it}^a, the densities of donor- and acceptor-like interface states, respectively, that have energy levels through which the Fermi level is swept when the gate voltage pulses are applied. The change in the Fermi level is illustrated in the energy band diagram in the right column of figure 11.

In eq (14), it was assumed that when the gate voltage pulse is turned off, all carriers except those trapped in interface defects return to the junction. However, some fraction, α, of the mobile charge may not drift back to the source and drain. Thus, a "geometric" component [101] is be added to the charge-pumping equation to give:

$$I_{cp} = f\, A_g \left(qN_{it} - \alpha C_{ox} \left(V_g - V_T\right)\right) \; , \tag{15}$$

where C_{ox} is the gate oxide capacitance, V_g is the gate voltage pulse amplitude, and V_T is the threshold voltage of the MOSFET. The "geometry" component is experimentally determined by measuring the charge-pumping current *versus* gate base level of voltage pulse for a given source-drain reverse bias voltage, as shown in the I-V curve at the bottom of figure 11. A constant value, after an initial rapid increase, of current as a function of pulse amplitude indicates a negligible "geometry component." In the I-V curve, the

current levels labeled with letters correspond to the position of the square waves in the center column of figure 11, labeled a, b, and c.

To demonstrate the utility of the charge-pumping technique in determining the density of interface trapped charge, *n*- and *p*-channel transistors fabricated in a silicon gate bulk CMOS process on 3- to 5-Ω•cm *n*-type silicon substrates were used. In figure 12, the charge-pumping current is plotted as the 50-kHz pulse base level is varied as was described in figure 11. Using eq (8), the density of interface states for this MOSFET, N_{it}, was determined to be $\sim 1.13 \times 10^{12}$ cm^{-2}. The area was calculated using the designed dimensions. The *p*-channel transistor was used for a similar measurement, and the density of interface states was determined to be $\sim 1.27 \times 10^{11}$ cm^{-2}. The results are illustrated in figure 13. The insets in figures 12 and 13 show schematically the circuits used to make these measurements.

5. GATED-DIODE TEST STRUCTURE

In the previous sections, techniques for determining neutral trapped charge density and interface trapped charge density were discussed. The test structures employed were MOS capacitors and MOSFETS. The integrated gated-diode electrometer [19] is a device that offers the possibility of using one test structure to address several different measurements. The gated diode, a junction diode which is surrounded by a gate, has been used to measure bulk generation lifetime and surface recombination velocity [105]. Figure 14 illustrates the reverse-bias leakage current characteristics of a gated diode as a function of the gate voltage. When the gate voltage is adjusted such that the silicon surface beneath the gate is accumulated, the reverse-bias leakage current is due to generation in the bulk depletion region under the junction. When the gate voltage is adjusted so that the silicon under the gate is depleted, the measured leakage increases. The additional leakage current is due to generation at interface states and in the depleted volume under the gate. When the silicon surface beneath the gate is inverted by the gate bias voltage, the lower amount of leakage current is due to generation current from the depleted volume under the junction and under the gate. The surface states no longer contribute.

The schematic diagram for the NBS integrated gated-diode electrometer, which is a gated diode integrated with a source-follower electrometer, is shown in figure 15. In this figure the transistor Q1 acts as a switch which allows a reverse-bias voltage, V, to be applied to the diode junction. When Q1 is turned off, the depletion region due to the reverse bias voltage begins to collapse. This collapse is due to the leakage current in the various depletion regions. The change in voltage dV/dt is related to I_L, through an expression of the type $I_L = C\,dV/dt$. In this expression C is the total capacitance of the depletion regions plus any parasitic capacitances in the structure.

A stand-alone gated-diode test structure from test pattern NBS-4 [90] was used to determine if the gated diode structure could be used to avalanche inject minority carriers and to do charge-pumping [90]. The diode was formed by diffusing phosphorus from a solid source to form a junction ~2 µm deep in 0.3-Ω•cm *p*-type silicon substrates. The charge-pumping current as a function of voltage pulse level behaved as it did for the transistor discussed earli-

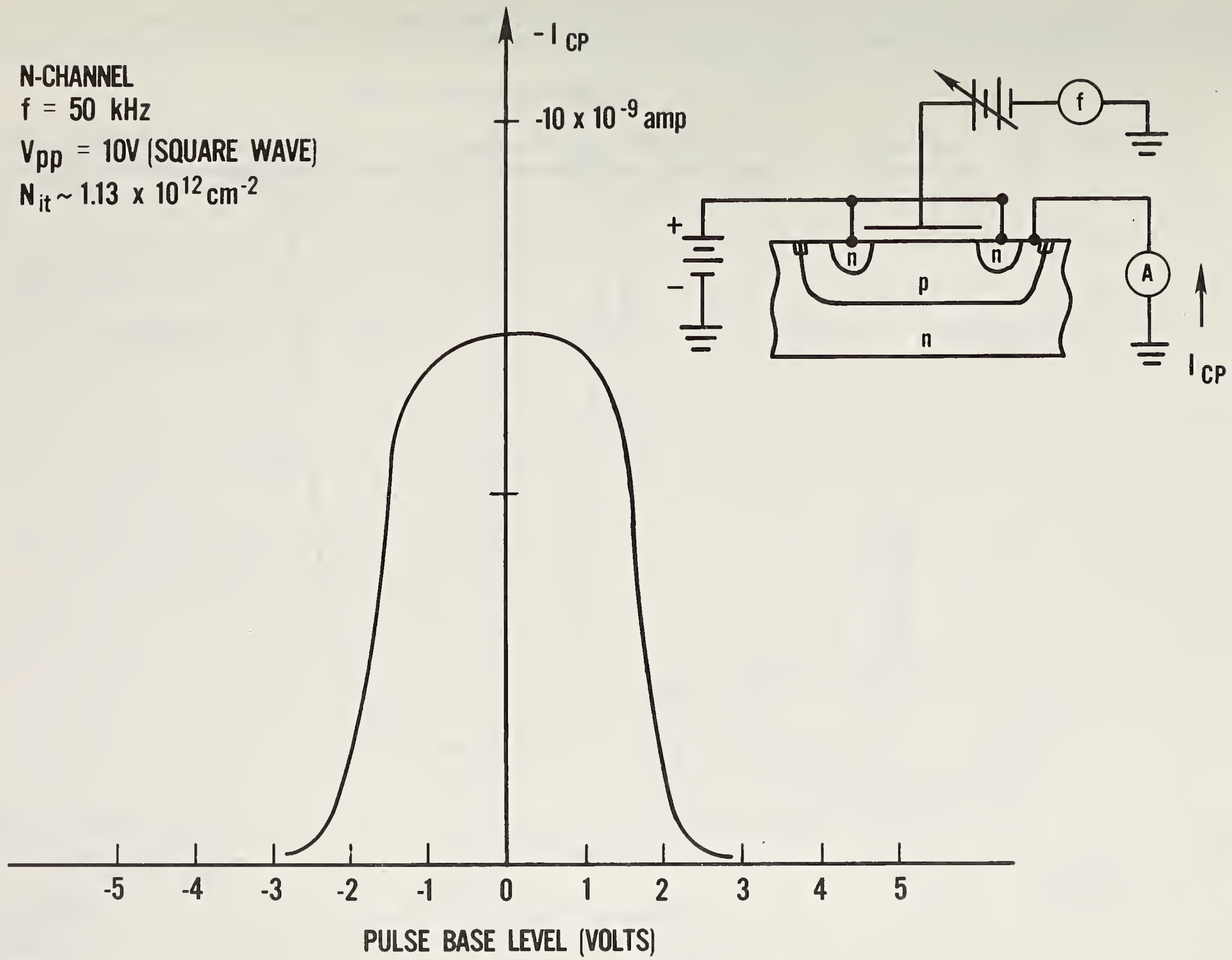


Figure 12. The charge-pumping I-V curve for an n-channel MOSFET. The inset on the right is a schematic of the circuit used to perform the measurement.

P-CHANNEL
f = 50 kHz
V_{pp} = 10V (SQUARE WAVE)
$N_{it} \sim 1.27 \times 10^{11}$ cm^{-2}

I_{CP}

$+10 \times 10^{-10}$ amps

PULSE BASE LEVEL (VOLTS)

Figure 13. The charge-pumping I-V curve for a *p*-channel MOSFET. The inset on the right is a schematic of the circuit used to perform the measurement.

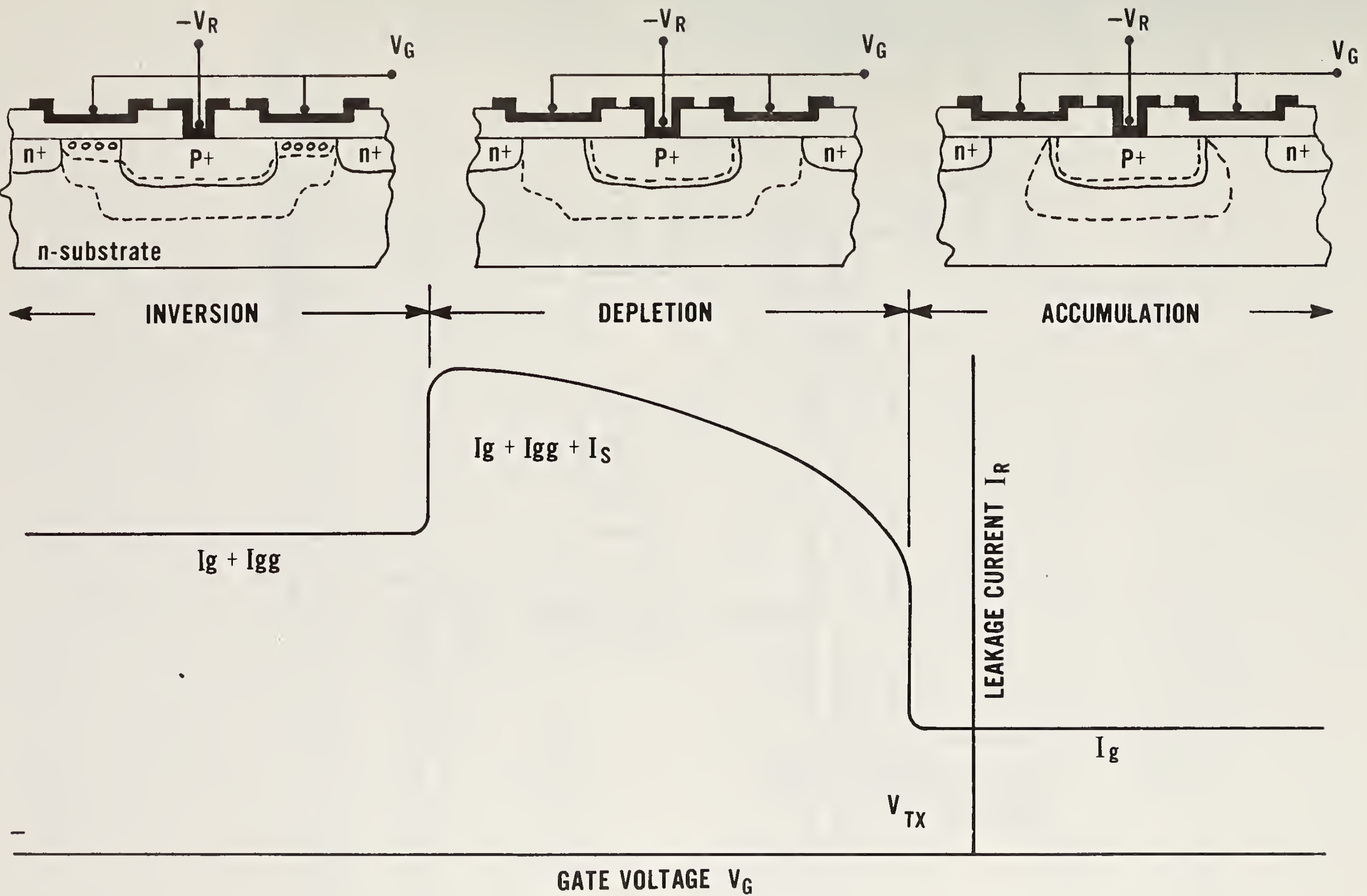


Figure 14. Idealized curve of reverse-bias leakage current I_l for a gated diode as a function of gate voltage showing the regimes where the condition of the material under the gate is accumulated, depleted, or inverted. I_g is the junction leakage current, I_s is the surface leakage current, and I_{gg} is the bulk leakage current. The insets at the top schematically illustrate the spatial extent of the depletion region for the case of a p^+n junction. (After Carver *et al.* [26])

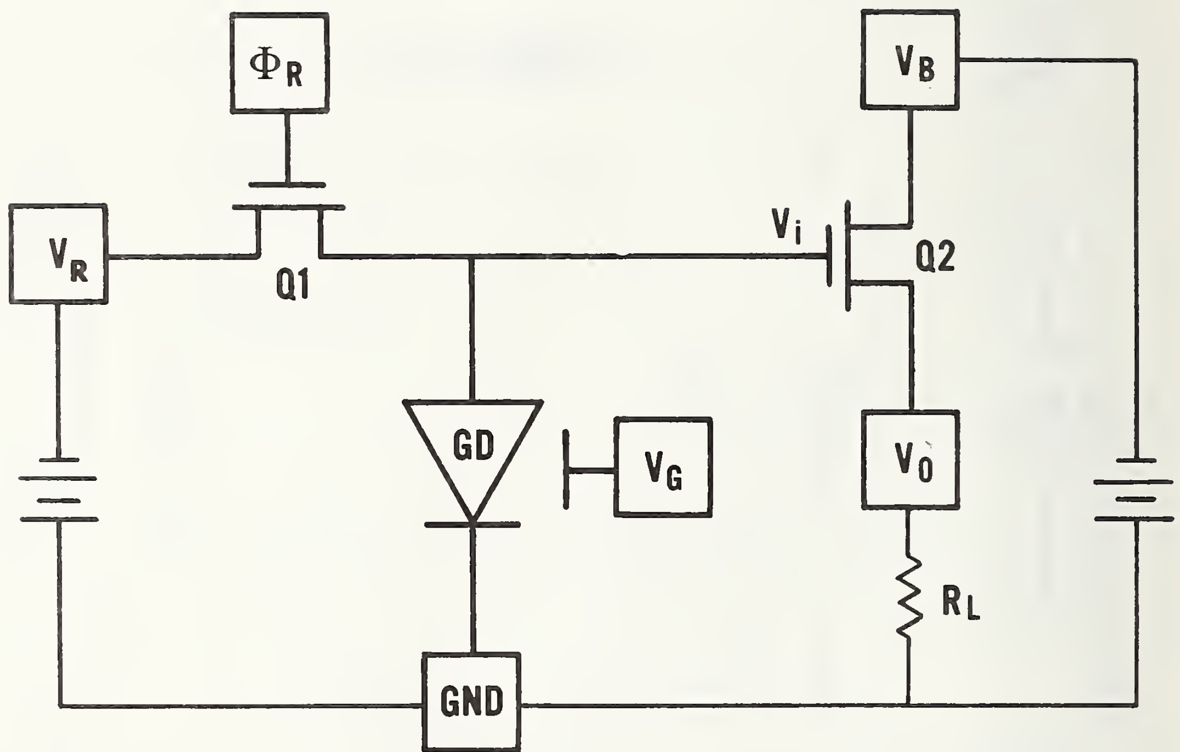


Figure 15. Schematic circuit diagram for the integrated gated-diode electrometer with a source-follower electrometer. The squares represent probe pads. The heavy lines denote portions of the circuit which are contained on the wafer. (After Carver *et al.* [26])

er. To inject electrons, a 10-kHz, 60-V square wave was applied to the gate of the gated-diode test structure. The C-V curves were remeasured and no shift in the flatband voltage was detected. This indicates that no charge was injected into the oxide. The charge-pumping I-V curve behaved similarly to that illustrated in figure 13. The p-type substrate cannot be pulsed into deep depletion because the adjacent n-region of the diode can act as a source of minority carriers for the p-region. The electrons form a negative space charge region under the gate. This space charge reduces the electric field in this region to a level below which avalanching can occur.

To prevent the n-region from acting as an electron source, the diode must be reverse biased to a voltage approximately equal to the amplitude of the avalanche injection voltage applied to the gate. However, the 60-V reverse-bias voltage exceeded the junction breakdown voltage of the diode. This situation is likely to occur in most devices of interest.

To prevent the junction from acting as a source of minority carriers and to avoid the necessity for extremely large reverse-bias voltages, a modification to the gated-diode test structure is required. A possible modification is the addition of a second gate surrounding and overlapping the existing gate; the avalanche and injection experiments would be performed on the second gate. The original gate acts as a switch - when open (biased into accumulation), it prevents the n-region from acting as a source of minority carriers for the surface under the outer measurement gate. A sketch of a dual gated-diode structure is shown in figure 16.

6. SUMMARY

The presence of oxide and interface trapped charge in MOSFETs causes the device characteristics to differ from the "ideal" characteristics usually assumed in IC design. The number and charge state of these defects are altered by various stresses during circuit fabrication, so it is important to know how these defect densities change with each process step and how they behave when a given process step is changed. If the physical identity of the defects were known, one could predict how these defect densities would change. Since their identity is not known, one must constantly measure their numbers. This report identifies measurement methods and microelectronic test structures which can be used to measure routinely oxide and interface trapped charge at the wafer level in an IC fabrication environment using computer-controlled instrumentation.

To study oxide trapped charge, free carriers must be present in the oxide to populate the oxide traps. High electric field techniques are appropriate for injecting free charge carriers into the gate oxide to become oxide trapped charge. A charge-pumping technique is the measurement method used for determining the density of interface trapped charge. Both of these measurement methods can be used in a production environment where routine measurement of these parameters occurs at the wafer level. These measurement methods make use of microelectronic test structures which are identical to those used to fabricate ICs.

A proposed new test structure useful for these measurements is a modified gated diode. A second gate surrounding the junction is added forming a dual-

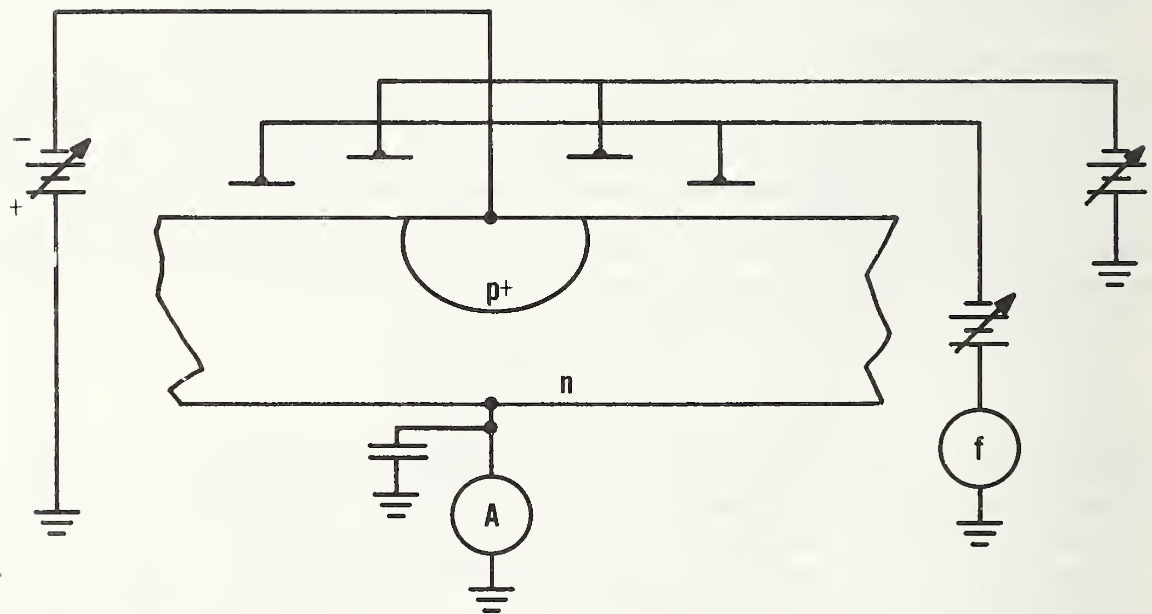


Figure 16. A schematic circuit diagram for measuring a dual-gated diode test structure.

gate gated diode. The dual-gate test structure can be used to measure leakage currents and oxide and interface trapped charge densities, thus allowing several measurements using a single test structure.

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

Interface states and oxide neutral traps are defects in metal-oxide-semiconductor (MOS) structures which adversely affect the operation of integrated circuits (IC). For very large scale integration (VLSI), the advanced techniques which are used to fabricate circuits with devices of submicrometer geometries expose the devices to ionizing radiation which can create these defects or alter the number of defects and their charge state and thus modify device operating characteristics. The physical identities of the defects which trap charge at the interface and in the bulk oxide are not well established. This means that one cannot a priori predict the behavior of the defects to a stress or fabrication process. Thus, it is desirable that the density of these defects be monitored routinely and that the measurement method used be easy to perform and fast and that it provide unambiguous results and be compatible with a production environment. The purpose of this study is to identify production-compatible measurement methods which can be used for routine measurement of neutral trap density and interface trapped charge. This study reviews the application of existing methods for quantifying the number of these defects. Methods determined to be most appropriate for the stated purpose are discussed in detail.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

Avalanche injection; capacitance-voltage curves; charge injection; charge pumping; gated diodes; interface states; metal-oxide-semiconductor devices; microelectronic test structures; MOSFETs; neutral traps; oxide-semiconductor interface; test structures.

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