NBSIR 81-2224

Advancement of Reliability, Processing and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS)

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Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
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Washington, DC 20234

Final Report

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U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

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Preface

In 1972, Dr. Martin Stickley, then Director of the ARPA Materials Science Office, with the advice and cooperation of Dr. George Heilmeier, then Assistant Director of Defense Research and Engineering (Electronics and Physical Science), requested Mr. Judson French, then Chief of the NBS Electronic Technology Division, to develop the plans for a research program directed toward attacking the problem of integrated circuit reliability through improvements in process controls and other means of building in quality.

The measurement-oriented program that resulted is described in this report. The initiation of the program received the enthusiastic support of Dr. Stephen Lukasic, then Director of ARPA. As time progressed and personnel changed, the program benefited from the advice and counsel of many individuals: Dr. Richard Reynolds, of the ARPA Materials Science Office (who, as the ARPA Project Officer, was directly responsible for the program during most of its existence); Dr. Arden Bement, later Director of the ARPA Materials Science Office; Dr. Heilmeier and Dr. Robert Fossum during their tenures as Director of ARPA; and Mr. Leonard Weisberg, later Assistant Director of Defense Research and Engineering (Electronics and Physical Science). Their encouragement and support is gratefully acknowledged.

The program also benefited from the cooperation of many in the industry who participated as contractors, collaborators, or sources of information. Their contributions, and those of the individual NBS researchers who conducted the in-house work, were essential to the program's success.

Ultimately, the measure of success of a program such as this is the effective utilization of the results of the research. Examples of such utilization are provided in the report; it is hoped that these and other unrecorded applications have fulfilled the expectations of the forward-looking managers who defined the need and initiated the program.

The problems addressed in this program present, in reality, a moving target. New advances in metrology are required to satisfy the demands of current and projected integrated circuit technologies. NBS is seeking to meet these needs through a major initiative on Basic Measurements for Very Large Scale Integration together with projects conducted in support of the Very High Speed Integrated Circuit and other advanced Defense Department programs.

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EXECUTIVE SUMMARY

In the early 1970s, the Defense Department's long-standing problem in obtaining specialized integrated circuits which would meet its reliability requirements at reasonable cost became more serious. It seemed clear that procurement of reliable integrated circuits by the traditional techniques would become increasingly more costly and difficult.

Procurement of semiconductor components for military use had traditionally been based on performance specifications supported by tests to screen out defective parts. By the early 1970s, this concept had been extended to procurement of integrated circuits, but there was considerable concern that the projected increases in the level of complexity of integrated circuits would eventually make full fault isolation by this technique prohibitively expensive both in time and money. The use of captive production lines to assure the manufacture of specialized devices and integrated circuits with controlled performance characteristics and adequate reliability though effective in special cases could not be extended broadly because of considerations of cost and flexibility.

The program described in this report was undertaken in 1973 to develop the measurement technology necessary to enable device manufacturers to exert more effective control over the materials and processes they use to make integrated circuits. It was devised to exploit and extend the ongoing NBS research activity on semiconductor measurement technology in which particularly effective interactions with the industry had already developed. Rather than following the more traditional and costly approach of tested-in reliability, this program provided a new thrust directed toward solving the DoD problem with integrated circuit reliability by providing the means to build in reliability in the production process, thus reducing the reliance on screening tests or captive lines. It had as its objective the development of methods of measurement and associated technology for use in controlling, and ultimately automating, various key processing and assembly procedures required for producing semiconductor devices, especially digital monolithic integrated circuits. The program consisted of a laboratory-based research effort; in-house studies at NBS and efforts contracted out-of-house to industry, universities, and other government laboratories were conducted. The program was initiated in January 1973 with a preliminary six-month planning phase; it was funded under ARPA Order 2397 during each of the next six fiscal years to a total level of about $10.9 million. The program ended formally at the end of October 1979, although a few contract research activities continued further into fiscal year 1980.

Work was carried out in 12 technical areas: resistivity and dopant characterization; crystal defects and contaminants; oxides and other insulator films; physical analysis techniques; film and layer thickness; materials for infrared detector arrays; materials and procedures for wafer processing; photolithography; microelectronic test patterns; wafer inspection and test; die and interconnection bonding; and hermeticity.

Advances in measurement technology were made in each of the 60 measurement problem areas addressed during the course of the program. These advances were communicated to the industry through seminars and workshops, individual plant and agency visits, videotapes on selected measurement techniques, and publications both in trade and archival journals and in a series of NBS reports on Semiconductor Measurement Technology specially established for this program. To date, over 220 reports of work conducted as part of this program have appeared in the technical literature; in addition, 20 progress reports were issued to provide information on the status of the research. These publications include reports from 24 contracted research projects on a wide variety of topics, which were carried out, usually over several years, by 10 industrial or consulting firms, three universities, and four government laboratories.

Timely implementation of the improved measurement technology developed in the program has already resulted in significant improvements in device performance and reliability as well as substantial cost savings in DoD programs. Thus, the technical feasibility of the approach chosen, providing the means to build reliability into the production process through the development of new or improved measurement techniques for use by the integrated circuit (IC) industry, has been demonstrated. Although most of the work was directed toward silicon IC technologies, results have also been applied in connection with characterization of infrared detector materials and in gallium arsenide integrated circuit technology.

Major impacts of the work resulted from applications of these techniques by the industry in both DoD and non-DoD programs. In addition, the results have been beneficially applied by systems houses. Evidence of application occurs through inclusion in widely used standards, through requests for specific items, or as a result of specific feedback which is principally anecdotal in nature. Work is continuing in connection with the tri-service programs on Very High Speed Integrated Circuits (VHSIC); many industrial contractors in this program are applying the results obtained to date and several are cooperating in extending the work. In addition, the concepts developed in regard to microelectronic test structures are being applied in connection with the fabrication of multipurpose chips as part of a major ARPA-supported long-range research effort on very large scale integration. Further, NBS is undertaking a major initiative on Basic Measurements for Very Large Scale Integration (VLSI) beginning in fiscal year 1981.

In summary, many improved measurement technologies of considerable diversity were developed and documented during this program. The results have been widely and beneficially applied in other DoD projects and by the U.S. semiconductor industry. At the present time the work is being extended under other programs to accommodate the denser circuits, larger chips, and new processing techniques associated with VLSI.

1. PROGRAM OBJECTIVE AND TECHNICAL NEED

1.1 Defense problem — In the early 1970s, the Defense Department's long-standing problem in obtaining reliable integrated circuits was aggravated by the rapidly growing commercial market for these devices. Because the Department's requirements share of the market was declining, it found difficulty in procuring at reasonable cost needed specialized integrated circuits which met its reliability requirements. It seemed clear that the combination of high performance requirements and small market volume would continue into the future and that procurement of reliable integrated circuits by the traditional techniques would become increasingly more costly and difficult.

This problem was reflected in overall system effectiveness. Rear Admiral R. J. Schneider pointed out in the keynote speech at the Navy Solid State Device Reliability Workshop, held in July 1972, that on the average, of the 100 aircraft on a billion-dollar attack carrier, only 65 were available at any given time. He described this situation as "one glaring example of how poor reliability affects operational effectiveness."[1] The poor performance records of some very costly aircraft and missile systems had been amply documented. Military avionics was achieving only 10 percent of targeted reliability,[2] and high failure rates had long been commonplace.[3]

A related problem area was the high cost of maintaining systems in the field. Failure is expensive; the annual cost to the DoD for maintenance of electronic equipment was estimated at $5 billion. For one type of DoD electronic equipment, 72.8 percent of the field failures were attributable to integrated circuits. Even the simplest component failure in the field has been found to cost the military a minimum of $300.[2]

1.2 State of the art at inception of program — Procurement of semiconductor components for military use had traditionally been based on performance specifications supported by tests to screen out defective parts. This approach, though expensive and frequently avoided through the use of waivers, had had demonstrated effectiveness when properly applied in the procurement of passive components, diodes, and transistors. By the early 1970s, the initial resistance to its extension to procurement of integrated circuits had been largely overcome. Nevertheless, there was considerable concern that the projected increases in the level of complexity of integrated circuits would eventually make full fault isolation by this technique prohibitively expensive both in time and money.

During this time, several strategic system projects were utilizing captive production lines to assure the manufacture of specialized devices and integrated circuits with controlled performance characteristics and adequate reliability. This alternative approach, though effective in special cases, could not be extended broadly because of considerations of cost and flexibility.

Other solutions to the problem were being sought. At the request of the Office of Defense Research and Engineering, an *ad hoc* committee of the National Materials Advisory Board investigated yield and materials problems in the manufacture of electronic components. While the reports of this

committee[4] and its subsidiary yield panel[5] indicated the need to improve existing procurement, screening, and acceptance procedures, they also emphasized the immense benefits which could be obtained through improved processes and in-process measurements, leading to upgraded yields, quality, and reliability throughout the electronics industry. In particular, they concluded that: "the impact of an organized program to make in-process measurements (for the manufacture of silicon semiconductor devices) could be truly immense. All aspects of the electronics industry would be upgraded by higher yields, quality, and reliability. The increased understanding of device processing would allow pursuit of goals that are presently unattainable because of geometrical or reliability limitations (microwave, displays, memories, etc.)."[4] The workshop on Solid State Device Reliability reached generally similar conclusions.[1]

Research and development programs underway in several government agencies were closely related to this problem. The National Bureau of Standards had for some time been concerned with measurement technology for semiconductor devices.[6] Even before it was formalized in 1968, the NBS Semiconductor Technology Program had been directed toward the enhancement of the performance, interchangeability, and reliability of semiconductor devices and the promotion of economy in their procurement through improvements in methods of measurement for the specification of materials and devices and for the control of device fabrication and assembly processes. This program had developed particularly effective interactions with the industry, both in defining and in disseminating the results of research projects and also had worked closely with the staff of a strategic systems project office to implement critically needed techniques for controlling the wire bonding process.

During FY-1973, the Naval Electronics Systems Command and the Naval Electronics Laboratory Center entered into contracts with three integrated circuit (IC) manufacturers to define research efforts directed toward improvement of IC reliability and manufacturing science (ICRMS). These efforts were expected to encompass the use of new manufacturing technologies as well as diagnostic and prediction techniques for control of IC processes.

A NASA effort on line certification which had been underway at the Marshall Space Flight Center for a number of years applied most of the existing tools for control of processes. The experience gained in connection with line certification provided a valuable base on which to build further work on test methodology. By 1973, NASA had consolidated much of its process-directed research and development activity into an overall project at the Jet Propulsion Laboratory intended eventually to lead to automated production of devices with predictable service life.

Finally, during the early 1970s, the Defense Advanced Research Projects Agency (ARPA) sponsored several fairly basic research efforts related to properties of thin insulating films including those characteristic of films used in metal-insulator-semiconductor (MIS) devices and a study of process-induced damage in silicon wafers. These projects, the last most directly, related to the question of device quality and understanding of device characteristics.

1.3 Specific technological problem addressed – The program described in this report was undertaken in 1973 to develop the measurement technology necessary to enable device manufacturers to exert more effective control over the materials and processes they use to make integrated circuits. It was devised to exploit and extend ongoing NBS research activity on semiconductor measurement technology. Rather than following the more traditional and costly approach of tested-in reliability, this program provided a new thrust directed toward the goal of built-in reliability through design, control of fabrication, and automation.

1.4 Anticipated payoff – This program was expected to assist in solving the DoD problem with integrated circuit reliability by providing the means to build in reliability in the production process, thus reducing the reliance on screening tests or captive lines. The program was to provide these means by developing new and improved process measurement techniques for use by the integrated circuit industry to achieve greatly improved control over material and device fabrication processes. These new controls would enable the manufacture of devices with narrower parameter distributions, and improved yields, reliability, and performance at lower cost. In the course of developing new process measurement and control techniques, the level of understanding of the intricacies of semiconductor processing would be greatly enhanced, leading to a considerable replacement of art by science in this field. Thus, this approach was seen as new, important, and viable.

The program was originally projected to cover a five-year period beginning in July 1973; the total cost was originally estimated to be in the range of $15 to $18 million. As actually carried out, the program was initiated in January 1973 with a preliminary six-month planning phase; it was funded under ARPA order 2397 during each of the next six fiscal years to a total level of about $10.9 million. The program ended formally at the end of October 1979, although a few contract research activities continued further into fiscal year 1980.

2. PROGRAM DESCRIPTION AND EVOLUTION

2.1 Program structure and plan – This program had as its objective the development of methods of measurement and associated technology for use in controlling, and ultimately automating, various key processing and assembly procedures required for producing semiconductor devices, especially digital monolithic integrated circuits. The program consisted of a laboratory-based research effort leading to practical output of methods and documentation for on-line use by the semiconductor integrated circuit manufacturer, his suppliers, and his customers. Both in-house studies at NBS and efforts contracted out-of-house to industry, universities, and other government laboratories were utilized.

Initially, an extensive field survey of the measurement needs of the semiconductor industry was conducted to assist in the selection of specific technical topics to be emphasized in the program. It is interesting to note that the items identified in this field survey were in general very similar to those identified to be controlled by the contractors in the Navy's ICRMS program, mentioned previously. Additional input was obtained in the first of a series of workshops designed to facilitate two-way communications between the Program and the industry.

Other communication mechanisms included individual plant and agency visits, preparation of videotapes on selected measurement techniques, publications in trade and archival journals, and, in particular, establishment of a subseries on Semiconductor Measurement Technology as part of the NBS Special Publication series. Of the 63 reports published to date in this subseries, 11 were progress reports, 32 were reports of ARPA-sponsored research, and four were reports of ARPA/NBS workshops; the remaining 16 were reports of work or workshops sponsored by NBS or other agencies. Two of the three videotapes prepared covered ARPA-sponsored work.

During the course of the program, 24 contracted research projects* on a wide variety of topics were carried out, usually over several years, by 10 industrial or consulting firms, three universities, and four government laboratories. In addition, several NBS divisions (other than the Electron Devices Division, previously the Electronic Technology Division, where the bulk of the in-house effort was carried out) participated in selected portions of the program.

2.2 Major technical problems and approaches – Specific technical topics selected for attention covered key processing and assembly steps, from control of incoming materials to evaluation of electrical characteristics and packaging. The comprehensive nature of this program, from starting materials through processing procedures to devices and from review of the state-of-the-art through the necessary research and development to practical application, permitted problems to be approached in a manner significantly different from that usually employed and led to rapid development and application of improved measurement methodology.

* A summary of research contracts issued during the program is provided in Appendix A.

Initially, work was undertaken in the following technical areas:

Resistivity and Dopant Characterization
Crystal Defects and Contaminants
Oxides and Other Insulator Films
Microelectronic Test Patterns
Photoresist
Film and Layer Thickness
Photomask Inspection
Wafer Inspection and Test
Die and Interconnection Bonding
Hermeticity and Residual Gas Analysis

In addition, activities were undertaken to improve in-house wafer processing capabilities and to establish improved methods for communicating with the industry (for both planning and dissemination purposes as noted in the previous subsection).

As the program developed, the work on oxides and other insulator films was extended to include study of a broad range of physical analysis methods. In addition, several projects related to materials and procedures for wafer processing were carried out, a relatively small laboratory effort was undertaken related to characterization of infrared detector materials, and consultation was provided to ARPA contractors regarding application of test structures and measurement techniques to the characterization of gallium arsenide. Major efforts were concentrated on development of optical methods for measuring linewidths (in the 0.5- to 10-μm range) in patterns on photomasks and wafers (an outgrowth of the initial work on photomask inspection) and on development, evaluation, and implementation of microelectronic test structures, the last frequently in concert with DoD agencies other than ARPA.

The general approach to the development of improvements in measurement methods began with identification of problem areas. This occurred as a result of contacts with military or other government agencies, participation in standards committees, or visits to or other contacts with industry. Once a problem area had been selected, the status of the field was determined through direct consultation, standards-committee activity, and literature search. The results of this determination were used in the planning of detailed steps toward solving the problem. Many times they also served another important function by forming the basis of a critical review, bibliography, or other survey report which had considerable value in communicating to the community-at-large the present status of a measurement area.

The steps toward solution of the problem involved a combination of laboratory investigation, standards-committee activities (including cooperative round-robin experiments), review and inclusion of work carried on elsewhere, and direct interaction with industry through visits, sponsors, or standards committees. As the work progressed, the information and techniques which resulted were disseminated as widely as possible. Use of interim results frequently improved manufacturing or measuring procedures; an important part of the work involved assistance to the industry, through training programs and other means, in incorporating and benefiting from these results at the earliest possible time. Ultimately, the results of the work were incorporated

into standard test methods or procedures. One very important aspect of the program was reduction of duplication of effort through the widest possible dissemination of the results achieved in-house and reported by others.

3. SCIENTIFIC AND TECHNICAL RESULTS AND ACCOMPLISHMENTS

Advances in measurement technology were made in each of the 60 measurement problem areas addressed during the course of the program. These were summarized in comprehensive progress reports (21a, 22/23a, 24a, 25a, 26a, 27/28a, 29/30a, 31/32a, 33a, 34/35a, 36/37a)* which cover the period between 1 July 1973 and 30 September 1977 and in progress briefs (38a, 39a, 40a, 41a, 42a, 43a, 44a, 45a, 46a) which cover the period between 1 October 1977 and 31 December 1979. In most cases, the results are more completely described in over 220 separate technical reports and articles, which are listed in section 6.

A brief listing of the various advances achieved follows with references to the more detailed reports and, in selected instances, other comments. Work is continuing in many of the technical areas addressed during this program. Information concerning on-going research activity is provided in the reports, Semiconductor Technology Program, Progress Briefs, which are issued about four times a year in the NBSIR series. A complete listing of publications which are available for unlimited distribution is provided in NBS List of Publications 72, Semiconductor Measurement Technology, which is revised annually in order to provide a complete record of NBS publication on Semiconductor Measurement Technology for the period up to the revision date.

A. Program Planning and Dissemination

(1) Initial workshop on IC measurement problems: 2n
(2) Initial review of trends in automated processing and assembly (contract 4-35807 to A. D. Little, Inc.): C15o
(3) General report on program content: 21o

B. Resistivity; Dopant Characterization

(1) Interlaboratory test for stability of and long-term precision attainable with standard reference wafers for four-probe resistivity measurements: †
(2) Surface preparation procedures for spreading resistance measurements: 15b, 20b (Additional results, obtained under Department of Energy sponsorship, may be found in references 7-9.)
(3) Algorithms for analysis of spreading resistance measurements (partially carried out under contract 5-35881 to Solecon Labs): 31b, 42b, 44b, §

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* Codes identify reports and other publications listed in section 6, Bibliography of Reports. The codes are identical with those used in NBS List of Publications 72. Codes beginning with "C" refer to publications prepared by contractors. Codes beginning with "N" refer to publications prepared by staff of other NBS divisions. Codes beginning with "R" refer to documents with restricted distribution; such documents are not listed in LP 72.

† Reported only in progress reports

§ Additional publications reporting work conducted at NBS in press or anticipated

(4) High-speed spreading resistance probe (contract 5-35914 to RCA Labs): C30b
(5) Impurity redistribution during thermal oxidation of silicon: 16b, 29b
(6) Algorithms for interpreting capacitance-voltage measurements of dopant profiles: 17b, 22b
(7) Computation of carrier mobilities in silicon (partially conducted under contract 7-35741 to University of Florida): 18b, 21b, C27b, C33b, ¶
(8) Re-evaluation of resistivity-dopant density relationships in silicon: 25b, 39b, 43b, § (This project also involved development of the planar square array four-probe test structure for resistivity measurements: 19b, 5g; development of the nuclear track technique for measurement of boron in silicon: 20d; and comparison of several techniques for measurement of phosphorus in silicon: 36b.)

C. Crystal Defects and Contaminants

(1) Deep-level measurements: 14c, 17c, 18c, 27c, 28c, 30c, 31c, 36c, 38c, 39c, 40c, 41c (Additional results, obtained under Department of Energy and NBS sponsorship, may be found in references 10-13.)
(2) Defect density profiling technique (order 809074 to Xerox Palo Alto Research Center): C35c, ¶

D. Oxides and Other Insulator Films

(1) Extended-range MIS capacitance-voltage and conductance-voltage technique (contract 5-35912 to RCA Laboratories): C19c, C20c, C21c, C22c, C23c, C24c, C25c, C26c, C33c (An application of the technique, partially supported by another DoD agency: C21l.)
(2) Bias-temperature stress test for oxide stability: †

E. Physical Analysis Techniques

(1) Surface analysis techniques: 3d, 7d
(2) Surface analysis workshop: 6n
(3) Electron spectroscopy techniques on sputter Auger profiling of the silicon-silicon dioxide interface (contract 5-35944 to Stanford University): C2d, C4d, C5d, C6d, C8d, C9d, C10d, C11d, C13d, C15d, C16d, C17d, C21d, C22d, V23d, C24d, C27d, C29d, C32d, C33d, C35d, C13e, C14e, C22e, ¶
(4) Optical reflectance methods for characterizing surface quality of sapphire substrates and surface damage of silicon (contract 5-35915 to RCA Laboratories): C1d, C19d, C30d, C38d
(5) X-ray photoelectron spectroscopy of clean silicon surfaces: N18½d
(6) X-ray photoelectron spectroscopy of the silicon-silicon dioxide interface (order 611377 to Jet Propulsion Laboratory): C18d, C26d, C36d, C37d, C42d, C321, C331, ¶

¶ Additional publications reporting work conducted by contractor in press or anticipated
§ Additional publications reporting work conducted at NBS in press or anticipated
† Reported only in progress reports

(7) Calibration standards for ion microprobe mass analysis (contract 5-35917 to Texas Instruments Central Research Laboratory): C14d, C31d

F. Film and Layer Thickness

(1) MOS capacitance methods for epitaxial layer thickness: †

G. Materials for Infrared Detector Arrays

(1) X-levels in indium-doped silicon: 24b, 38b, R32c
(2) Characterization of extrinsic silicon: 23b, 40b, 41b, R37c, §

H. Materials and Procedures for Wafer Processing

(1) Measurement techniques for purity of process chemicals (contract 5-35717 to Penn State University): C4e, C16e
(2) Dose measurements for ion implantation (contract 5-35891 to Hughes Research Labs): C7e, C12e
(3) Alignment effects on implantation profiles (contract 5-35891 to Hughes Research Labs): C2e, C6e, 15e, 20e, 23e, 25e, ¶
(4) Implantation profiles (contract 5-35891 to Hughes Research Labs and orders 708041 and 801846 to Naval Research Lab): C21e, C27e, C28e, C30e, §, ¶
(5) Nondestructive test for integrity of passivation overcoats (contract 5-35913 to RCA Laboratories): C12j, C15j, C22j
(6) Improvements to NBS wafer fabrication facility: 17e
(7) Process-induced radiation effects: 17l, 24l, 25l, 26l, 28l, 29l, 30l

I. Photolithography

(1) Photoresist sensitometry: 3e, 8e, 24e, 29e
(2) Comparisons of automated photomask inspection techniques (orders 408726, 503183, and 602156 to Lawrence Livermore Laboratory): 1f, 15f, 17f
(3) Optical linewidth measurements in the 0.5- to 10-μm range (significant funding also provided by NBS): N2f, N3f, N5f, N6f, 7f, N9f, N10f, N11f, N12f, N13f, N14f, 16f, 19f, 21f, 22f, 23f, 24f, 25f, 27f, § (Initial results on semitransparent photomasks, carried out with NBS sponsorship may be found in reference 14.)
(4) Linewidth measurement by diffraction pattern analysis (contract 5-35890 and order 702980 to Recognition Systems Incorporated): C4f, C26f

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† Reported only in progress reports
¶ Additional publications reporting work conducted by contractor in press or anticipated
§ Additional publications reporting work conducted at NBS in press or anticipated

J. Microelectronic Test Patterns

(1) General applications: 1g, 6g, 7g, 8g, 10g, 17g, 20g, 23g, 28g, 32g, 33g
(2) Test pattern workshop: 5n
(3) Test patterns designed for use in re-evaluating resistivity-dopant density relationships in silicon (NBS-3 and NBS-4): 3g, 4g, 16g
(4) Test patterns for CMOS/SOS LSI process (contract 5-35916 to RCA Laboratories): C12g, C29g
(5) Test patterns for probe card evaluation: 19g
(6) The circular charge-coupled device as a microelectronic test structure (order 502498 to Naval Electronics Laboratory Center): C2g
(7) Modular array concept: 24g, 27g
(8) Sheet resistor test structures: 9g, 14g, 15g
(9) Application of the cross-bridge sheet resistor test structure for evaluating linewidth variations associated with mask fabrication and wafer processing: † (Additional results, carried out with AFAL sponsorship, may be found in reference 15.)
(10) Production-compatible potentiometric electrical alignment test structure: 11g, 25g
(11) Design and initial testing of integrated gated-diode-electrometer test structure for measurement of leakage current, generation lifetimes, etc. (contract 6-35766 to Westinghouse Defense and Electronic Systems Center): 21g, ¶ (Additional results, carried out with CSDL (Navy) sponsorship, may be found in reference 16.)
(12) MOSFET profiler for measuring dopant profiles by means of a conventional wafer prober with dc instrumentation: 13g, 18g, 30g
(13) Random fault test structures: †

K. Wafer Inspection and Test

(1) Automated scanning low energy electron probe (orders 501718, 602542, and 711782 to Naval Research Laboratory): C25d, C28d
(2) Dual wavelength laser-source flying-spot scanner: 4j, 5j, 6j, 10j, 11j, 14j, 21j (Results of later extensions, under Department of Energy sponsorship, to the study of large-area photovoltaic solar cells may be found in reference 17.)
(3) Scanning electron microscopy (contract 4-35897 and order 513840 to Hi Rel Labs: 16j
(4) Use of the SEM in the electron-beam-induced-current (EBIC) mode: 7j, 8j, 9j, 13j
(5) Basic investigations of scanning acoustic microscopy (contract 5-35899 to Stanford University): C18j, C23j, C24j, C29j, C33j, C34j, C36j
(6) Development of scanning acoustic microscopy in an industrial environment (contract 5-35898 to Hughes Research Labs): C17j, C19j, C25j, C27j, C28j, C30j, C31j, C16o, ¶

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† Reported only in progress reports
¶ Additional publications reporting work conducted by contractor in press or anticipated

L. Die and Interconnection Bonding

(1) Thermal response technique for die attach evaluation: †
(2) Ultrasonic wire bonding mechanisms and process monitor tests: 11h, 12h, 16h (A summary of results obtained prior to the inception of this program may be found in reference 18.)
(3) Wire bond pull tests (destructive and nondestructive): 17h, 18h (A summary of results obtained prior to the inception of this program may be found in reference 19.)
(4) Acoustic emission techniques for evaluating bond integrity: 14h, 15h, 20h

M. Hermeticity and Moisture Measurement

(1) Relationship between moisture infusion and device reliability (contract 5-35880 to Martin Marietta - Orlando): C4i, C5i
(2) Hermeticity and moisture measurement workshops: 3n, §
(3) Interlaboratory evaluation of radioisotope leak test: 3i
(4) Dry-gas gross leak tests: † (Additional results, obtained with NBS funding, may be found in reference 20.)

† Reported only in progress reports
§ Additional publications reporting work conducted at NBS in press or anticipated

4. APPLICATIONS AND CONSIDERATIONS FOR THE FUTURE

4.1 Conclusions of technical feasibility – In this Program many improved measurement technologies of considerable diversity were developed and documented. As discussed in greater detail in the following section, timely implementation of some of these technologies has already resulted in significant improvements in device performance and reliability as well as substantial cost savings in DoD programs. Thus, the technical feasibility of the approach chosen, providing the means to build reliability into the production process through the development of new or improved measurement techniques for use by the integrated circuit industry, has been demonstrated.

4.2 Additional R&D requirements and opportunities – Recent trends in integrated circuits have been toward very large scale integration with greater complexity, larger device density, smaller feature size, and larger chip size. These trends, together with shifts toward new process technologies, have resulted in still greater demands on the technology for dimensional measurements, materials characterization, and other types of measurements for control of fabrication and assembly processes.[21] Consequently, despite the progress made during the course of this Program, many measurement problems remain to be solved.

NBS is continuing work on optical linewidth measurements in the 0.5- to 10-μm range and on microelectronic test structures as part of the Defense Department's program to develop very high speed integrated circuits (VHSIC). Implementation of the results obtained in these and other project areas will assist VHSIC contractors in the efficient fabrication of chip sets for the VHSIC program. Other opportunities to both apply and extend this work will occur in the ARPA Ultra High Speed Integrated Circuit Program. NBS staff are presently engaged in preliminary activity associated with selected parts of this ARPA Program.

In addition, the Commerce Department has undertaken an initiative on Basic Measurements for Very Large Scale Integration (VLSI) in the NBS Electron Devices Division beginning in fiscal year 1981. This initiative is intended to provide the same types of technical outputs as the ongoing Semiconductor Technology Program, extended to accommodate the denser circuits, larger chips, and new processing techniques associated with VLSI. Although rather detailed preliminary plans have been developed,[22] it is essential to emphasize that considerable flexibility is required in order to enable the program to respond to industry requirements as they develop. It is also important to realize that, as has been done in the NBS Semiconductor Technology Program heretofore, many of these activities involve much more than simply finding a way to make a measurement. Fundamental work to develop a clear understanding of the basis for the measurement and its range of utility is often required as well. The augmented program will address the following key issues in six critical areas.

Silicon characterization: methods for profiling the distribution of dopant impurities, especially in shallow, low-dose ion implantations; methods for characterizing nondopant or deep-level impurities and resolution of differences between results obtained by various methods; identification of

appropriate parameters to be specified for substrate wafers; and techniques for characterizing wafer surface distortion.

Interface characterization: methods for measuring neutral trap densities and distributions near silicon-silicon dioxide interfaces; techniques for characterizing the structural and electrical properties of this and other device interfaces; techniques for evaluating multilayer metal interconnect systems; and methods for measuring contact resistance at the interconnect-semiconductor interface.

Process control metrology: methods for measuring linewidth and edge quality in small features with large aspect ratio (height to width); measures for sensitometry and other attributes of resists; and metrology associated with control of processes such as plasma etching, ion implantation, laser annealing, and ion milling.

Microelectronic test structures: scaling to VLSI dimensions of test structures for measuring material characteristics, pattern definition and registration, and random fault densities and distributions; test structures with integral signal processing circuitry; correlations between test structure characteristics and device or circuit properties; and dynamic and reliability test structures.

Package evaluation: methods for measuring device temperature and package heat transfer characteristics; methods for evaluating mechanical integrity; and tests for hermeticity and internal moisture levels.

Testing: models for fault mechanisms; this portion of the effort is expected to link with other NBS programs being developed to address broader aspects of testing complex integrated circuit chips and systems.

5. PROGRAM IMPACT AND ASSESSMENT OF TECHNOLOGY DEVELOPED

The results of this effort were a wide variety of well-documented processing practices, controls, and measurements for use on production lines throughout the silicon device industry. Major impacts of the work resulted from applications of these techniques by the industry in both DoD and non-DoD programs. In addition, the results have been beneficially applied by systems houses. Evidence of application occurs through inclusion in widely used standards, through requests for specific items, or as a result of specific feedback which is principally anecdotal in nature; the following examples are representative of those collected during the course of the program. It should be realized that some of the most recently achieved results have not yet been applied to the fullest extent and that reports of additional use of old, as well as new, results are continuing to be received at frequent intervals.

- The silicon resistivity standards have been widely used throughout the industry; through September 1979, 114 sets of SRMs 1520 and 1521 and 20 of 1522 had been sold, fully depleting current stock. In 1980, 110 sets of SRMs 1521 and 1522 and 50 sets of 1523 will be certified based on procedures developed in this program. These reference standards are being used both for calibrating four-probe test sets and the newer contactless resistivity meters now finding greater use in the industry.

- The surface preparation procedures for spreading resistance measurements have been incorporated into standards whose development by ASTM Committee F-1 on Electronics is now nearing completion.[23]

- The revised resistivity-dopant density relationships are being incorporated in ASTM standards, now under development by ASTM Committee F-1, which will replace data long used by the industry.

- The computer program developed at NBS to evaluate electrical properties of extrinsic silicon and used as a critical element in the study of X-levels in indium-doped silicon, is in active use at Rockwell International; the program has also been requested by Hughes Aircraft Company, Honeywell, Air Force Materials Lab, Army Night Vision Lab, Jet Propulsion Lab, and University of Cincinnati.

- Rockwell International has routinely applied the room temperature spreading resistance profiling method for measuring uniformity of indium density in silicon wafers following NBS demonstration of the value and suitability of this method.

- The Air Force Materials Laboratory used NBS-determined Hall effect data on indium-doped silicon to test the validity of their Hall-analysis computer program; the NBS data are a sample data set of unquestioned reliability for which the correct analysis results are known. The same data were also supplied to IBM for a similar type of analysis.

- Both equipment manufacturers and users recognized the importance of utilizing the principles developed in the work on Dose Measurements for Ion Implantation, performed at Hughes Research Laboratories under contract, to obtain adequate control of the implantation process.

- The work on Angular Sensitivity of Controlled Implanted Doping Profiles (jointly carried out at NBS and Hughes) has led to a follow-on project supported by the Naval Ocean Systems Center at NBS to evaluate experimentally the junction depth of selected implants as a function of implant angle.

- Results of calculations of radiation levels associated with advanced lithographic and patterning techniques were used by the DoD VHSIC Lithography Committee as background material for developing a program to understand the radiation damage associated with x-ray and e-beam lithography.

- Fifty-seven persons representing 50 organizations (microscope, photomask, and integrated circuit manufacturers) participated in the first two training seminars held to describe NBS-developed procedures for measuring 1- to 10-μm wide lines on IC photomasks. At least two attendees followed up their participation by conducting mini-seminars at their own companies to transmit the information to coworkers. Also, at least one microscope manufacturer has modified the instruction manuals for its image-shearing measurement system to correspond with the NBS procedures. Continued interest has led to the conduct of two additional seminars in 1980, accommodating over 70 more persons and the scheduling of a seminar on the West Coast in the spring of 1981.

- Many companies, including Burroughs, IBM, MOSTEK, Motorola, Siliconix, Hewlett-Packard (H-P), Vickers Instruments, Rockwell International, Western Electric, and Zeiss are currently using the linewidth measurement procedures developed by NBS.

- Ten companies, IBM, H-P, Vickers, ITP, Roger K. Sherman Co., Rockwell, National Semiconductor, Siliconix, Electromask, and Qualitron, participated with NBS in a collaborative experiment to establish the validity of a photomask-like linewidth standard (NBS SRM 474) and associated measurement procedures; many other companies expressed interest in participating in this experiment but could not be accommodated because it was not possible to calibrate enough test specimens before the experiment began.

- A linewidth measurement system based on the NBS scanning photometric microscope system is now available commercially.

- One or more of the mask sets for the three earliest test patterns developed in the program (NBS-2, NBS-3, and NBS-4) have been released to nearly 95 industrial, government, and academic organizations which have employed them in setting up process lines and for troubleshooting certain processing problems. Organizations which obtained these test patterns include Sandia Laboratories, Texas Instruments, Fairchild, MOSTEK, H-P, Tektronix, RCA, National Semiconductor, Motorola, Honeywell, Night Vision Lab, MIT, TRW, and Hughes.

- Tapes for test pattern NBS-15 for electrical measurement of photomask alignment have been sent to some eight companies including Texas

- Instruments, Motorola, Westinghouse, MOSTEK, Intel, Hughes, Fairchild, and National Semiconductor.

- Test structures developed and evaluated in the program have been widely adapted for in-house process development. Applications include gallium arsenide integrated circuits, silicon LSI circuits, bubble memory devices, SOS LSI circuits, radiation-hardened CMOS total dose test program, thin-film strain gages, and tin-oxide technology.

- RCA has utilized the spatial integrity test structure concept, developed under contract at RCA Labs, in connection with its SOS LSI manufacturing operations.

- At the request of the Air Force Weapons Laboratory, the design of the integrated gated diode electrometer test structure was supplied to Harris Semiconductor for use in a radiation-hardened CMOS total dose assurance program.

- Follow-on programs to develop and apply test structure concepts are being conducted in conjunction with the Air Force Avionics Laboratory (test patterns NBS-16 and NBS-26 for a radiation-hardened silicon-gate CMOS/SOS process), the Charles Stark Draper Laboratory (integrated gated-diode electrometer, MOSFET dc profiler, and other test structures as applied to a Navy radiation-hardened CCD development project), and the ARPA Ultra High Speed Integrated Circuits Program (test structures for CMOS/SOS process).

- The dual wavelength laser-source flying spot scanner has been adapted by the Hughes Aircraft Company and, in its modified form, replicated by the Solar Energy Research Institute and several Department of Energy contractors in the solar photovoltaic program.

- The scanning electron microscope procedures developed under contract at Hi Rel Laboratories are cited in MIL-STD-1580 and were used in training seminars conducted in conjunction with the Fifth Annual Advanced Techniques in Failure Analysis Symposium held in Los Angeles in October 1979.

- The destructive bond pull tests in MIL-STD-883B and MIL-STD-750B and the nondestructive bond pull test in MIL-STD-883B are based on ARPA-supported work at NBS.

- Two ASTM standards covering destructive and nondestructive wire bond tests resulted from the ARPA-supported work and are in use by the industry.

- Ribbon wire, initially developed in a previous ARPA-supported NBS project, was demonstrated to be superior for certain bonding applications; Cermet Division of Bala Electronics Corp. issued in the summer of 1978 a technical information report on bonding ribbon wire to thick film copper extracted directly from an NBS Progress Report. Also, a major semiconductor manufacturer has qualified a ribbon-wire process for some high-reliability programs.

- Equipment makers have incorporated results of NBS wire-bonding work in the design of new products. For example, Kulicke and Soffa (bonding machines), Small Precision Tools (bonding tools), Sterndent Metals (bonding wire), and Unitek (bond pullers) all have adopted appropriate results.

- During an NBS-coordinated and analyzed ASTM interlaboratory experiment, a major design fault was found in the automated destructive-nondestructive bond pull tester most widely used for testing high reliability devices. The manufacturer redesigned (following NBS suggestions) and retrofitted all of the thousand or so units in the field so that they could be used for pull testing in accordance with MIL-STD-883B and MIL-STD-750B.

- Application of the results of the wire-bonding work in military programs has led to yield increases by factors of 2 to 35 at the bonding step, avoided 3- to 6-month delays in programs, and saved millions of dollars in several high reliability programs. In addition, these results made possible construction of large hybrid circuits (with >500 bonds) which are essential to several programs.

- No field failures due to faulty wire bonds have been reported in several DoD programs which employed the NBS-developed bond test procedures.

- A major computer company has implemented 100-percent testing of some production thermal compression bonds in connectors using acoustic emission methods developed at NBS.

- General Dynamics is referencing NBS-developed information on an acoustic-emission bond-fatigue test in qualifying tape-bonded devices for a missile program.

- Ten organizations (including IBM, Motorola, IsoVac, Hughes, TRW, Fairchild, Burroughs, and Lockheed) participated in an NBS-coordinated interlaboratory test to improve radioisotope leak test procedures. This test both demonstrated that such interlaboratory tests were feasible for leak testing methods and resulted in an order of magnitude increase in the precision of the measurement.

- Modifications to seal tests in MIL-STD-750B and MIL-STD-883B were made based on NBS work.

These applications serve to illustrate the broad and comprehensive nature of the impact that the program has achieved.

6. BIBLIOGRAPHY OF REPORTS*

a. Progress Reports

21a Semiconductor Measurement Technology, Quarterly Report, July 1 to September 30, 1973, W. M. Bullis, Ed., NBS Spec. Publ. 400-1 (March 1974).

22/23a Semiconductor Measurement Technology, Combined Quarterly Report, October 1, 1973 to March 31, 1974, W. M. Bullis, Ed., NBS Spec. Publ. 400-4 (November 1974).

24a Semiconductor Measurement Technology, Progress Report, April 1 to June 30, 1974, W. M. Bullis, Ed., NBS Spec. Publ. 400-8 (February 1975).

25a Semiconductor Measurement Technology, Progress Report, July 1 to September 30, 1974, W. M. Bullis, Ed., NBS Spec. Publ. 400-12 (May 1975).

26a Semiconductor Measurement Technology, Progress Report, October 1, 1974 to December 31, 1974, W. M. Bullis, Ed., NBS Spec. Publ. 400-17 (November 1975).

27/28a Semiconductor Measurement Technology, Progress Report, January 1 to June 30, 1975, W. M. Bullis, Ed., NBS Spec. Publ. 400-19 (April 1976).

29/30a Semiconductor Measurement Technology, Progress Report, July 1, 1975 to December 31, 1975, W. M. Bullis, Ed., NBS Spec. Publ. 400-25 (October 1976).

31/32a Semiconductor Measurement Technology, Progress Report, January 1, 1976 to June 30, 1976, W. M. Bullis, Ed., NBS Spec. Publ. 400-29 (April 1977).

33a Semiconductor Measurement Technology, Progress Report, July 1 to September 30, 1976, W. M. Bullis and J. F. Mayo-Wells, Eds., NBS Spec. Publ. 400-36 (July 1978).

34/35a Semiconductor Measurement Technology, Progress Report, October 1, 1976 to March 31, 1977, W. M. Bullis, Ed., NBS Spec. Publ. 400-38 (November 1979).

* The codes used in this section are identical with those used in NBS List of Publications 72. This document is revised annually in order to provide a complete record of NBS publication on Semiconductor Measurement Technology for the period up to the revision date. Codes beginning with "C" refer to publications prepared by contractors. Codes beginning with "N" refer to publications prepared by staff of other NBS divisions. Codes beginning with "R" refer to documents with restricted distribution; such documents are not listed in LP 72.

36/37a Semiconductor Measurement Technology, Progress Report, April 1, 1977 to September 30, 1977, W. M. Bullis, Ed., NBS Spec. Publ. 400-45 (August 1980).

38a Semiconductor Technology Program, Progress Briefs, October 1, 1977 to December 31, 1977, W. M. Bullis, Ed., NBSIR 78-1444 (March 1978).

39a Semiconductor Technology Program, Progress Briefs, January 1, 1978 to March 31, 1978, W. M. Bullis, Ed., NBSIR 78-1444-2 (July 1978).

40a Semiconductor Technology Program, Progress Briefs, April 1, 1978 to June 30, 1978, W. M. Bullis, Ed., NBSIR 78-1444-3 (October 1978).

41a Semiconductor Technology Program, Progress Briefs, July 1, 1978 to September 30, 1978, W. M. Bullis, Ed., NBSIR 79-1591 (January 1979).

42a Semiconductor Technology Program, Progress Briefs, October 1, 1978 to December 31, 1978, W. M. Bullis, Ed., NBSIR 79-1591-2 (March 1979).

43a Semiconductor Technology Program, Progress Briefs, January 1, 1979 to March 31, 1979, W. M. Bullis, Ed., NBSIR 79-1591-3 (June 1979).

44a Semiconductor Technology Program, Progress Briefs, April 1, 1979 to June 30, 1979, W. M. Bullis, Ed., NBSIR 79-1591-4 (August 1979).

45a Semiconductor Technology Program, Progress Briefs, July 1, 1979 to September 30, 1979, W. M. Bullis, Ed., NBSIR 79-1591-5 (December 1979).

46a Semiconductor Technology Program, Progress Briefs, October 1, 1979 to December 31, 1979, W. M. Bullis, Ed., NBSIR 80-2006 (April 1980).

b. Resistivity and Hall Effect

15b Ehrstein, J. R., Improved Surface Preparation for Spreading Resistance Measurements on *p*-Type Silicon, *Semiconductor Measurement Technology:* Spreading Resistance Symposium, NBS Spec. Publ. 400-10 (December 1974), pp. 249-255.

N16b Kraft, R., Finite Difference Techniques for Diffusion and Redistribution Problems with Segregation-type Boundary Conditions, *Proceedings of the AICA International Symposium on Computer Methods for Partial Differential Equations,* Lehigh University, Bethlehem, Pennsylvania, June 17-19, 1975, pp. 328-334.

17b Mattis, R. L., and Buehler, M. G., *Semiconductor Measurement Technology:* A BASIC Program for Calculating Dopant Density Profiles from Capacitance-Voltage Data, NBS Spec. Publ. 400-11 (June 1975).

18b Li, S. S., *Semiconductor Measurement Technology:* The Dopant Density and Temperature Dependence of Electron Mobility and Resistivity in N-Type Silicon, NBS Spec. Publ. 400-33 (March 1977).

19b Buehler, M. G., and Thurber, W. R., Measurement of the Resistivity of a Thin Square Sample with a Square Four-Probe Array, *Solid-State Electronics* 20, 403-406 (1977).

20b Ehrstein, J. R., Effect of Specimen Preparation on the Calibration and Interpretation of Spreading Resistance Measurements, *Semiconductor Silicon/1977,* H. R. Huff and E. Sirtl, Eds., pp. 377-386 (Electrochemical Society, Princeton, N.J., 1977).

21b Li, S. S., and Thurber, W. R., The Dopant Density and Temperature Dependence of Electron Mobility and Resistivity in *n*-Type Silicon, *Solid-State Electronics* 20, 609-616 (1977).

22b Mattis, R. L., and Buehler, M. G., A New Method for Calculating Background Dopant Density from p-n Junction Capacitance-Voltage Measurements, *J. Electrochem. Soc.* 124, 1918-1923 (1977).

23b Blackburn, D. L., and Larrabee, R. D., Automated Photovoltaic Technique for Nondestructively Measuring Resistivity Variations of High Resistivity Silicon Wafers, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 168-179 (Electrochemical Society, Princeton, N.J., 1978).

24b Larrabee, R. D., Interpretation of Hall Measurements, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 71-76 (Electrochemical Society, Princeton, N.J., 1978).

25b Thurber, W. R., Mattis, R. L., and Liu, Y. M., Resistivity-Dopant Density Relationship for Silicon, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 81-92 (Electrochemical Society, Princeton, N.J., 1978).

C27b Li, S. S., The Dopant Density and Temperature Dependence of Hole Mobility and Resistivity in Boron Doped Silicon, *Solid-State Electronics* 21, 1109-1117 (1978).

N29b Gilsinn, D., and Kraft, R., *Semiconductor Measurement Technology:* DISTRIB I, An Impurity Redistribution Computer Program, NBS Spec. Publ. 400-57 (February 1979).

C30b Goldsmith, N., and Mayer, A., High-Speed Spreading Resistance Probe, NBS-GCR-79-166 (March 1979).

31b Dickey, D. H., and Ehrstein, J. R., *Semiconductor Measurement Technology:* Spreading Resistance Analysis for Silicon Layers with Nonuniform Resistivity, NBS Spec. Publ. 400-48 (May 1979).

C33b Li, S. S., *Semiconductor Measurement Technology:* The Theoretical and Experimental Study of the Temperature and Dopant Density Dependence of Hole Mobility, Effective Mass, and Resistivity in Boron-Doped Silicon, NBS Spec. Publ. 400-47 (November 1979).

36b Thurber, W. R., A Comparison of Measurement Techniques for Determining Phosphorus Densities in Semiconductor Silicon, *J. Electron. Mater.* 9, 551-560 (March 1980).

38b Larrabee, R. D., Interpretation of Hall Measurements, *J. Electrochem. Soc.* 127, 1640-1643 (July 1980).

39b Thurber, W. R., Mattis, R. L., Liu, Y. M., and Filliben, J. J., Resistivity-Dopant Density Relationship for Phosphorus-Doped Silicon, *J. Electrochem. Soc.* 127, 1807-1812 (1980).

40b Larrabee, R. D., Thurber, W. R., and Bullis, W. M., *Semiconductor Measurement Technology:* A FORTRAN Program for Calculating the Electrical Properties of Extrinsic Silicon, NBS Spec. Publ. 400-63 (October 1980).

41b Larrabee, R. D., and Blackburn, D. L., Theory and Application of a Nondestructive Photovoltaic Technique for the Measurement of Resistivity Variations in Circular Semiconductor Slices, *Solid-State Electronics* 23, 1059-1068 (1980).

42b Albers, J. H., Continuum Formulation of Spreading Resistance Correction Factors, *J. Electrochem. Soc.* 127, 2259-2263 (1980).

43b Thurber, W. R., Mattis, R. L., Liu, Y. M., and Filliben, J. J., Resistivity-Dopant Density Relationship for Boron-Doped Silicon, *J. Electrochem. Soc.* 127, 2291-2294 (1980).

44b Albers, J. H., Comparison of Spreading Resistance Correction Factor Algorithms Using Model Data, *Solid-State Electronics* 23, 1197-1205 (1980).

c. Defects and Impurities; Carrier Lifetime

14c Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon p-n Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, Eds., pp. 549-560 (Electrochemical Society, Princeton, New Jersey, 1973.)

17c Buehler, M. G., *Semiconductor Measurement Technology:* Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements - Videotape Script, NBS Spec. Publ. 400-26 (April 1976).

18c Buehler, M. G., and Phillips, W. E., A Study of the Gold Acceptor in a Silicon p^+n Junction and an n-type MOS Capacitor by Thermally Stimulated Current and Capacitance Measurements, *Solid-State Electronics* 19, 777-788 (1976).

C19c Goodman, A. M., *Semiconductor Measurement Technology:* Safe Operation of Capacitance Meters Using High Applied-Bias Voltage, NBS Spec. Publ. 400-34 (December 1976).

C20c Goodman, A. M., Safe Operation of Capacitance Meters Using High Applied-Bias Voltage, *RCA Rev.* 37, 491-514 (1976).

C21c Goodman, A. M., *Semiconductor Measurement Technology:* Suppression of Premature Dielectric Breakdown for High-Voltage Capacitance Measurements, NBS Spec. Publ. 400-37 (July 1977).

C22c Goodman, A. M., *Semiconductor Measurement Technology:* A 25-kV Bias-Isolation Unit for 1-MHz Capacitance and Conductance Measurements, NBS Spec. Publ. 400-40 (September 1977).

C23c Goodman, A. M., Suppression of Premature Dielectric Breakdown for High-Voltage Capacitance Measurements, *RCA Rev.* 38, 436-442 (1977).

C24c Goodman, A. M., A 25-kV Bias-Isolation Unit for 1-MHz Capacitance and Conductance Measurements, *RCA Rev.* 38, 512-532 (1977).

C25c Kuczer, P., Hook, H. O., and Goodman, A. M., *Semiconductor Measurement Technology:* A Versatile High-Voltage Bias Supply for Extended Range MIS C(V) and G(V) Measurements, NBS Spec. Publ. 400-41 (December 1977).

C26c Kuczer, P., Hook, H. O., and Goodman, A. M., A Versatile High-Voltage Bias Supply for Extended Range MIS C(V) and G(V) Measurements, *RCA Rev.* 39, 309-339 (1978).

27c Koyama, R. Y., Wafer Mapping of Electrically Active Defects, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 220-228 (Electrochemical Society, Princeton, N.J., 1978).

28c Koyama, R. Y., Techniques for Characterizing Defects in Starting Silicon Wafers Using TSM, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 53-60 (Electrochemical Society, Princeton, N.J., 1978).

30c Myers, D. R., and Phillips, W. E., Existence of an Isotope Shift for the Sulfur Deep Level in Silicon, *Appl. Phys. Letters* 32, 756-758 (1978).

31c Koyama, R. Y., Phillips, W. E., Myers, D. R., Liu, Y. M., and Dietrich, H. B., The Energy Levels and the Defect Signature of Sulfur-Implanted Silicon by Thermally Stimulated Measurements, *Solid-State Electronics* 21, 953-955 (1978).

R32c Larrabee, R. D., "X" Levels in Indium-Doped Silicon, *Proc. IRIS Specialty Group Meeting,* Annapolis, Maryland, June 13-15, 1978, pp. 253-261.

C33c Goodman, A. M., Extended Range MIS C(V) Measurement, A Technique for Monitoring Semiconductor Device Processing, NBS-GCR-78-155 (January 1979).

C35c Johnson, N. M., Bartelink, D. J., Gold, R. B., and Gibbons, J. F., Constant-Capacitance DLTS Measurement of Defect-Density Profiles in Semiconductors, *J. Appl. Phys.* 50, 4828-4833 (1979).

36c Koyama, R. Y., and Buehler, M. G., Novel Variable-Temperature Controllable Chuck for Use in the Detection of Deep Levels in Processed Semiconductor Wafers, *Rev. Sci. Instrum.* 50, 983-987 (1979).

R37c Larrabee, R. D., and Thurber, W. R., Temperature Dependence of the Responsivity of Indium-Doped Silicon Infrared Detectors, NBSIR 79-1786R (August 1979).

38c Myers, D. R., and Phillips, W. E., Observation of Unequal Densities for Sulfur Defects in Silicon Predeposited by Low Fluence Ion Implantation, *J. Electron. Mater.* 8, 781-788 (1979).

39c Phillips, W. E., Koyama, R. Y., and Buehler, M. G., Suppression of Measurement Interferences from Interface States and Mobile Ions in Thermally Stimulated Current Measurements in an MOS Capacitor, *J. Electrochem. Soc.* 126, 1979-1981 (1979).

40c Myers, D. R., Koyama, R. Y., and Phillips, W. E., An Implantation Predeposition Technique for the Introduction of Deep-Level Chemical Impurities, *Proc. Ion Beam Modification of Mater. Conf.*, Budapest, Hungary, September 4-8, 1978, pp. 439-448.

41c Myers, D. R., Koyama, R. Y., and Phillips, W. E., An Implantation Predeposition Technique for the Introduction of Deep-Level Chemical Impurities, *Radiat. Eff.* 48, 145-150 (1980).

d. Physical Analysis Techniques

C1d Duffy, M. T., Zanzucchi, P. J., and Cullen, G. W., Method to Determine Quality of Sapphire, NBS-GCR-76-61 (September 1975).

C2d Johannessen, J. S., Spicer, W. E., and Strausser, Y. E., Phase Separation in Silicon Oxides as Seen by Auger Electron Spectroscopy, *Appl. Phys. Letters* 27, 452-454 (1975).

3d Lieberman, A. G., Problems in Using Surface Analysis Techniques for the Depth Profiling of Microelectronic Materials, *Tech. Digest, 1975 International Electron Devices Meeting*, Washington, D. C., December 1-3, 1975, pp. 126-129.

C4d Johannessen, J. S., Chemical Shifts of Auger Lines Seen in SiO_x and SiO_2-Si Interfaces, *Faraday Discuss. Chem. Soc.* 60, 306-309 (1975).

C5d Johannessen, J. S., Electron Beam Effects in AES of Silicon Oxides, *Faraday Discuss. Chem. Soc.* 60, 313-316 (1975).

C6d Johannessen, J. S., Spicer, W. E., and Strausser, Y. E., A Study of the Chemical Composition of MOS and MNOS Structures by Auger Electron Spectroscopy, *Thin Solid Films* 32, 311-314 (1976).

7d Lieberman, A. G., Introductory Concepts for Silicon Surface Analysis, *Semiconductor Measurement Technology:* ARPA/NBS Workshop IV, Surface Analysis for Silicon Devices, NBS Spec. Publ. 400-23 (March 1976), pp. 3-6.

C8d Johannessen, J. S., Spicer, W. E., and Strausser, Y. E., Use of Auger Electron Spectroscopy to Determine the Structure of Silicon Oxide Films, *Semiconductor Measurement Technology:* ARPA/NBS Workshop IV, Surface Analysis for Silicon Devices, NBS Spec. Publ. 400-23 (March 1976), pp. 119-123.

C9d Strausser, Y. E., and Johannessen, J. S., An Auger Electron Spectroscopy Study of Silicon Spectra from Silicon Monoxide, Silicon Dioxide, and Silicon Nitride, *Semiconductor Measurement Technology:* ARPA/NBS Workshop IV, Surface Analysis for Silicon Devices, NBS Spec. Publ. 400-23 (March 1976), pp. 125-138.

C10d Johannessen, J. S., Spicer, W. E., and Strausser, Y. E., Auger Depth Profiling of Interfaces in MOS and MNOS Structures, *J. Vac. Sci. Technol.* 13, 849-855 (1976).

C11d Johannessen, J. S., Spicer, W. E., and Strausser, Y. E., An Auger Analysis of the SiO_2-Si Interface, *J. Appl. Phys.* 47, 3028-3037 (1976).

C13d Taylor, N. J., Johannessen, J. S., and Spicer, W. E., Crater-Edge Profiling in Interface Analysis Employing Ion-Beam Etching and AES, *Appl. Phys. Letters* 29, 497-499 (1976).

C14d Dobrott, R. D., Keenan, J. A., and Larrabee, G. B., Ion Microprobe Analysis of Integrated Circuit Structures, *15th Annual Proceedings, Reliability Physics 1977,* Las Vegas, Nevada, April 12-14, 1977, pp. 54-60.

C15d Johannessen, J. S., Helms, C. R., Spicer, W. E., and Strausser, Y. E., Auger Depth Profiling of MNOS Structures by Ion Sputtering, *IEEE Trans. Electron Devices* ED-24, 547-551 (1977).

C16d Helms, C. R., Garner, C. M., Miller, J., Lindau, I., Schwarz, S., and Spicer, W. E., Studies of Si/SiO_2 Interfaces by Auger Sputter Profiling and Photoelectron Spectroscopy Using Synchrotron Radiation, *Proc. 7th Intern. Vac. Congr. & 3rd Intern. Conf. Solid Surfaces,* Vienna, September 1977, pp. 2241-2243.

C17d Spicer, W. E., Lindau, I., and Helms, C. R., Frontiers in Surface and Interface Analysis, *R/D: Research/Development* 28 (12), 20-31 (December 1977).

C18d Grunthaner, F. J., and Maserjian, J., Experimental Observations of the Chemistry of the SiO_2/Si Interface, *IEEE Trans. Nucl. Sci.* NS-24 (6) 2108-2112 (December 1977).

N18½d Erickson, N. E., ESCA Studies of Clean Si (111) Surfaces, *Physica Scripta* 16, 462-465 (1977).

C19d Zanzucchi, P. J., Duffy, M. T., and Alig, R. C., Optical Reflectance Method for Determining Surface Quality of Sapphire, *J. Electrochem. Soc.* 125, 299-305 (1978).

20d Thurber, W. R., and Carpenter, B. S., Boron Determination in Silicon by the Nuclear Track Technique, *J. Electrochem. Soc.* 125, 654-657 (1978).

C21d Helms, C. R., Spicer, W. E., and Johnson, N. M., New Studies of the Si-SiO_2 Interface Using Auger Sputter Profiling, *Solid State Communications* 25, 673-676 (1978).

C22d Schwarz, S. A., Helms, C. R., and Spicer, W. E., High Resolution Auger Sputter Profiling Study of the Effect of Phosphorus Pileup on the Si-SiO_2 Interface Morphology, *J. Vac. Sci. Technol.* 15, 227-230 (1978).

C23d Helms, C. R., Strausser, Y. E., and Spicer, W. E., Observation of an Intermediate Chemical State of Silicon in the Si-SiO_2 Interface by Auger Sputter Profiling, *Appl. Phys. Letters* 33, 767-769 (1978).

C24d Strausser, Y. E., and Majumder, K. S., Chemical Structure of the Al/SiO_2 Interface, *J. Vac. Sci. Technol.* 15, 238-239 (1978).

C25d Christou, A., *Semiconductor Measurement Technology:* Automated Low-Energy Electron Probe (ASLEEP) for Semiconductor Wafer Diagnostics, NBS Spec. Publ. 400-30 (April 1978).

C26d Grunthaner, F. J., and Maserjian, J., Chemical Structure of the Transitional Region of the SiO_2/Si Interface, *The Physics of SiO_2 and Its Interfaces,* S. T. Pantelides, Ed., pp. 389-395 (Pergamon Press, New York, 1978).

C27d Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Auger Sputtering Profiling Studies of the Si-SiO_2 Interface, *The Physics of SiO_2 and Its Interfaces,* S. T. Pantelides, Ed., pp. 366-372 (Pergamon Press, New York, 1978).

C28d Cristou, A., Nelson, G., Jenkins, W., Davey, J. E., and Wilkens, N., Characterization of Semiconductor Wafer Defects by ASLEEP, SEM, and Scanning AES, *Scanning Electron Microscopy/1978,* Vol. 1, O'Hare, Illinois, April 17-21, 1978, pp. 273-282.

C29d Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Auger Sputter Profiling Studies of the Si-SiO_2 Interface, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3,

P. A. Barnes and G. A. Rozgonyi, Eds., pp. 136-138 (Electrochemical Society, Princeton, N.J., 1978).

C30d Zanzucchi, P. J., and Duffy, M. J., Surface Damage and the Optical Reflectance of Single-Crystal Silicon, *Appl. Optics* 17, 3477-3481 (1978).

C31d Larrabee, G., and Dobrott, R., Techniques for the Preparation and Analysis of Standard Silicon Semiconductor Specimens for the Ion Microprobe Mass Analyzer, NBS-GCR-79-158 (January 1979).

C32d Helms, C. R., Morphology and Electronic Structure of Si-SiO_2 Interfaces and Si Surfaces, *J. Vac. Sci. Technol.* 16, 608-614 (1979).

C33d Schwarz, S. A., and Helms, C. R., Model of Ion Knock-On Mixing with Application to Si-SiO_2 Interface Studies, *J. Vac. Sci. Technol.* 16, 781-783 (1979).

C35d Schwarz, S. A., and Helms, C. R., A Statistical Model of Sputtering, *J. Appl. Phys.* 50, 5492-5499 (1979).

C36d Grunthaner, F. J., Grunthaner, P. J., Vasquez, R. P., Lewis, B. F., Maserjian, J., and Madhukar, A., Local Atomic and Electronic Structure of Oxide/GaAs and SiO_2/Si Interfaces Using High-Resolution XPS, *J. Vac. Sci. Technol.* 16, 1443-1453 (1979).

C37d Grunthaner, F. J., Grunthaner, P. J., Vasquez, R. P., Lewis, B. F., Maserjian, J., and Madhukar, A., High-Resolution X-Ray Photoelectron Spectroscopy as a Probe of Local Atomic Structure: Application to Amorphous SiO_2 and the Si-SiO_2 Interface, *Phys. Rev. Letters* 43, 1683-1686 (1979).

C38d Duffy, M. T., Zanzucchi, P. J., Ham, W. E., Corboy, J. F., and Cullen, G. W., *Semiconductor Measurement Technology:* Method to Determine the Quality of Sapphire, NBS Spec. Publ. 400-62 (August 1980).

C41d Wilson, R. G., and Weglein, R. D., Acoustic Material Signatures Using the Reflection Acoustic Microscope, *Ultrasonic Mater. Characterization,* H. Berger and M. Linzer, Co-Editors, NBS Spec. Publ. 596 (November 1980), pp. 345-355.

C42d Vasquez, R. P., and Grunthaner, F. J., Intensity Analysis of XPS Spectra to Determine Oxide Uniformity: Application to SiO_2/Si Interfaces, *Surface Science* 99, 681-688 (1980).

e. Wafer Processing

C2e Wilson, R. G., Planar and Axial Channeling of 800 keV As in <110> Silicon, *Appl. Phys. Letters* 29, 770-772 (1976).

3e Novotny, D. B., Photoresist Exposure - Measurement and Control, *Proc. Soc. Photo-Optical Instrum. Engrs.* 80, *Developments in Semiconductor Microlithography*, 9-13 (1976).

C4e Tressler, R. E., Stach, J., and Metz, D., Gas Phase Composition Considerations in the Thermal Oxidation of Silicon in Cl-H-O Ambients, *J. Electrochem. Soc.* 124, 607-609 (1977).

C6e Wilson, R. G., Dunlap, H. L., and Jamba, D. M., Angular Sensitivity of Controlled Implanted Doping Profiles, *Semiconductor Silicon/1977*, H. R. Huff and E. Sirtl, Eds., pp. 1023-1034 (Electrochemical Society, Princeton, N.J., 1977).

C7e Jamba, D. M., *Semiconductor Measurement Technology:* Some Aspects of Dose Measurement for Accurate Ion Implantation, NBS Spec. Publ. 400-39 (July 1977).

8e Novotny, D. B., Sensitometry of Photoresists for Microelectronics, *Photographic Science and Engineering* 21, 351-355 (1977).

C12e Jamba, D. M., Secondary Particle Collection in Ion Implantation Dose Measurement, *Rev. Sci. Instrum.* 49, 634-638 (1978).

C13e Strausser, Y. E., Scheibner, E. J., and Johannessen, J. S., Observations of Al_2O_3 and Free Silicon in the Interface Between Aluminum Films and SiO_2, *Thin Solid Films* 52, 203-214 (1978).

C14e Johannessen, J. S., Spicer, W. E., Gibbons, J. F., Plummer, J. D., and Taylor, N. J., Observation of Phosphorus Pile-Up at the SiO_2-Si Interface, *J. Appl. Phys.* 49, 4453-4458 (1978).

15e Wilson, R. G., Dunlap, H. L., Jamba, D. M., and Myers, D. R., *Semiconductor Measurement Technology:* Angular Sensitivity of Controlled Implanted Doping Profiles, NBS Spec. Publ. 400-49 (November 1978).

C16e Stach, J., Das, M. B., and Tressler, R. E., Development of Measurement Techniques for Monitoring Chemical Purity of Materials Used in Digital IC Processing, NBS-GCR-78-134 (September 1978).

17e Leedy, T. F., and Liu, Y. M., *Semiconductor Measurement Technology:* Microelectronic Processing Laboratory at NBS, NBS Spec. Publ. 400-53 (December 1978).

20e Myers, D. R., and Wilson, R. G., Alignment Effects on Implantation Profiles in Silicon, *Proc. Ion Beam Modification of Mater. Conf.*, Budapest, Hungary, September 4-8, 1978, pp. 103-111.

C21e Wilson, R. G., and Comas, J., Correlation of Atomic Distribution and Implantation Induced Damage Profiles in Be-Ion Implanted Silicon, *Proc. Ion Beam Modification of Mater. Conf.*, Budapest, Hungary, September 4-8, 1978, pp. 547-556.

C22e Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Studies of the Effect of Oxidation Time and Temperature on the Si-SiO_2 Interface using Auger Sputter Profiling, *J. Appl. Phys.* 50, 7007-7014 (1979).

23e Myers, D. R., Wilson, R. G., and Comas, J., Considerations of Ion Channeling for Semiconductor Microstructure Fabrication, *J. Vac. Sci. Technol.* 16, 1893-1896 (1979).

24e Albers, J. H., and Novotny, D. B., Intensity Dependence of Photochemical Reaction Rates for Photoresists, *J. Electrochem. Soc.* 127, 1400-1403 (1980).

25e Myers, D. R., and Wilson, R. G., Alignment Effects on Implantation Profiles in Silicon, *Radiat. Eff.* 47, 91-94 (1980).

C27e Comas, J., and Wilson, R. G., Channeling and Random Equivalent Depth Distributions of 150 keV Li, Be, and B Implanted in Silicon, *J. Appl. Phys.* 51, 3697-3701 (1980).

C28e Wilson, R. G., Atom and Carrier Depth Distribution for 300 keV Arsenic Channelled in the <110> of Silicon as a Function of Alignment Angle and Ion Fluence, *Radiat. Eff. Lett.* 57, 109-113 (1980).

29e Novotny, D. B., Experimental Photoresist Sensitometry and Exposure Modeling, *Proc. Soc. Photo-Optical Instrum. Engrs.* 221, *Semiconductor Microlithography V,* 184-193 (1980).

C30e Wilson, R. G., and Comas, J., Correlation of Atomic Distribution and Implantation Induced Damage Profiles in Be-Ion Implanted Si, *Radiat. Eff.* 47, 137-142 (1980).

f. Micrometrology

1f Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Proc. Soc. Photo-Optical Instrum. Engrs.* 55, *Photofabrication Imagery,* 84-89 (1975).

N2f Jerke, J. M., *Semiconductor Measurement Technology:* Optical and Dimensional-Measurement Problems with Photomasking in Microelectronics, NBS Spec. Publ. 400-20 (October 1975).

N3f Swyt, D. A., NBS Program in Photomask Linewidth Measurements, *Solid State Technology* 19 (4), 55-61 (April 1976).

C4f Kasdan, H. L., and George, N., Linewidth Measurement by Diffraction Pattern Analysis, *Proc. Soc. Photo-Optical Instrum. Engrs.* 80, *Developments in Semiconductor Microlithography,* 54-63 (1976).

N5f Swing, R. E., The Theoretical Basis of a New Optical Method for the Accurate Measurement of Small Line-Widths, *Proc. Soc. Photo-Optical Instrum. Engrs.* 80, *Developments in Semiconductor Microlithography,* 65-77 (1976).

N6f Jerke, J. M., Hartman, A. W., Nyyssonen, D., Rosberry, F. W., Swing, R. E., Swyt, D. A., and Young, R. D., Accurate Line-Width Measurements at the National Bureau of Standards, *Proc. Microelectronics Seminar - Interface '76,* Monterey, California,

7f Jerke, J. M., Hartman, A. W., Nyyssonen, D., Swing, R. E., Young, R. D., and Keery, W. E., Comparison of Linewidth Measurements on an SEM/Interferometer System and an Optical Linewidth-Measuring Microscope, *Proc. Soc. Photo-Optical Instrum. Engrs.* 100, *Developments in Semiconductor Microlithography II,* 37-45 (1977).

N9f Young, R. D., Length Calibrations in the Micrometer and Sub-Micrometer Range, *Ann. CIRP* 25, 245-250 (1977).

N10f Nyyssonen, D., Linewidth Measurement with an Optical Microscope: The Effect of Operating Conditions on the Image Profile, *Appl. Optics* 16, 2223-2230 (1977).

N11f Swyt, D. A., and Rosberry, F. W., A Comparison of Some Optical Microscope Measurements of Photomask Linewidths, *Solid State Technology* 20 (8), 70-75 (August 1977).

N12f Swyt, D. A., Rosberry, F. W., and Nyyssonen, D., Calibration of Optical Microscopes for Photomask Linewidth Measurements, *Proc. Microelectronics Seminar - Interface '77,* Monterey, California, October 5-7, 1977, pp. 131-144.

N13f Swyt, D. A., An NBS Physical Standard for the Calibration of Photomask Linewidth Measuring Systems, *Proc. Soc. Photo-Optical Instrum. Engrs.* 129, *Effective Utilization of Optics in Quality Assurance,* 98-105 (1977).

N14f Swyt, D. A., Design of a Pattern on a Photomask-Like Physical Standard for Evaluation and Calibration of Linewidth-Measuring Systems, *Solid State Technology* 21 (1), 35-42 (January 1978).

15f Novotny, D. B., and Ciarlo, D. R., *Semiconductor Measurement Technology:* Automated Photomask Inspection, NBS Spec. Publ. 400-46 (April 1978).

16f Nyyssonen, D., Optical Linewidth Measurements on Wafers, *Proc. Soc. Photo-Optical Instrum. Engrs.* 135, *Developments in Semiconductor Microlithography III,* 115-119 (1978).

17f Novotny, D. B., and Ciarlo, D. R., Automated Photomask Inspection, *Solid State Technology* 21 (5), 51-59, 76 (May 1978) and 21 (6), 59-67 (June 1978).

19f Swyt, D. A., Rosberry, F. W., and Nyyssonen, D., Photomask Linewidth Measurement, *Circuits Manufacturing* 18 (9), 20 ff (September 1978).

21f Nyyssonen, D., and Jerke, J. M., Linewidth Measurement: From Fine Art to Science, *Tech. Digest, 1978 Internat. Electron Devices Meeting*, Washington, D. C., December 4-6, 1978, pp. 437-440.

22f Nyyssonen, D., and Jerke, J. M., Optical Linewidth Measurement - A Basic Understanding, *Proc. Microelectronic Measurement Technology Seminar*, San Jose, California, February 6-7, 1979, pp. 251-266.

23f Nyyssonen, D., Spatial Coherence: The Key to Accurate Optical Micrometrology, *Proc. Soc. Photo-Optical Instrum. Engrs.* 194, *Applications of Optical Coherence*, 34-44 (1979).

24f Jerke, J. M., Ed., *Semiconductor Measurement Technology:* Accurate Linewidth Measurements on Integrated-Circuit Photomasks, NBS Spec. Publ. 400-43 (February 1980).

25f Nyyssonen, D., Linewidth Measurement Spotlight, *Semiconductor International* 3 (3), 39-56 (March 1980).

C26f Kasdan, H. L., Linewidth Measurement by Diffraction Pattern Analysis, NBS GCR-79-175 (April 1980).

27f Nyyssonen, D., Calibration of Optical Systems for Linewidth Measurements on Wafers, *Proc. Soc. Photo-Optical Instrum. Engrs.* 221, *Semiconductor Microlithography V*, 119-126 (1980).

g. Test Structures

1g Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974).

C2g Steigerwalt, S. T., and Lagnado, I., The CCD as a Test Structure for Semiconductor Process Control, *Microelectronics J.* 7, 23-29 (1975).

3g Buehler, M. G., David, J. M., Mattis, R. L., Phillips, W. E., and Thurber, W. R., *Semiconductor Measurement Technology:* Planar Test Structures for Characterizing Impurities in Silicon, NBS Spec. Publ. 400-21 (December 1975).

4g Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, NBS Spec. Publ. 400-22 (May 1976).

5g Buehler, M. G. and Thurber, W. R., A Planar Four-Probe Test Structure for Measuring Bulk Resistivity, *IEEE Trans. Electron Devices* ED-23, 968-974 (1976).

6g Galloway, K. F., and Buehler, M. G., The Application of Test Structures and Test Patterns to the Development of Radiation Hardened Integrated Circuits: A Review, NBSIR 76-1093 (August 1976).

7g Buehler, M. G., and Sawyer, D. E., Microelectronic Test Patterns for Use in Procuring Reliable, Custom Integrated Circuit Chips, *1976 Government Microcircuit Applications Conference Digest of Papers*, Orlando, Florida, November 9-11, 1976, pp. 62-65.

8g Buehler, M. G., and Sawyer, D. E., Microelectronic Test Patterns Aid Production of Custom ICs, *Circuits Manufacturing* 17 (2), 46-56 (February 1977).

9g David, J. M., and Buehler, M. G., A Numerical Analysis of Various Cross Sheet Resistor Test Structures, *Solid-State Electronics* 20, 539-543 (1977).

10g Buehler, M. G., Microelectronic Test Patterns for Use in Procuring Custom and Highly Reproducible Integrated Circuits, *Proc. Symposium on Utilization of LSICs in Military Systems*, Arlington, Virginia, August 9-11, 1977, pp. III 102-III 117.

11g Russell, T. J., Leedy, T. F., and Mattis, R. L., A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing, *Tech. Digest, International Electron Devices Meeting*, Washington, D.C., December 5-7, 1977, pp. 7A-7F.

C12g Ham, W. E., Intrachip and Spatial Parametric Integrity - An Important Part of IC Process Characterization, *Tech. Digest, International Electron Devices Meeting*, Washington, D.C., December 5-7, 1977, pp. 406-409.

13g Buehler, M. G., Dopant Profiles Determined from Enhancement Mode MOSFET DC Measurements, *Appl. Phys. Letters* 31, 848-850 (1977).

14g Buehler, M. G., and Thurber, W. R., An Experimental Study of Various Cross Sheet Resistor Test Structures, *J. Electrochem. Soc.* 125, 645-650 (1978).

15g Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* 125, 650-654 (1978).

16g Thurber, W. R., and Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-4, NBS Spec. Publ. 400-32 (April 1978).

17g Buehler, M. G., Microelectronic Test Patterns for Use in Procuring LSICs, *Proc. Industry/Joint Services Automatic Test Conf. and Workshop,* San Diego, California, April 5-7, 1978, pp. 233-235.

18g Buehler, M. G., Limitations and Applications of the DC MOSFET Profile Method, *Semiconductor Characterization Techniques,* Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds., pp. 241-252 (Electrochemical Society, Princeton, N.J., 1978).

19g Mattis, R. L., and Doggett, M. R., A Microelectronic Test Pattern for Analyzing Automated Wafer Probing and Probe Card Patterns, *Solid State Technology* 21 (11), 76-79 (November 1978).

20g Russell, T. J., Maxwell, D. A., Reimann, C. T., and Buehler, M. G., A Microelectronic Test Pattern for Measuring the Uniformity of an Integrated Circuit Fabrication Technology, *Proc. Govt. Microcircuit Applications Conf.,* Monterey, California, November 14-16, 1978, pp. 33-36.

21g McCarthy, D., Acevedo, J., Stamps, B., Lonky, M., and Buehler, M. G., An Advanced Integrated Test Structure for High Speed Measurement of Generation Lifetime, *Proc. Govt. Microcircuit Applications Conf.,* Monterey, California, November 14-16, 1978, pp. 37-38.

23g Russell, T. J., Maxwell, D. A., Reimann, C. T., and Buehler, M. G., A Microelectronic Test Pattern for Measuring Uniformity of an Integrated Circuit Fabrication Technology, *Solid State Technology* 22 (2), 71-74 (February 1979).

24g Buehler, M. G., Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-Pad Array, *Proc. Microelectronics Measurement Technology Seminar,* San Jose, California, February 6-7, 1979, pp. 27-38.

25g Russell, T. J., and Maxwell, D. A., *Semiconductor Measurement Technology:* A Production-Compatible Microelectronic Test Pattern for Evaluating Photomask Misalignment, NBS Spec. Publ. 400-51 (April 1979).

27g Buehler, M. G., Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-Pad Array Approach, *Solid State Technology* 22 (10), 89-94 (October 1979).

28g Linholm, L. W., Carver, G. P., and Russell, T. J., The Use of Microelectronic Test Structures to Characterize IC Materials, Processes, and Processing Equipment, *Proc. Measurement Sci. Conf.,* San Luis Obispo, California, November 30 - December 1, 1979, pp. 129-150.

C29g Ham, W. E., *Semiconductor Measurement Technology:* Comprehensive Test Pattern and Approach for Characterizing SOS Technology, NBS Spec. Publ. 400-56 (January 1980).

30g Buehler, M. G., The D-C MOSFET Dopant Profile Method, *J. Electrochem. Soc.* 127, 701-704 (1980).

32g Carver, G. P., Linholm, L. W., and Russell, T. J., The Use of Microelectronic Test Structures to Characterize IC Materials, Processes, and Processing Equipment, *Solid State Technology* 23 (9), 85-92 (September 1980).

33g Buehler, M. G., The Use of Electrical Test Structure Arrays for Integrated Circuit Process Evaluation, *J. Electrochem. Soc.* 127, 2284-2290 (1980).

35g Buehler, M. G., Effect of the Drain-Source Voltage on Dopant Profiles Obtained from the d-c MOSFET Profile Methid, *IEEE Trans. Electron Devices* ED-27, 2273-2277 (1980).

h. Bonding and Packaging

11h Harman, G. G., Metallurgical Failure Modes of Wire Bonds, presented as part of a Workshop on Metallurgical Failure Modes, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, pp. 131-141.

12h Harman, G. G., A Metallurgical Basis for the Non-Destructive Bond Pull-Test, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, pp. 205-210.

14h Harman, G. G., The Use of Acoustic Emission in a Test for Beam Lead Bond Integrity, *14th Annual Proceedings, Reliability Physics 1976,* Las Vegas, Nevada, April 20-22, 1976, pp. 86-97.

15h Harman, G. G., The Use of Acoustic Emission in a Test for Beam-Lead, TAB, and Hybrid Chip Capacitor Bond Integrity, *IEEE Trans. Parts, Hybrids, and Packaging* PHP-13, 116-127 (1977).

16h Harman, G. G., and Albers, J., The Ultrasonic Welding Mechanism as Applied to Aluminum- and Gold-Wire Bonding on Microelectronics, *IEEE Trans. Parts, Hybrids, and Packaging* PHP-13, 406-412 (1977).

17h Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test - How to Use It, How to Abuse It, *Proc. 1978 IEEE Electronic Components Conference,* Anaheim, California, April 25, 1978, pp. 291-299.

18h Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test - How to Use It, How to Abuse It, *IEEE Trans. Components, Hybrids, and Manufacturing Technology* CHMT-1, 203-210 (1978).

20h Harman, G. G., *Semiconductor Measurement Technology:* Nondestructive Tests Used to Insure the Integrity of Semiconductor Devices, with Emphasis on Acoustic Emission Techniques, NBS Spec. Publ. 400-59 (September 1979).

i. Hermeticity; Moisture Measurement

3i Ruthberg, S., Neff, G. R., and Martin, B. D., Radioisotope Hermetic Test Precision, *Proc. 1977 Internat. Microelectronics Symp.*, Baltimore, Maryland, October 24-26, 1977, pp. 131-137.

C4i Sulouff, R. E., A Study of Leak Rate Versus Reliability of Hybrid Packages, *Proc. 1978 Internat. Microelectronics Symp.*, Minneapolis, Minnesota, September 25-27, 1978, pp. 121-124.

C5i Sulouff, R. E., Investigation of Moisture Measurement, Failure Rate, and Leak Rate and Study of Moisture Infusion, NBS-GCR-79-170 (August 1979).

j. Device Inspection and Test

4j Sawyer, D. E., and Berning, D. W., Laser Scanning of Active Semiconductor Devices, *Tech. Digest, 1975 International Electron Devices Meeting*, Washington, D.C., December 1-3, 1975, pp. 111-114.

5j Sawyer, D. E., and Berning, D. W., *Semiconductor Measurement Technology:* Laser Scanning of Active Semiconductor Devices - Videotape Script, NBS Spec. Publ. 400-27 (February 1976).

6j Sawyer, D. E., and Berning, D. W., Laser Scanning of MOS IC's Reveals Internal Logic States Nondestructively, *Proc. IEEE* 64, 393-394 (1976).

7j Galloway, K. F., Leedy, K. O., and Keery, W. J., Electron-Beam-Induced Currents in Simple Device Structures, *Proc. 26th Electronic Components Conf.*, San Francisco, California, April 26-28, 1976, pp. 257-262.

8j Keery, W. J., Leedy, K. O., and Galloway, K. F., Electron Beam Effects on Microelectronic Devices, *Scanning Electron Microscopy/1976*, Toronto, April 5-9, 1976, pp. 507-514.

9j Galloway, K. F., Leedy, K. O., and Keery, W. J., Electron-Beam-Induced Currents in Simple Device Structures, *IEEE Trans. Parts, Hybrids, and Packaging* PHP-12, 231-236 (1976).

10j Sawyer, D. E., and Berning, D. W., Thermal Mapping of Transistors With a Laser Scanner, *Proc. IEEE* 64, 1634-1635 (1976).

11j Sawyer, D. E., and Berning, D. W., Mapping Nonlinearities Over the Active Regions of Semiconductor Devices, *Proc. IEEE* 64, 1635-1637 (1976).

C12j Kern, W., and Comizzoli, R. B., New Methods for Detecting Structural Defects in Glass Passivation Films, *J. Vac. Sci. Technol.* 14, 32-39 (1977).

13j Leedy, K. O., A Bibliography on Electron Beam Induced Current Analysis of Semiconductor Devices, *Solid State Technology* 20 (2), 45-48 (February 1977).

14j Sawyer, D. E., and Berning, D. W., *Semiconductor Measurement Technology:* A Laser Scanner for Semiconductor Devices, NBS Spec. Publ. 400-24 (February 1977).

C15j Kern, W., and Comizzoli, R. B., *Semiconductor Measurement Technology:* Techniques for Measuring the Integrity of Passivation Overcoats on Integrated Circuits, NBS Spec. Publ. 400-31 (March 1977).

16j Devaney, J. R., Leedy, K. O., and Keery, W. J., *Semiconductor Measurement Technology:* Notes on SEM Examination of Microelectronic Devices, NBS Spec. Publ. 400-35 (April 1977).

C17j Weglein, R. D., Wilson, R. G., and Bonnell, D. M., Scanning Acoustic Microscopy - Application to Fault Detection, *15th Annual Proceedings, Reliability Physics 1977,* Las Vegas, Nevada, April 12-14, 1977, pp. 37-43.

C18j Quate, C. F., A Scanning Acoustic Microscope, *Semiconductor Silicon/1977,* H. R. Huff and E. Sirtl, Eds., pp. 422-430 (Electrochemical Society, Princeton, N.J., 1977).

C19j Wilson, R. G., Weglein, R. D., and Bonnell, D. M., Scanning Acoustic Microscopy for Integrated Circuit Diagnostics, *Semiconductor Silicon/1977,* H. R. Huff and E. Sirtl, Eds., pp. 431-440 (Electrochemical Society, Princeton, N.J., 1977).

21j Sawyer, D. E., Berning, D. W., and Lewis, D. C., Laser Scanning of Active Integrated Circuits and Discrete Semiconductor Devices, *Solid State Technology* 20 (6), 37-41, 48 (June 1977).

C22j Comizzoli, R. B., Nondestructive, Reverse Decoration of Defects in IC Passivation Overcoats, *J. Electrochem. Soc.* 124, 1087-1095 (1977).

C23j Kompfner, R., and Quate, C. F., Acoustic Radiation and Its Use in Microscopy, *Physics in Technology* 8, 231-237 (1977).

C24j Atalar, A., Quate, C. F., and Wickramasinghe, H. K., Phase Imaging in Reflection with the Acoustic Microscope, *Appl. Phys. Letters* 31, 791-793 (1977).

C25j Weglein, R. D., and Wilson, R. G., Image Resolution of the Scanning Acoustic Microscope, *Appl. Phys. Letters* 31, 793-796 (1977).

C27j Weglein, R. D., and Wilson, R. G., Characteristic Material Signatures by Acoustic Microscopy, *Electron. Lett.* 14, 352-354 (1978).

C28j Weglein, R. D., Gray Scale for Scanning Acoustic Microscopy, *Electron. Lett.* 14, 656-657 (1978).

C29j Atalar, A., An Angular-Spectrum Approach to Contrast in Reflection Acoustic Microscope, *J. Appl. Phys.* 49, 5130-5139 (1978).

C30j Weglein, R. D., and Wilson, R. G., An Acoustic Gray Scale for Scanning Acoustic Microscopy and Diagnostic Ultrasound, *Ultrasound Imaging* 1, 89-100 (1979).

C31j Weglein, R. D., A Model for Predicting Acoustic Material Signatures, *Appl. Phys. Letters* 34, 179-181 (1979).

C33j Quate, C. F., Atalar, A., and Wickramasinghe, H. K., Acoustic Microscopy with Mechanical Scanning - A Review, *Proc. IEEE* 67, 1092-1114 (1979).

C34j Quate, C. F., The Acoustic Microscope, *Sci. Am.* 241 (4), 62-70 (October 1979).

C36j Quate, C. F., Innovative Measurement Technology for the Semiconductor Device Industry — "The Acoustic Microscope — A New Instrument for Viewing Integrated Circuits," NBS GCR-80-204 (May 1980).

1. Radiation Effects

171 Galloway, K. F., Keery, W. J., and Leedy, K. O., Integrated Circuit Damage Resulting from SEM Examination, *Proc. 25th Electronic Components Conf.*, Washington, D.C., May 12-14, 1975, pp. 263-266.

C211 Goodman, A. M., and Weitzel, C. E., The Effect of Electron-Beam Aluminization on the Si-Sapphire Interface, *Appl. Phys. Letters* 31, 114-117 (1977).

241 Galloway, K. F., and Mayo, S., Radiation Dose at the Silicon-Sapphire Interface Due to Electron-Beam Aluminization, *J. Appl. Phys.* 49, 2586-2588 (1978).

251 Galloway, K. F., and Mayo, S., On the Compatibility of X-Ray Lithography and SOS Device Fabrication, *IEEE Trans. Electron Devices* ED-25, 549-550 (1978).

261 Galloway, K. F., VLSI Processing, Radiation, and Hardening, *IEEE Trans. Nucl. Sci.* NS-25, 1469-1472 (1978).

281 Galloway, K. F., and Mayo, S., Radiation Levels Associated with the Electron-Beam Metallization Process, *Solid State Technology* 22 (5), 96-100 (May 1979).

291 Galloway, K. F., VLSI Processing, Radiation and Hardening, *Semiconductor International* 2 (4), 65-73 (May 1979).

301 Galloway, K. F., Mayo, S., and Roitman, P., Radiation Levels Associated with Advanced Lithographic Techniques, *J. Electrochem. Soc.* 126, 2245-2248 (1979).

C32l Grunthaner, F. J., Lewis, B. F., Vasquez, R. P., Maserjian, J., and Madhukar, A., Reduced Oxidation States and Radiation-Induced Trap Generation at Si/SiO_2 Interface, *The Physics of MOS Insulators*, G. Lucovsky, S. T. Pantelides, and F. L. Galeener, Eds., pp. 290-295 (Pergamon Press, New York, 1980).

C33l Grunthaner, F. J., Lewis, B. F., Zamini, N., Maserjian, J., and Madhukar, A., XPS Studies of Structure-Induced Radiation Effects at the Si/SiO_2 Interface, *IEEE Trans. Nucl. Sci.* NS-27, 1640-1646 (1980).

n. Proceedings of Symposia and Workshops

2n Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, NBS Spec. Publ. 400-3 (February 1974).

3n Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, NBS Spec. Publ. 400-9 (December 1974).

5n Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop III. Test Patterns for Integrated Circuits, NBS Spec. Publ. 400-15 (January 1976).

6n Lieberman, A. G., *Semiconductor Measurement Technology:* ARPA/NBS Workshop IV. Surface Analysis for Silicon Devices, NBS Spec. Publ. 400-23 (March 1976).

o. Miscellaneous

C15o Rudenberg, H. G., Automated Integrated Circuit Processing and Assembly, NBS-GCR-76-64 (April 1975).

C16o Weglein, R. D., Acoustic Properties of Sputtered Glass at Microwave Frequencies, *Appl. Phys. Letters* 29, 277-279 (1976).

21o Bullis, W. M., The NBS Semiconductor Technology Program, *Proc. Symposium on Utilization of LSICs in Military Systems*, Arlington, Virginia, August 9-11, 1977, pp. III 87-III 101.

7. REFERENCES

1. Proceedings, Solid State Device Reliability Workshop, Warrenton, Virginia, July 24-28, 1972, NAVMAT Report SER 16-033.

2. Heilmeier, G. H., Reliability — Some Early Impressions of a Pentagon Newcomer, *10th Annual Proceedings, Reliability Physics 1972,* Las Vegas, Nevada, April 5-7, 1972, pp. 1-4.

3. Nossiter, B. D., Weapons Systems: A Story of Failure, *Washington Post,* January 26, 1969, p. A1.

4. *Ad Hoc* Committee on Materials and Processes for Electron Devices, Materials and Processes for Electron Devices, National Materials Advisory Board Publication NMAB-289, May 1972, p. 106.

5. Yield of Electronic Materials and Devices, National Materials Advisory Board Publication NMAB-290, July 1972.

6. Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511 (December 1969).

7. Oettinger, F. F., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1 to December 31, 1977, NBSIR 78-1474 (September 1978).

8. Oettinger, F. F., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1977 to September 30, 1978, NBSIR 79-1756 (June 1979).

9. Ehrstein, J. R., Two-Probe (Spreading Resistance) Measurements for Evaluation of Semiconductor Materials and Devices, *Nondestructive Evaluation of Semiconductor Materials and Devices,* J. N. Zemel, Ed., pp. 1-66 (Plenum Press, New York, 1979).

10. Koyama, R. Y., Detection of Deep Levels in High Power Semiconductor Materials and Devices, *NBS J. Res.* 83, 273-281 (1978).

11. Koyama, R. Y., and Buehler, M. G., *Semiconductor Measurement Technology:* A Wafer Chuck for Use Between -196 and 350°C, NBS Spec. Publ. 400-55 (January 1979).

12. Oettinger, F. F., and Larrabee, R. D., Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1978 to September 30, 1979, NBSIR 80-2061 (August 1980).

13. Forman, R. A., Optical Study of Isotopic Effects in the Sulfur Deep Level in Silicon, *Appl. Phys. Letters* 37, 776-778 (1 November 1980).

14. Nyyssonen, D., Optical Linewidth Measurements on Silicon and Iron-Oxide Photomasks, *Proc. Soc. Photo-Optical Instrum. Engrs.* 100, *Developments in Semiconductor Microlithography II,* 127-134 (1977).

15. Linholm, L. W., CMOS/SOS Test Patterns for Process Evaluation and Control: Annual Report, March 1 to November 1, 1978, NBSIR 79-1595 (January 1979).

16. Carver, G. P., and Buehler, M. G., An Analytical Expression for the Evaluation of Leakage Current in the Integrated Gated-Diode Electrometer, *IEEE Trans. Electron Devices* ED-27, 2245-2252 (1980).

17. Sawyer, D. E., and Kessler, H. K., Laser Scanning of Solar Cells for the Display of Cell Operating Characteristics and Detection of Cell Defects, *IEEE Trans. Electron Devices* ED-27, 864-872 (1980).

18. Harman, G. G., Ed., *Semiconductor Measurement Technology:* Microelectronic Ultrasonic Bonding, NBS Spec. Publ. 400-2 (January 1974).

19. Albers, J. H., Ed., *Semiconductor Measurement Technology:* The Destructive Bond Pull Test, NBS Spec. Publ. 400-18 (February 1976).

20. Ruthberg, S., A Rapid Cycle Method for Gross Leak Testing with the Helium Leak Detector, *IEEE Trans. Components, Hybrids, and Manufacturing Tech.* CHMT-3, 564-570 (1980).

21. Bullis, W. M., *Semiconductor Measurement Technology:* Metrology for Submicrometer Devices and Circuits, NBS Spec. Publ. 400-61 (May 1980).

22. Bullis, W. M., and Scace, R. I., The NBS Semiconductor Technology Program and VLSI, NBSIR 80-2057 (June 1980).

23. Standard Practice for Preparing High-Resistivity *n*-Type Silicon for Spreading Resistance Measurements (ASTM Designation F 674), *1980 Annual Book of ASTM Standards,* Part 43. See also Standard Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe (ASTM Designation F 672), *ibid.*

APPENDIX

Research Contracts Summary

Contract or Order No.	Organization	Title	Start	End	Approximate Cost (k$)
4-35807	A. D. Little, Inc.	Automated Integrated Circuit Processing and Assembly	2/ 7/74	5/31/75	37.9
502498*	Naval Electronics Laboratory Center	Investigate CCD Test Patterns for Application to Semiconductor Process Control	10/ 1/73	6/30/75	160.0
408726* 503183* 602156*	Lawrence Livermore Laboratory	Automated IC Photomask Inspection	1/ 1/74	3/ 1/77	215.0
4-35897 513840*	Hi-Rel Laboratories	Electron Microscope Failure Analysis Techniques	3/ 1/74	12/31/76	25.0
501718* 602542* 711782*	Naval Research Laboratories	The Generation and Qualification of an Automated Scanning Low Energy Electron Probe for Semiconductor Wafer and IC Diagnostics	8/ 2/74	9/30/77	165.0
5-35717	Pennsylvania State University	Development of Measurement Techniques for Monitoring Chemical Purity of Materials Used in Digital IC Processing	7/15/74	11/ 1/77	259.0
5-35880	Martin Marietta Aerospace	Hermeticity and Packaging - Moisture Measurements	4/ 3/75	9/25/78	140.1+
5-35881	Solecon Laboratories	Spreading Resistance Probe Calibration for Silicon	4/ 3/75	5/31/78	53.1
5-35890 702980*	Recognition Systems, Inc.	Quantitative Analysis of MAME-1 Performance	4/ 3/75	8/15/78	30.2
5-35891	Hughes Research Laboratories	Measurement Technology for Critical Implantation Parameters	4/14/75	9/30/80	234.8
5-35898	Hughes Research Laboratories	Scanning Acoustic Microscope Measurement Technology	4/14/75	3/31/79	392.7
5-35899	Stanford University	The Acoustic Microscope - A New Instrument for Viewing Integrated Circuits	9/ 1/75	3/31/79	307.0
5-35912	RCA Laboratories	Extended Range MIS C(V) Measurement - A Technique for Monitoring Semiconductor Device Processing	4/24/75	11/30/77	151.1
5-35913	RCA Laboratories	Development of Techniques for Measuring the Integrity of Passivation Overcoats on Integrated Circuits	4/24/75	1/14/77	67.0
5-35914	RCA Laboratories	Study of High Speed Spreading Resistance (Probe)	4/24/75	9/30/78	139.4
5-35915	RCA Laboratories	Method to Determine Quality of Sapphire	4/25/75	8/16/79	250.3
5-35916	RCA Laboratories	Test Pattern Design and Analysis for SOS/LSI	4/24/75	3/31/79	199.7
5-35917	Texas Instruments Incorporated	Development of Techniques for the Preparation and Analysis of Standard Silicon Semiconductor Specimens for Ion Microprobe Mass Analyzer	4/30/75	12/31/78	169.3
5-35944	Stanford University	Innovative Measurement Technology for the Semiconductor Device Industry Based on Electron Spectroscopy	6/30/75	4/ 2/79	632.8†
611377*	Jet Propulsion Laboratory	Techniques for Chemical Diagnostics in Semiconductor Processing	2/15/76	8/31/79	202.0
6-35766	Westinghouse Electric Corp	Advanced Planar Silicon Test Structures to be Measured with High Speed Testers	9/ 1/76	10/31/79	199.0
7-35741	University of Florida	Mobility-Dopant Density Relations in n- and p-Type Silicon	3/11/77	6/10/80	81.7
708041* 801846*	Naval Research Laboratory	Ion Implanted Silicon Characteristics	3/11/77	9/30/79	41.0
809074*	Xerox Corporation	DLTS Measurements and Analysis	4/ 3/78	9/15/78	9.5

* Order No.
\+ Includes $3070 Government furnished equipment
† Includes $138 300 special equipment.

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10. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

The program described in this report was undertaken in 1973 to develop the measurement technology necessary to enable device manufacturers to exert more effective control over the materials and processes they use to make integrated circuits with the ultimate aim of providing increased reliability at reasonable cost. Work was carried out in 12 technical areas: resistivity and dopant characterization; crystal defects and contaminants; oxides and other insulator films; physical analysis techniques; film and layer thickness; materials for infrared detector arrays; materials and procedures for wafer processing; photolithography; microelectronic test patterns; wafer inspection and test; die and interconnection bonding; and hermeticity. Many improved measurement technologies of considerable diversity were developed and documented during this program. The results have been widely and beneficially applied in other DoD projects and by the U.S. semiconductor industry. At the present time the work is being extended to accommodate the denser circuits, larger chips, and new processing techniques associated with very large scale integration.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

Electronics; integrated circuits; metrology; microelectronics; semiconductors; silicon.

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