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Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1978 to September 30, 1979

F. F. Oettinger and R. D. Larrabee, Editors

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
U.S. Department of Commerce
Washington, DC 20234

August 1980

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PREFACE

This work was conducted as a part of the Semiconductor Technology Program at the National Bureau of Standards (NBS). This program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems of the Department of Energy (DOE) under DOE Task Order AO21-EES. The contract is monitored by Dr. Russell Eaton of DOE. The NBS point of contact for information on the various task elements of this project is F. F. Oettinger of the Electron Devices Division at the National Bureau of Standards.

Measurement Techniques for High Power Semiconductor Materials and Devices

ANNUAL REPORT
October 1, 1978 to September 30, 1979

F. F. Oettinger and R. D. Larrabee, Editors

EXECUTIVE SUMMARY

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from the rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes. Application of this measurement technology will, for example, enable industry to make devices with higher individual power-handling capabilities, thus permitting large reductions in the cost of power-handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major tasks under this project are (1) to evaluate procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce lifetime or contribute to leakage current in power-device-grade silicon, (2) to coordinate standardization activities of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon material and structures, (3) to determine technical impediments to a more effective utilization of neutron transmutation doped silicon for thyristor production, and (4) to determine the measurement and analysis needs to aid in the application of zinc oxide varistor technology for the manufacture of high voltage limiters for lightning arrester application.

Deep-Level Measurements — The presence of deep-level impurities in semiconductor power devices is a consequence of their unintentional introduction during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. In either case, the dominant effect of the deep level is to modify the minority carrier lifetime. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize and understand the behavior of intentionally added impurities. The use of such techniques for process diagnostics would enhance the manufacturer's ability to control the quality (yield, reliability, and cost) of his product. The effective utilization of deep-level measurements requires three things: (1) developing well-characterized measurement and data analysis proce-

dures, (2) characterizing a variety of levels to establish the validity of the techniques and establishing a data bank of the properties of known defect levels, and (3) understanding the relationship between the presence of deep levels and the corresponding device parameters. Efforts during this contract period were aimed at satisfying these basic requirements.

A deep-level transient spectroscopy (DLTS) facility was established in this laboratory. Detailed comparisons of this technique were made with the previously established isothermal transient capacitance (ITCAP) technique. The ITCAP and DLTS techniques were used to characterize a variety of deep levels which were purposely introduced by diffusion. Direct comparisons are made between these characterizations and such data as are available in the literature.

In addition, two deep levels found in a commercially fabricated power-rectifier wafer were characterized and studied in detail. Wafer maps of the defect density for each of these levels were measured. However, no correlation between electrical parameters and defect density of either level was observed. The behavior of the DLTS signal at temperatures higher than where the emission from these two levels is observed is not understood at this time. This region of the DLTS signal will be studied in greater detail because this is the region where the deeper lifetime controlling levels produce DLTS signals.

Spreading Resistance Measurements - The spreading resistance technique has been widely used to obtain resistivity profiles, both for process control and process development applications. Until recently, however, the repeatability and reproducibility of measurements obtainable on high resistivity *n*-type material (typically used for the starting material for power transistors and thyristors) with conventional specimen preparation techniques have been very limited. For example, while specimens polished with silica generally have acceptably low levels of scatter for successive data points after a given specimen polishing, they have poor reproducibility of mean value upon repreparation of the specimen surface. Lapped specimens, on the other hand, exhibit somewhat better reproducibility of mean value upon repreparation of the specimen but exhibit noticeably more scatter (poorer precision) between successive measurements after any one specimen preparation. This specimen preparation problem had served to limit the reliability with which the spreading resistance technique could be used to monitor the development of state-of-the-art or even of routine device structures.

The results of extensive testing to identify and verify improved specimen preparation procedures were reported during FY-78. It was shown that the use of diamond polishing for high resistivity *n*-type silicon gives excellent reproducibility of average spreading resistance value and, in fact, gives improved repeatability of succes-

sive spreading resistance data compared to that obtainable with silica-polished specimens.

During FY-79, the results of those tests were reported to the February meeting of ASTM Committee F-1 on Electronics. Based on those tests, a draft of a proposed preferred procedure for preparing specimens prior to spreading resistance measurements was written and submitted to Subcommittee F-1.06 on Electrical and Optical Characterization. The draft of the preferred procedure was discussed by the subcommittee, amended accordingly, and approved for submission to formal ballot approval by the entire committee. This letter ballot was scheduled for the first quarter of FY-80.

A multilaboratory test of the repeatability and reproducibility of spreading resistance measurements was subsequently agreed upon by the same subcommittee. The test has been designed to involve at least eleven laboratories with each laboratory making spreading resistance measurements on a wide resistivity range of p- and n-type silicon specimens. In this test, laboratories are allowed to use one of three specimen surface preparations: silica polishing, diamond polishing, or lapping. The experimental design calls for the results to be analyzed as a function of specimen preparation.

Neutron Transmutation Doped Silicon Studies – Neutron transmutation doping (NTD) is a promising technique for the production of uniformly doped silicon needed to optimize the performance of high power devices. Unfortunately, the NTD process itself introduces lattice damage, which must be removed before useful devices can be fabricated from neutron-irradiated silicon. The nature of the damage produced appears to depend on the characteristics of the reactor used to create the NTD material, especially on the magnitude of the neutron flux and on the velocity distribution of the neutrons. However, at present there are no generally agreed-upon standard techniques for accurately characterizing reactors for NTD silicon production. In addition, the annealing procedures for removing the damage that is produced are not well understood, and there is considerable disagreement as to the means for removing lattice damage in a manner consistent with desired thyristor characteristics. For example, the dependence of the annealing techniques required upon the particular neutron velocity distribution ratio has not been determined, and annealing techniques that allow reproducible lifetime control by subsequent electron irradiation have not yet been developed.

During this reporting period, a survey was conducted involving manufacturers and users of NTD silicon, as well as with research workers in universities, government laboratories, and private industry involved with the NTD process. The objective of the survey was to determine the technical impediments to a more effective utilization of NTD silicon for thyristor production.

A summary report that discusses the problems involved in the NTD process and elaborates the concerns related to damage in transmuta-

tion doped silicon resulting from the neutron irradiation has been prepared.

Zinc Oxide Varistor Studies – Zinc oxide technology is relatively new and is only beginning to be applied in lightning arrester applications. Other lower power applications exist and the required device development is accomplished mainly by empirical methods. Zinc oxide ceramics are polycrystalline, multiphase bodies and, by silicon standards, dirty. Good fundamental understanding of their behavior has only recently been described in the literature, and as yet only in an incomplete way. Their electrical conductivity varies as V^{α}, where V is voltage and α, the nonlinear exponent, can be as large as 80. It is not known what limitation on α exists nor what material properties determine it. Zinc oxide has relatively low thermal conductivity. The energy absorbed during a transient by the ceramic has to be dissipated, and any standby heating reduces the energy-absorption capability of the device. Low current instability is usually present; its cause is not known.

During this reporting period, a study was carried out to determine the measurements and analysis needs to aid in the application of zinc oxide varistor technology to the manufacture of high-voltage limiters for surge arrester applications. Visits were made to several manufacturers to discuss their programs for development of zinc oxide (ZnO) lightning arresters and to learn about measurement problems that they may be experiencing. The literature on zinc oxide varistors was critically reviewed to determine how well the behavior of the devices is understood and in which direction new research should go.

Based on these inputs, a summary report that details the measurements and analysis needs associated with the fabrication and characterization of zinc oxide varistors was prepared.

1. INTRODUCTION

This project is directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and from the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes.

The project is designed to provide, disseminate, and foster the standardization of improved measurement methods required in high-power semiconductor technology, for use in specifying materials and devices in commerce, and for use by industry in controlling device manufacturing processes and in designing systems. Application of this measurement technology will, for example, enable industry to: (1) make power semiconductor devices with greater uniformity of characteristics, thus permitting improvements in parallel and series connections of devices for applications from fusion generation to ac/dc conversion, (2) make devices with higher individual power handling capabilities, thus permitting large reductions in the cost of power handling equipment and fostering the development of dc transmission lines to reduce both energy waste and the extent of required rights-of-way, and (3) provide devices, and the systems utilizing them, with the reliability and performance required in energy generation, utilization, and conservation.

The major tasks under this project are (1) to evaluate procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce lifetime or contribute to leakage current in power-device grade silicon, (2) to coordinate standardization activities of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon material and structures, (3) to determine technical impediments to a more effective utilization of neutron transmutation doped silicon for thyristor production, and (4) to determine the measurement and analysis needs to aid in the application of zinc oxide varistor technology for the manufacture of high voltage limiters for lightning arrester application.

2. DEEP-LEVEL MEASUREMENTS

by

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2.1 Objectives

The overall objective of this task is to evaluate the use of thermally stimulated current and capacitance measurements (TSM) and other deep-level measurement techniques for characterizing defects which control leakage current and lifetime in power-grade silicon materials and devices. Phases 1, 2, and 3 of this continuing task were completed in September 1976, September 1977, and September 1978, respectively. The present phase of this task (phase 4) had the following specific objectives:

2.1 Compare specific characteristics of the deep-level transient spectroscopy (DLTS) technique to the isothermal transient capacitance (ITCAP) technique in order to establish the relationship between the results of these two techniques.

2.2 Characterize defect centers which are created by the intentional introduction of specific impurities into the silicon lattice.

2.3 Correlate device electrical parameters with the presence of deep-level defects by measuring wafer maps of both the device electrical parameters and the defect density.

2.2 Background

Deep-level defect measurement techniques such as TSM [2-1] and DLTS [2-2] utilize the ability of electrically active defects to trap free carriers and to re-emit them by thermal stimulation. Analysis of the measured thermal emission rate into the depletion layer of a test device as a function of temperature leads to activation energies of the defects present. The magnitude of the capacitance changes associated with the emission can be related to the densities of the defects present. The interest in measurement of deep levels in semiconductors, particularly in application to power devices, stems from two related aspects: 1) detection, identification, and control of unwanted intrinsic or process-induced impurities or defects; and 2) characterization and control of impurities specifically introduced for lifetime control. These techniques, which had generally been confined to laboratory studies of packaged devices, have now been extended to measurements on devices in wafer form [2-3,2-4], and routine procedures for measurement and analysis of data are being developed so that these techniques can be utilized as diagnostic tools during fabrication.

The approach in this program has been twofold. Apparatus has been developed to permit deep-level measurements on both packaged devices and full-sized wafers. Although the developed measurement techniques are fully applicable

to either device format, each format offers distinctive advantages. The packaged device format permits higher precision in thermometry; this in turn allows more precision in the measurement of emission rate and thermal activation energy. Although these measurements can also be performed on the full-wafer apparatus, this equipment is more suited for mapping of such parameters as deep-level defect density and the corresponding electrical device parameters of interest. In addition, where it is used as a diagnostic tool in the manufacturing of power devices, the wafer-probing apparatus offers the advantage of allowing deep-level measurements to be made on processed wafers without the costly and time-consuming packaging step.

2.3 Accomplishments During Reporting Period

2.3.1 Comparison of Deep-Level Measurement Techniques (Objective 2.1)

2.3.1.1 Introduction

The primary method used for characterizing defects at NBS in the past has been the isothermal transient capacitance (ITCAP) technique. Details of this technique have been discussed previously [2-5,2-6]. In this method, a temperature is selected, and a 1-MHz capacitance bridge measures the transient response of the depletion capacitance of a test device after trapping of majority carriers in deep-level centers. This capacitance increases as the depletion width decreases due to re-emission of trapped majority carriers from the deep level. The decay time constant of the capacitance transient at any selected temperature is the reciprocal of the emission rate of carriers from the deep-level center at that temperature. The emission rate of electrons in its simplest form (see ref. [2-5], pp. 40-46, for additional details) is given by (an analogous relationship can be given for holes):

$$e_n = B_n T^2 \exp(-\Delta E_n / kT) , \qquad (2\text{-}1)$$

where e_n is the electron emission rate, T is the absolute temperature, k is the Boltzmann constant, ΔE_n is the energy separation of the deep level in question from the conduction band edge, and $B_n T^2$ is a factor containing the electron capture cross section, electron thermal velocity, and the density of states at the conduction band edge. The factor T^2 in the expression $B_n T^2$ is based on the thermal velocity varying as $T^{1/2}$ and the density of states at the band edge varying as $T^{3/2}$. The factor of proportionality, B_n (or B_p) will be taken as a constant in this report. The resulting capacitance transient can be modeled by:

$$C(t,T) = C_f - (C_i - C_f) \exp(-e_n t) , \qquad (2\text{-}2)$$

where C(t,T) is the measured capacitance as a function of time, t, at the selected temperature, T, and C_i and C_f are the capacitances at the beginning and end of the transient response. Figure 2-1 shows a series of reverse-bias pulses (upper trace) preceded by an interval of zero bias during which the deep levels are filled with majority carriers. The transient response to the application of the reverse bias is shown in the lower trace of figure 2-1 as an exponential increase in capacitance from an initial value of C_i to a final value of C_f in accordance with eq (2-2).

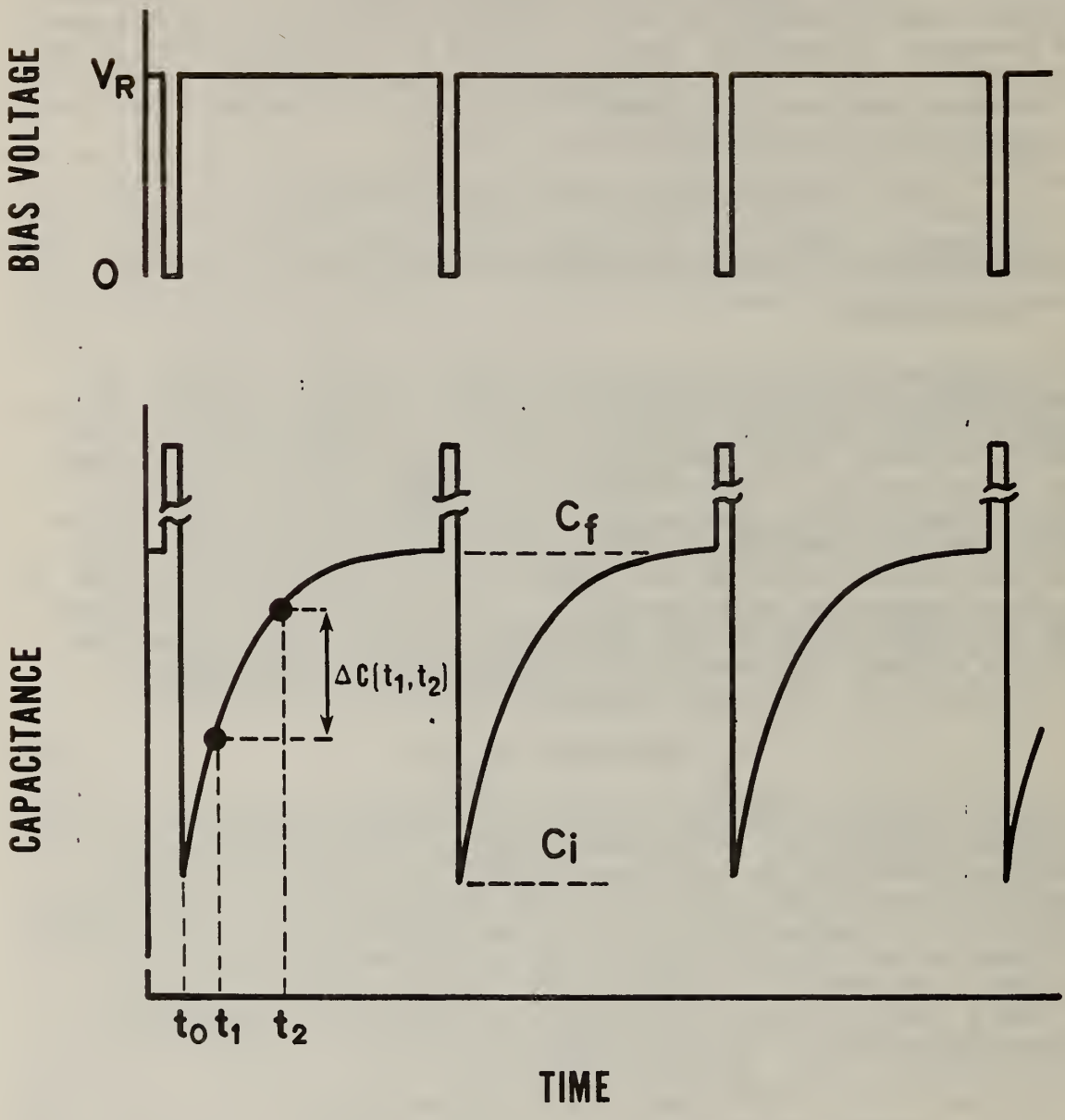


Figure 2-1. Schematic representation of reverse-bias pulses of applied voltage (upper trace) and the resulting capacitance transient (lower trace).

In the ITCAP technique, a commercial 1-MHz capacitance bridge is used to measure the capacitance, and a chart recorder is used to record a single transient after the application of the reverse-bias voltage V_R following a momentary zero-bias charging interval. The device temperature is held constant during the measurement. This measurement is then repeated at different temperatures. Because the response time of the commercial capacitance bridge is approximately 2 ms, emission rates faster than approximately 50 s^{-1} are not measurable. The limitation on the slow end of the emission rate range is the patience of the operator and the temperature stability of the cryostat.

In the DLTS technique [2-2], the test device is continually pulsed at a fixed repetition rate as shown in the upper trace of figure 2-1. A higher frequency (10 to 100 MHz) capacitance bridge is generally used, and emission rates as fast as 2×10^4 s^{-1} are measurable. The recording and analysis of data also differ from that used in the ITCAP technique. The temperature of the device is allowed to increase or decrease at a slow rate while the difference in capacitance at two predetermined times t_1 and t_2, $\Delta C(t_1,t_2)$, is recorded (see lower trace in fig. 2-1). As shown by Lang [2-2], the DLTS signal ΔC (t_1,t_2), can be used to measure the decay rate of the exponential capacitance transient.

2.3.1.2 The High Frequency Capacitance Bridge and Signal Processing

A variety of methods has been devised for implementing the high frequency capacitance bridge in DLTS measurements [2-7,2-8]. Figure 2-2 is a schematic diagram of the bridge assembly and the DLTS signal processing scheme used in the present measurements. This system was selected on the basis of its basic simplicity and inherent insensitivity to operating frequency. An rf signal voltage is applied to the center tap of one winding of an rf transformer* through blocking capacitor, C. One end of this winding is connected to the device under test (DUT) and the other to a balance capacitor (C_B). The balance capacitor is adjusted so that its capacitance equals the depletion capacitance of the device under test. Thus, under steady-state balanced conditions, the rf currents in the two halves of this winding are equal and opposite, and no net voltage is developed across the other (output) winding of the transformer. Two synchronous pulse generators provide the reverse bias to the device under test and the initiation signals to the analog gate and digital timer. The capacitance transient produces an unbalance of the current in the center-tapped winding of the transformer, and a voltage is developed across the output winding of the transformer. The phase shifter and the double-balanced mixer provide phase-sensitive detection of the resultant transient-capacitance signal appearing across the output winding. The signal processing section of figure 2-2 utilizes a double box-car integrator as described by Lang [2-2]. In addition, an analog gate is provided to block the capacitance transient signal during the charging pulse in order to avoid overloading the input circuits of the box-car integrator (see Appendix A for details of the analog-gate circuit; also see Appendix B for modifications to the bridge of fig. 2-2 which improves the operation of the circuit).

*Minicircuits Laboratory model TM01-IT rf transformer has been used in this application. However, its use does not constitute a recommendation or endorsement by NBS, nor does it imply that this transformer is necessarily the best available for this application.

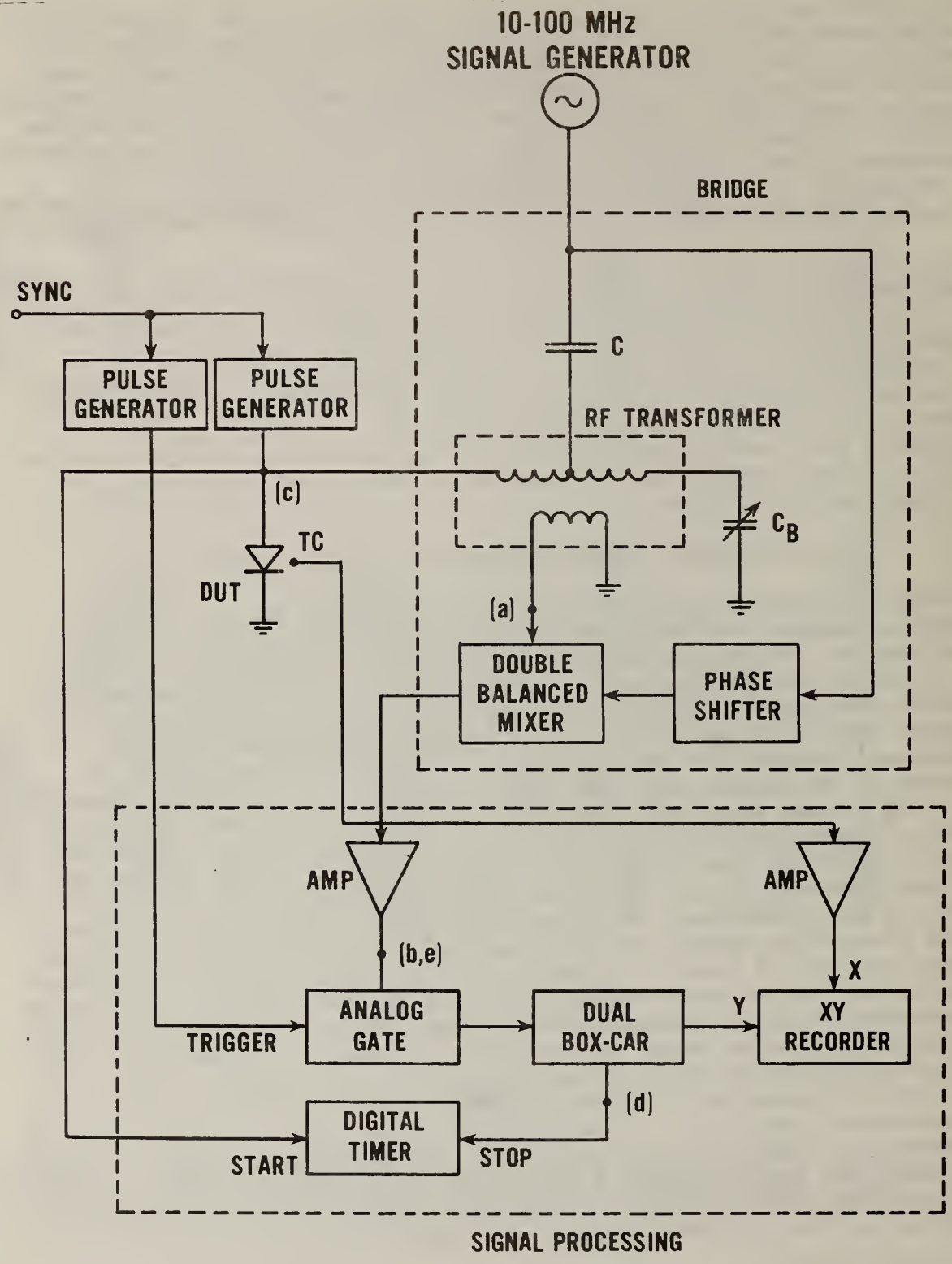


Figure 2-2. Schematic diagram for the high frequency bridge and the signal processing for the DLTS measurement. The signals appearing at the lettered points are shown by the corresponding traces in figure 2-3 and are discussed in the text.

Figure 2-3 shows oscilloscope traces of the relevant signals observed at the lettered points of the circuit of figure 2-2 with a platinum-diffused p^+n junction diode as the device under test. The signal from the pulse generator (trace c) is a negative 10-V reverse bias pulse with a 1.5-μs zero-voltage interval between pulses for charging the deep levels with majority carriers. The rf voltage at the device under test is about 100 mV peak-to-peak. A large unbalanced rf signal is developed across the output winding of the transformer during the zero-bias charging interval because of the large depletion capacitance under these conditions (trace a). The actual capacitance transients are shown in traces (b) and (e) on two different time scales. Trace (b) shows that the recovery time of the capacitance bridge after reestablishing reverse bias is less than 10 μs. It should be noted that the capacitance transient is positive in figure 2-3 (trace e). The setting of the phase shifter determines whether positive or negative signals are obtained for any given set of conditions, so the actual polarity observed and reported has no special significance.

Trace (d) of figure 2-3 shows the position of the sampling gates of the box-car integrator. The sampling gate width (typically 5 μs) and the sampling delay times appropriate to the measurement conditions are preselected for a given situation. In the present system, the sampling delay times (hereafter called delay times), t_1 and t_2 (see fig. 2-1), are measured using a digital counter/timer. A signal from one pulse generator starts a counter/timer at the beginning of the DLTS transient, and one of the sampling-gate signals stops it. The final reading of the counter is a direct measure of t_1 or t_2. This technique affords a convenient way of measuring t_1 and t_2 with high accuracy.

The temperature of the device under test is sensed by a thermocouple (TC), amplified, and used to drive the x-axis of an x-y recorder. The DLTS output signal, $\Delta C(t_1,t_2)$, from the dual box-car integrator is used to drive the y-axis of the recorder. Examples of the resulting recordings are shown in figure 2-4 and are discussed in the following section.

2.3.1.3 Comparison of DLTS and ITCAP Measurements

Examples of typical DLTS curves observed on the x-y recorder of figure 2-2 are shown in figure 2-4 for a palladium-diffused diode. Figure 2-4a shows a large peak (i.e., energy level) introduced by palladium diffusion into n-type silicon; there is also a suggestion of an additional deeper level (arrow). When palladium is diffused into p-type silicon, there are two large peaks (i.e., energy levels (fig. 2-4b)), with a detectable signal between them that may represent additional levels.

Each of the curves as illustrated in figure 2-4 represents a scan in temperature from liquid nitrogen temperature (-195.8°C) to about room temperature with the gate delay times (t_1, t_2) fixed at the values indicated. In order to determine the activation energy corresponding to any given level, it is necessary to observe these DLTS curves with a variety of gate delay times. This is illustrated in figure 2-5. This figure shows a series of DLTS peaks traced by an x-y recorder that characterize the electron emission from a platinum level in n-type silicon. Nine different settings of the gate delay times t_1 and t_2 were used to produce nine distinct peaks corresponding to

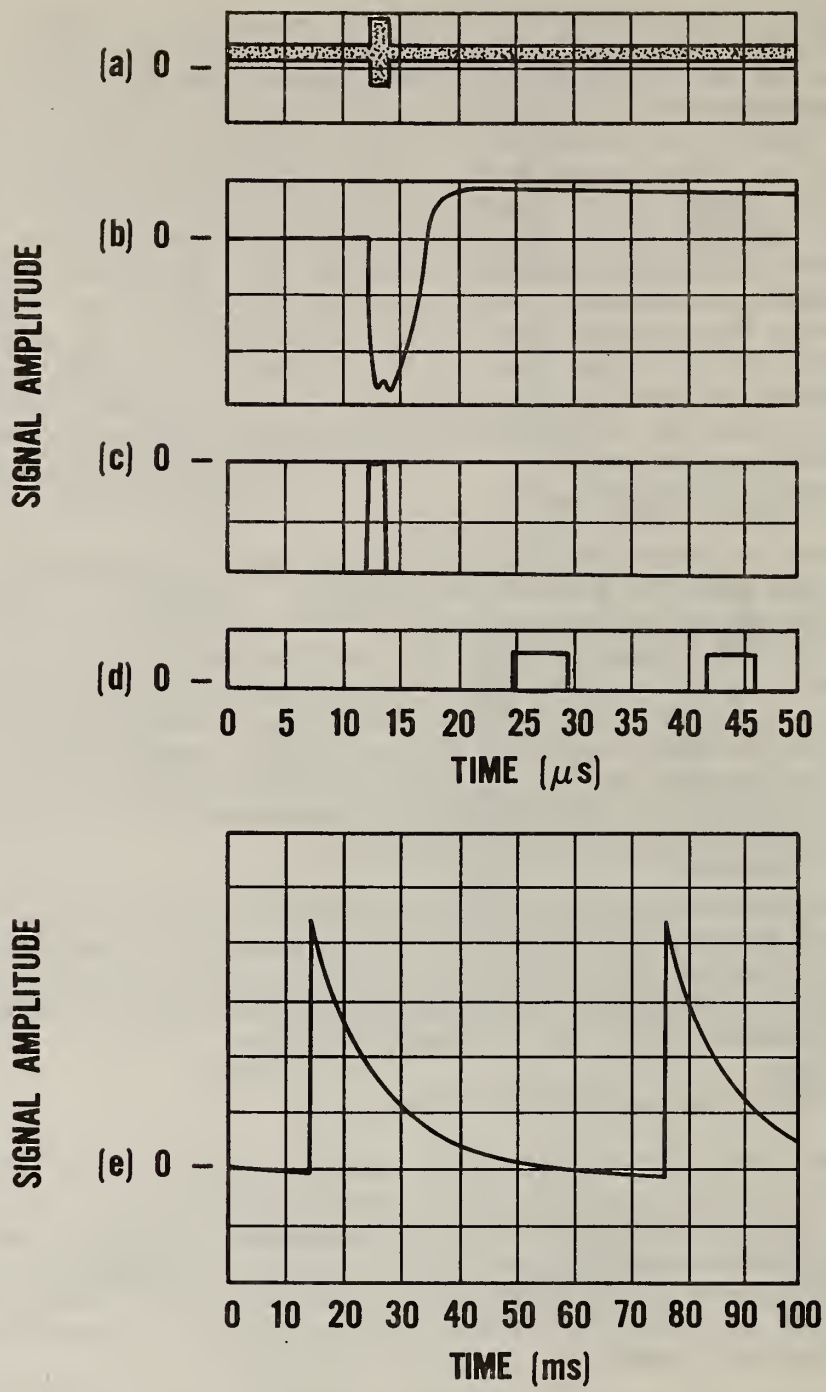
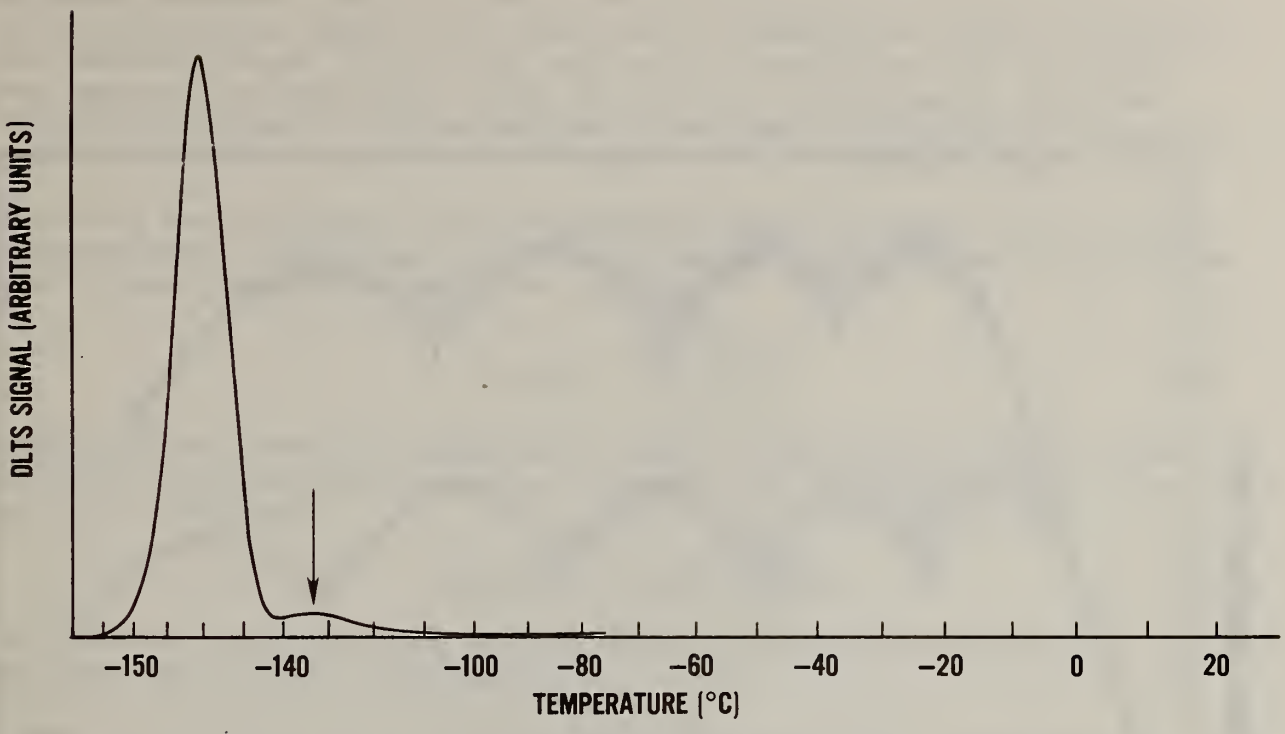
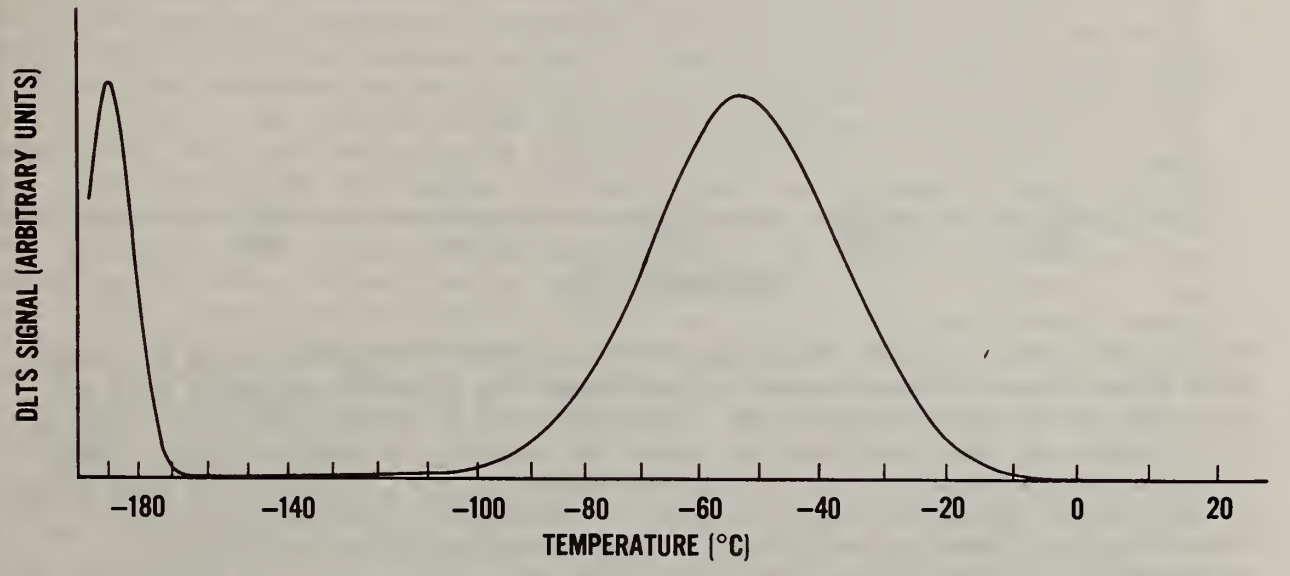


Figure 2-3. Drawings of oscilloscope traces of the signals observed at the lettered points on figure 2-2; the traces were measured with a platinum-diffused p^+n junction device at approximately -140°C with an rf frequency of 38.6 MHz. Trace e shows the latter portion of the DLTS transient on a longer time scale with ten times the vertical sensitivity of the initial portion shown in trace b. The zero level of each trace is shown on the left, and the vertical scales are 500 mW, 200 mV, 5 V, 5 V, and 20 mV per unit distance equal to the horizontal tick-marks for traces a through e, respectively.



a. DLTS curve of a p^+n Pd-diffused diode with t_1 = 4113 μs and t_2 = 48,240 μs.



b. DLTS curve of an n^+p Pd-diffused diode with t_1 = 9 μs and t_2 = 105 μs.

Figure 2-4. DLTS curves of two different junction devices; the indicated times are the respective gate delay times (i.e., t_1 and t_2) of the box-car integrator.

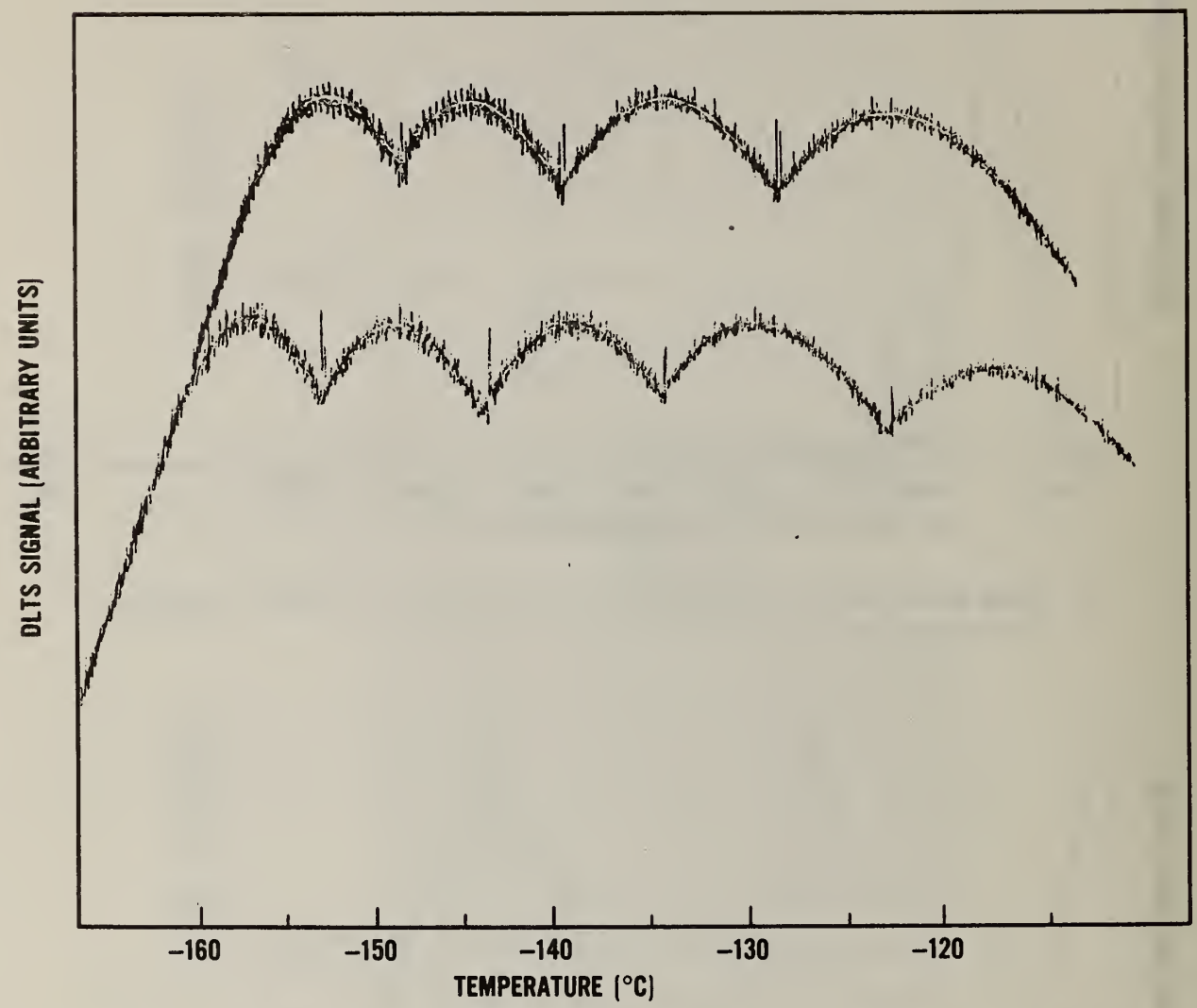


Figure 2-5. X-y recorder tracings of a series of DLTS peaks using different gate delay times. These curves characterize the electron emission from a platinum level in *n*-type silicon. The lower set of curves has been displaced with respect to the upper set of curves for clarity of presentation. Taken in order of peak position in temperature (from left to right), the nine pairs of gate delay times are (t_1/t_2 in μs): 4902.5/49002.5, 2002.5/20002.5, 1002.5/10002.5, 502.5/5002.5, 202.5/2002.5, 102.5/1002.5, 52.5/502.5, 22.5/202.5, 12.5/102.5; these times also apply to figure 2-7. A heating rate of approximately 0.1°C/s was used.

different emission rates at different temperatures from the same deep level. In this particular example, two scans over the temperature range were made at four selected values of t_1 and t_2 (top set of curves); then two more scans were made at five additional values of t_1 and t_2 (intentionally displaced lower set of curves). The temperature of each peak corresponds to a specific emission rate determined by the gate delay times as discussed below.

These data were analyzed using the technique discussed by Lang [2-2]. The emission rate at the temperature of the peaks in figure 2-5 can be calculated from the gate delay times using the relation:

$$e_n(T_m) = \frac{\ln(t_1/t_2)}{(t_1 - t_2)} \qquad (2\text{-}3)$$

where T_m is the absolute temperature at the maximum of the DLTS peak corresponding to the gate delay times of t_1 and t_2. By taking the logarithm of eq (2-1), one obtains:

$$\ln(e_n/T^2) = \ln(B_n) - \Delta E_n/kT \ . \qquad (2\text{-}4)$$

Thus, the intercept of a plot of $\ln(e_n/T^2)$ *vs.* $1/T$ gives the factor B_n, and the slope of the line yields $\Delta E_n/k$.

Figure 2-6 illustrates the Arrhenius plots for two levels in platinum-diffused silicon (details of device preparation are given in the next section). Platinum produces one level in each half of the band gap. Two sets of data are presented in figure 2-6 for each of these levels. One set was observed by DLTS and the other by ITCAP. The DLTS data were measured on devices on unscribed wafers using the hot/cold wafer mapping apparatus [2-3]. The ITCAP data were measured on packaged devices scribed from the same wafers. These data were analyzed using a linear regression computer program to find the least-squares regression line and to determine the corresponding B and ΔE values. The results of the statistical analyses on these four individual data sets and the combined DLTS and ITCAP data sets are shown in table 2-1. Entries include the number of data points, the Pearson's correlation coefficient, the activation energy, and the B factor determined from the linear regression line. The error of estimation of the ΔE and B values is also noted in the table. These results show that it is possible to achieve a very good linear fit to the experimental data resulting in relatively small errors of estimation of ΔE and B. However, comparison of the results of the analyses on the individual DLTS and ITCAP data sets shows that different values for B and ΔE of the same level are obtained. For example, although the statistical error of estimation of ΔE_n is about 1 meV for the individual DLTS or the ITCAP measurements, these values differ by a significant amount thereby producing a significant difference in the B_n factors. Similar comments can be made for the ΔE_p and B_p values for the other level. These differences are believed to originate from systematic errors in either or both measurement systems. However, the overall agreement of the two measurement systems and the quality of the data, as seen in figure 2-6, are quite acceptable; the ΔE_n and ΔE_p for these two levels of platinum in silicon were estimated to be 197 $\pm$ 5 and 300 $\pm$ 3 meV, respectively.

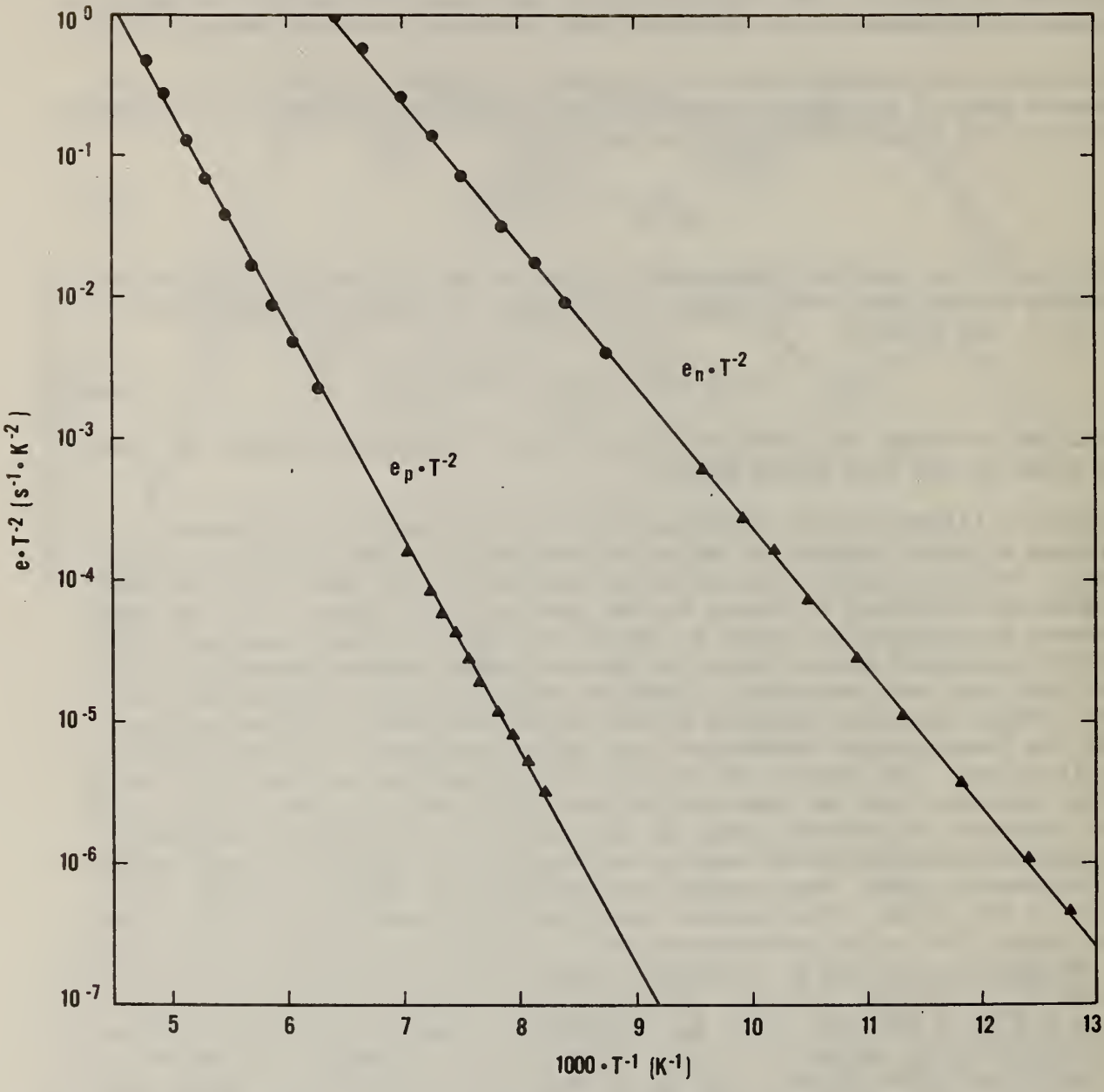


Figure 2-6. Arrhenius plots for two levels of platinum in silicon as measured by DLTS (dots) and ITCAP (triangles).

Table 2-1. Summary of the Statistical Analyses on the Four Data Sets for the Two Levels of Platinum in Silicon Shown in Figure 2-6.

	DLTS	ITCAP	Combined
Number of Data Points	9	9	18
Level in Upper Half of Bandgap (n-type silicon)			
Correlation Coefficient	-0.9999348	-0.9999402	-0.9999514
ΔE_n (meV)	201.5 $\pm$ 0.9	194.0 $\pm$ 0.8	196.9
B_n ($\times 10^6$) ($s^{-1} \cdot K^{-2}$)	3.02 $\pm$ 8.0%	1.37 $\pm$ 10.9%	2.01
Level in Lower Half of Bandgap (p-type silicon)			
Correlation Coefficient	-0.9999636	-0.9999130	-0.9999919
ΔE_p (meV)	301.2 $\pm$ 1.0	297.7 $\pm$ 1.5	300.2
B_p ($\times 10^6$) ($s^{-1} \cdot K^{-2}$)	8.44 $\pm$ 6.4%	6.34 $\pm$ 14.2%	7.92

Table 2-2 summarizes the results of five separate DLTS measurements of the platinum level in the upper half of the band gap in silicon. The measurements were made on three separate devices (A, E, and F) on the same wafer (F_1, F_2, and F_3 are three independent measurements on the same device). These data show the statistical variability or the reproducibility of the measurement. The variations in the data of table 2-2 are attributed to systematic uncertainties in the measurements with the largest uncertainty assumed to be in the accuracy of the specimen temperature measurement. The row with 45 data points is the result of statistically combining all of the data with equal weight. The goodness-of-fit in this case is not as good as that of any individual data set, but both activation energy, ΔE_n, and the intercept, B_n, reflect the "composite" value of all the data. Thus, it can be concluded that the results agree better with other DLTS results (table 2-2) than with ITCAP results (table 2-1). A systematic error of about 1°C in the wafer chuck apparatus would account for the discrepancy in activation energy between the DLTS and ITCAP results for the deeper level and 2.3°C for the shallower level. These are not unreasonable values in view of the possibility of poor thermal contact between the wafer and its heat sink (this contact is maintained by a vacuum hold-down scheme without the use of thermal compound).

2.3.1.4 Model Calculation of DLTS Curves

Equation (2-1) contains all the physics which govern the simplest thermal emission behavior of deep levels in semiconductors. However, unambiguous analysis of experimental data by the use of this equation depends on a number of assumptions: 1) the emission-rate constant, B (i.e., the capture cross section), is independent of temperature; 2) there are no electric-field effects (e.g., Poole-Frenkel effect [2-9]) which can change the effective activation energy; 3) the levels in a multilevel system do not interact and are well separated in energy; 4) the depletion edge is abrupt (to avoid minority carrier effects); etc. Failure of any of these assumptions can lead to an erroneous determination of the activation energy. For example, if the B factor (i.e., cross section) depends on some power of the temperature [2-10], the apparent activation energy computed by the process discussed above will differ from the true activation energy; if there is an exponential dependence [2-11], then the calculated ΔE will represent some composite of thermal activation and the cross section effects. On the other hand, electric-field effects, closely spaced multilevel systems, and minority carrier effects could lead to nonexponential behavior of the capacitance transient. In such cases, analysis and unambiguous assignment of activation energies are not straightforward.

Since the basic DLTS measurement technique is amenable to analytic modeling, it is possible to predict the theoretical behavior of specifically characterized defect centers. The simplest case would be a moderately deep but isolated level. A moderately deep level avoids the necessity of considering both majority and minority carriers which can be emitted with comparable probability from a center near midgap. If only majority carrier emission is prevalent, then eq (2-1) describes the emission rate for electrons, and capacitance transients will behave according to eq (2-2), with analogous relations for holes. The DLTS measurement proceeds by sampling the exponential

Table 2-2. Reproducibility of the DLTS Measurement on the Platinum Level in n-type Silicon.

Device	N	ΔE (meV)	B ($\times 10^6$) ($s^{-1} \cdot K^{-2}$)	Correlation Coefficient
A	9	201.5 $\pm$ 0.9	3.02 $\pm$ 8.0%	-0.9999348
E	9	201.8 $\pm$ 0.8	3.12 $\pm$ 7.3%	-0.9999448
F_1	9	204.4 $\pm$ 1.1	3.99 $\pm$ 10.2%	-0.999897
F_2	9	204.1 $\pm$ 1.2	4.00 $\pm$ 10.8%	-0.999884
F_3	9	203.0 $\pm$ 1.0	3.64 $\pm$ 9.4%	-0.999911
A, E, F_1, F_2, F_3	45	203.0 $\pm$ 0.6	3.55 $\pm$ 5.5%	-0.9998008

transient at two times, t_1 and t_2, and then displaying the difference $\Delta C(t_1, t_2, T)$ (see fig. 2-1). Thus:

$$\Delta C(t_1, t_2, T) = C(t_1, T) - C(t_2, T)$$
$$= (C_i - C_f) [\exp(-e_n t_1) - \exp(-e_n t_2)] . \quad (2\text{-}5)$$

The behavior of the DLTS signal with actual experimentally measured DLTS parameters is illustrated in figure 2-7. The upper curves were obtained by evaluating the right-hand side of eq (2-5); $e_n(T)$ was calculated from eq (2-1) using the experimentally derived parameters for the platinum level in the upper half of the silicon bandgap: $\Delta E_n = 0.2018$ eV, $B_n = 3.115 \times 10^6$ $s^{-1} \cdot K^{-2}$, and combined with the t_1 and t_2 values used in the actual measurement of Device E (see table 2-2). The magnitude of the transient $(C_i - C_f)$ is proportional to the defect density [2-1]. The experimental curves in the lower half of the figure have been replotted on a linear temperature scale for convenience. (In the actual measurement, the thermocouple temperature is recorded on a nonlinear scale.) It can be seen that there are no large differences in the shapes and the positions of the corresponding curves. A more critical comparison is made in the "activation energy" plot of figure 2-8. The solid line corresponds to the theoretically calculated Arrhenius plot with $\Delta E_n = 0.2018$ eV and $B_n = 3.115 \times 10^6$ $s^{-1} \cdot K^{-2}$. Points on this line were analyzed with the same regression analysis procedure used for experimental data and precisely the same parameters that were initially assumed were obtained. The closed circles are the data points taken from the actual experimental curves. A pair of dashed lines is also plotted in figure 2-8. These lines correspond to the two temperatures at the "half-maximum" position on each theoretical curve. These lines therefore delineate a "width" of the theoretical DLTS curves. The open circles plot the corresponding position of the "half-maximum" of the experimental curves. [Although the "Left Half Maximum" and the "Right Half Maximum" curves appear linear, they have no significance in terms of an "activation energy." They are plotted here for comparison purposes.] As can be seen, the agreement between theory and experiment is very good and this suggests that this platinum level behaves like a single isolated level.

Another question of concern is "How sensitive is the DLTS technique and analysis to nonexponential capacitance transients or nonideal situations?" Although a variety of conditions could lead to nonideal situations, the situation when two nearby levels contribute simultaneously, but independently, to the capacitance transient provides a typical example. Two aspects of this situation will be considered in this report: 1) distortions of the DLTS curves due to the presence of a second nearby level and 2) the corresponding misleading results of the analysis of DLTS data if the nearby level is disregarded.

The theoretical curves of figure 2-9 were computed for the ideal case of a single level at $\Delta E_n = 0.2018$ eV with $B_n = 3.115 \times 10^6$ $s^{-1} \cdot K^{-2}$. Consider the situation when, in addition to this primary level at 0.2018 eV, a second level at 0.175 eV is also present. Let this level have only half the density and the same cross section as the primary level. The resulting DLTS signal is then modeled by the following equation:

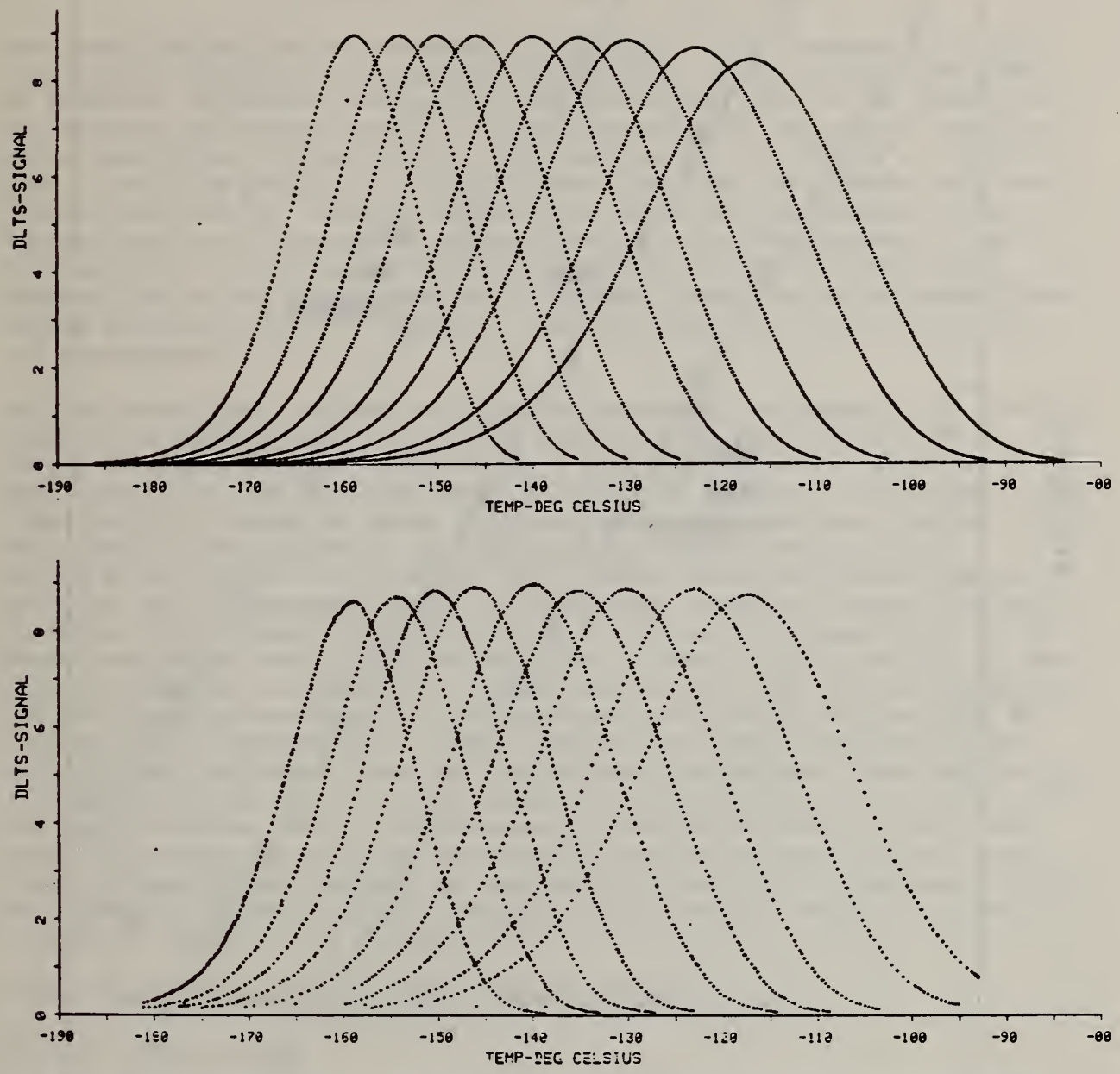


Figure 2-7. The DLTS curves for a platinum level in silicon determined from theory using ΔE_n = 0.2018 eV and B_n = 3.115 x 10^6 $s^{-1} \cdot K^{-2}$ (upper set of curves) and experimental measurement (lower set of curves); gate delay time settings for these curves are given in the caption to figure 2-5.

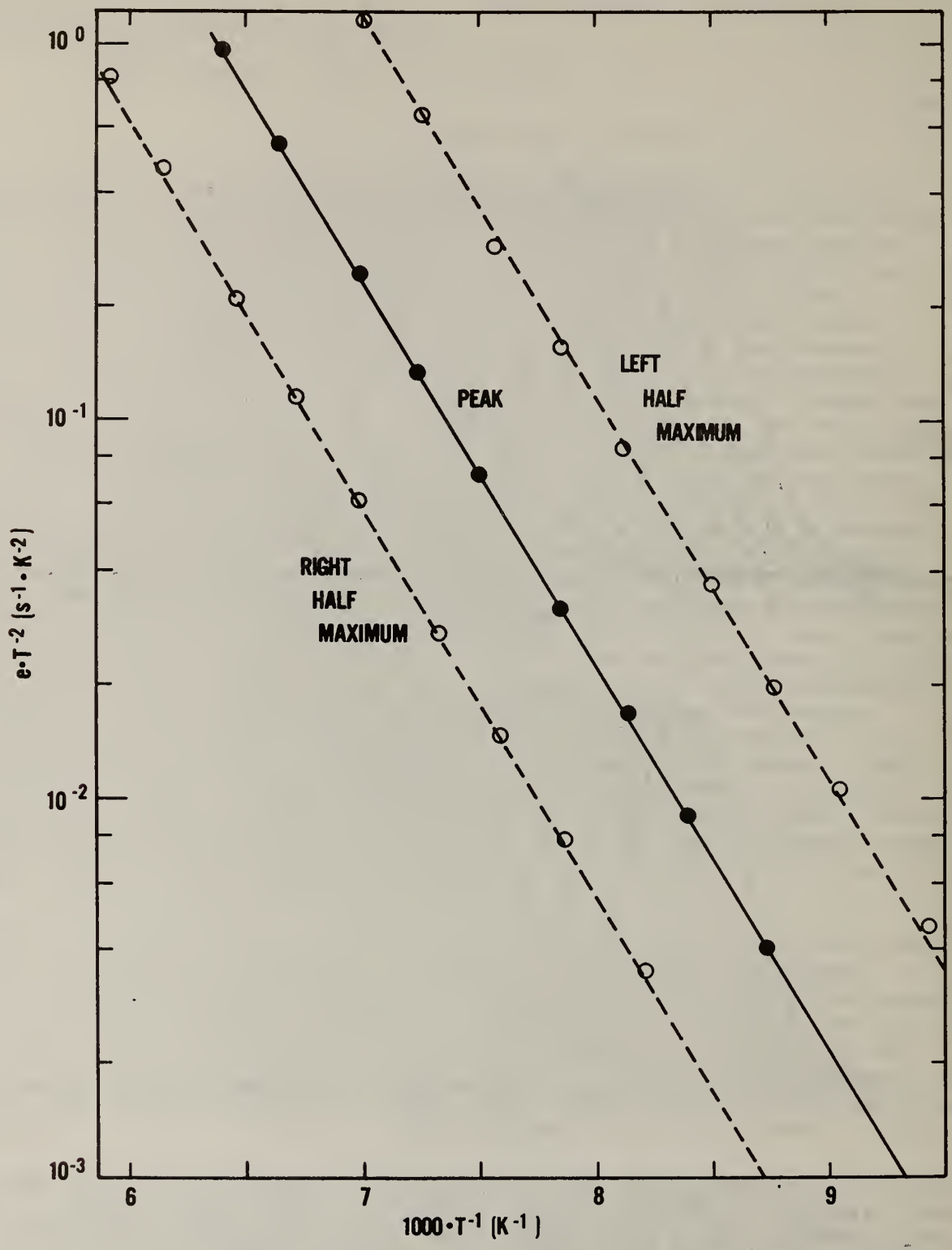


Figure 2-8. Arrhenius plots for the theoretical (solid lines) and experimental (closed circles) DLTS curves. The dashed lines (theory) and open circles (experiment) correspond to the left and right half maximum temperatures of each DLTS peak.

$$\Delta C(t_1, t_2, T) = (C_i - C_f) \left[\exp(-e_{n1}t_1) - \exp(-e_{n1}t_2) + \frac{1}{2}\left(\exp(-e_{n2}t_1) - \exp(-e_{n2}t_2)\right)\right] . \quad (2\text{-}6)$$

The resulting DLTS curves are shown in figure 2-9. The presence of the shallower level introduces a low temperature shoulder on the primary DLTS peak. In addition, it distorts the position of the primary peak to the extent that the apparent activation energy given by a single level analysis of these DLTS curves results in a value of $\Delta E_n = 0.212$ eV with $B_n = 9.71 \times 10^6$. In principle, it would be possible to separate these two levels by choosing very small values of t_1 and t_2. However, in practice, there are limitations in the response time of the capacitance bridge (usually a few microseconds to tens of microseconds). Large values of t_1 and t_2 are only limited by one's patience in doing the measurement and the thermal stability of the system. The curves shown in figure 2-9 represent the usual range of t_1 and t_2 for typical measurements.

For the second case, consider a situation completely analogous to the first except that the two levels are closer together with $\Delta E_{n1} = 0.2036$ eV, $\Delta E_{n2} = 0.187$ eV, the same factor of $B_n = 2.48 \times 10^6$ $s^{-1} \cdot K^{-2}$ applies to both levels, and the shallower level has half the density of the deeper. The resulting DLTS curves are shown in figure 2-10. A single-level analysis of these DLTS curves results in an "apparent" activation energy of $\Delta E_n = 0.2018$ eV with $B_n = 3.115 \times 10^6$ $s^{-1} \cdot K^{-2}$. These curves may reveal a subtle bulge on the low temperature side of each curve. However, chances are quite probable that on experimental data these bulges would be missed, and the apparent activation energy would be accepted. A more critical analysis of the data is presented in figure 2-11. Again (as in fig. 2-8), the Arrhenius plot and the lines representing the "half-maximum" are plotted for the ideal single-level theoretical case shown in figure 2-7 (solid and dashed lines). In addition, the present case for the two-level system under consideration is represented by the dots and open circles. In this figure, it is evident that the peak positions predict the presence of an apparent single level. However, the "width" of the peaks reveals the presence of more than one level. Thus, although situations such as depicted in figure 2-9 are obvious, a situation such as figure 2-10 could easily lead one astray. Excessive width is a sensitive indicator of a second level.

2.3.2 Characterization of Defect Centers (Objective 2.2)

2.3.2.1 Introduction

The two major deep-level measurement techniques available in the laboratory (ITCAP and DLTS) were used to characterize a variety of impurity-induced defects. Details of the ITCAP technique have been discussed previously [2-5,2-6]; the DLTS technique and its comparison to ITCAP were discussed in section 2.3.1 of this report. In addition to measurements on sulfur and gold levels which have been measured previously, measurements were completed on platinum, palladium, and manganese. These results are summarized in the next section (2.3.2.2).

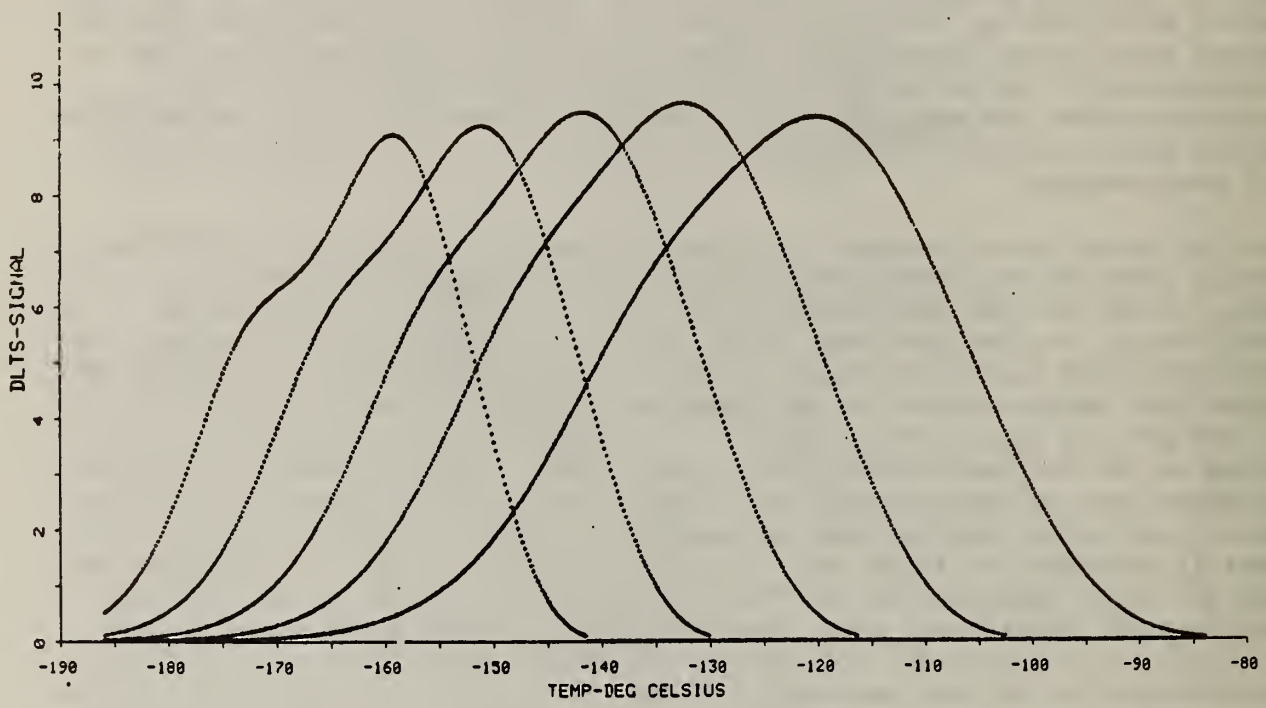


Figure 2-9. Theoretical DLTS curves based on the presence of two levels: primary level at ΔE_n = 0.2018 eV with B = 3.115 x 10^6 $s^{-1} \cdot K^{-2}$; secondary level at ΔE_n = 0.175 eV with the same B_n factor, but only half the density of the primary level; the curves (from left to right) correspond to the five pairs of gate delay settings (t_1/t_2 in μs): 4902.5/49002.5; 1002.5/10002.5; 202.5/2002.5; 52.5/502.5; and 12.5/102.5; these times also apply to figure 2-10.

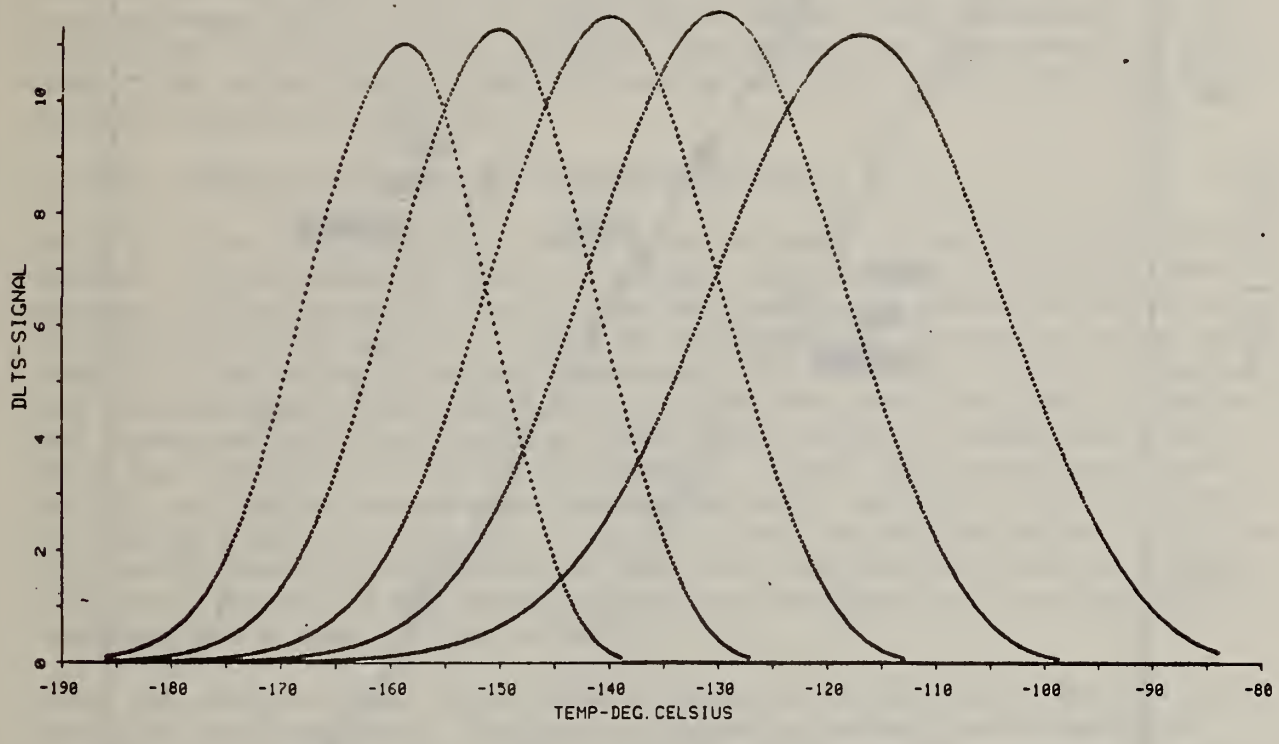


Figure 2-10. Theoretical DLTS curves based on two levels at ΔE_{n1} = 0.2036 eV, ΔE_{n2} = 0.1870 eV and $B_n = B_1 = B_2 = 2.48 \times 10^6$ $s^{-1} \cdot K^{-2}$; the gate sampling time settings are given in the caption to figure 2-9.

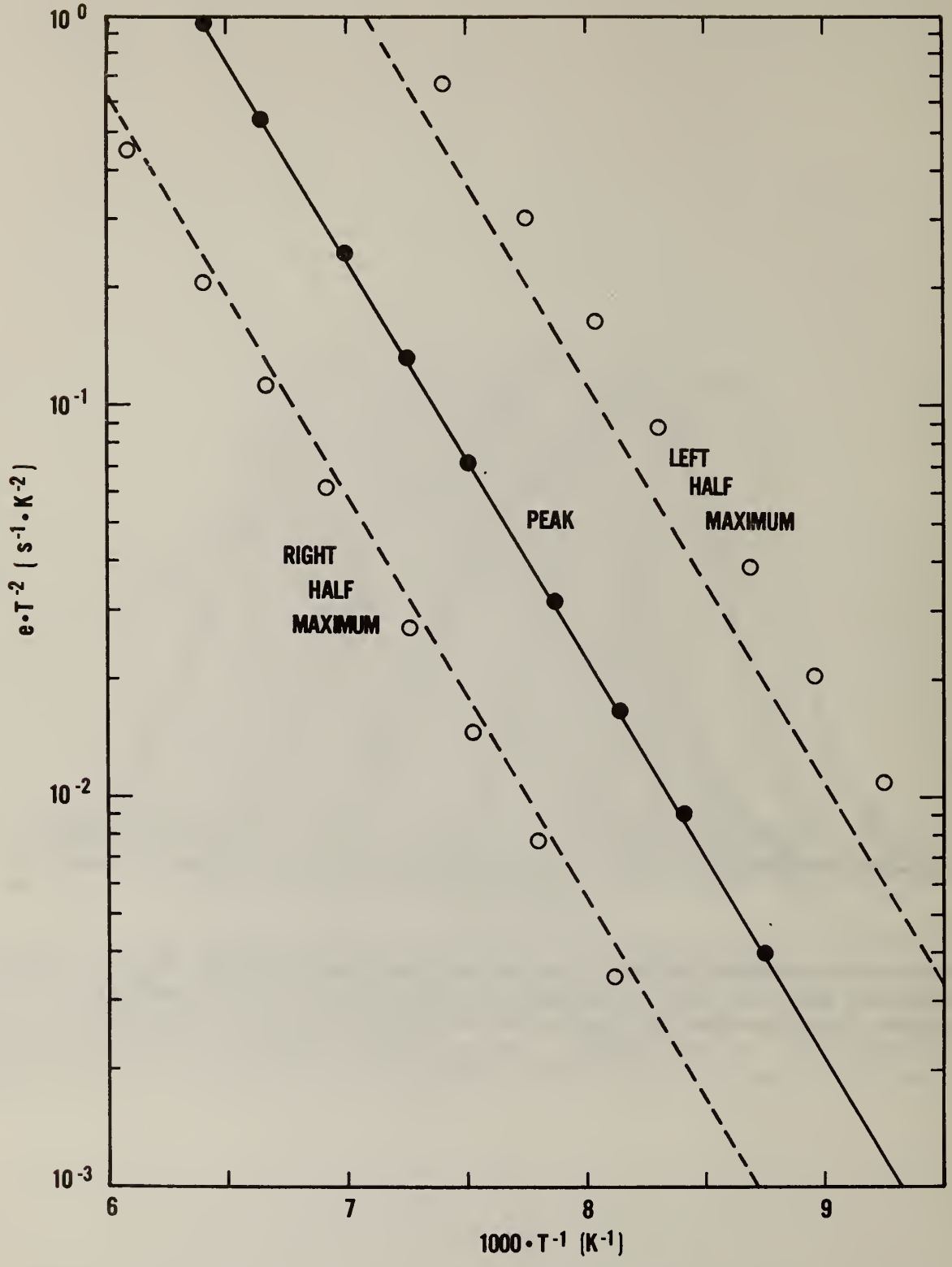


Figure 2-11. The Arrhenius plot and position of the left and right half maximum compared for a single isolated level (solid and dashed lines) and two closely spaced levels (dots).

The published literature on the subject of deep levels in semiconductors is replete with a multiplicity of levels associated with a variety of impurities. In many cases, different authors disagree with respect to the activation energy associated with a particular impurity defect. Platinum levels afford a classic example of this situation. A recent paper [2-12] summarizes the reported levels of platinum from nine sources. There appear to be at least 16 distinct levels. If one accepts the published literature at face value, these different levels may be attributable to differences in the activation energies of platinum defects. For example, different diffusion sources, different diffusion schedules, or different quenching schedules may have been used and may have given rise to different levels. On the other hand, it is also possible that some of the differences could be attributable to measurement error. Even if no errors are made in the measurement of the capacitance transient *per se*, errors in the temperature measurement or failures of any of the assumptions discussed in section 2.3.1.4 could lead to erroneous activation energies.

2.3.2.2 Summary of Deep Level Characterizations

Table 2-3 lists six impurities which were purposely introduced into silicon wafers. The conductivity type of the wafer into which the impurities were diffused is designated by n or p. The deep levels are characterized by the factors ΔE and B of eq (2-1), where ΔE is the thermal activation energy with respect to the majority carrier band edge. The technique(s) used to measure the characterization parameters is(are) also indicated. The defect density was determined from the results of dynathermal thermally stimulated capacitance measurements [2-1] using a commercial, 1-MHz, calibrated capacitance bridge. All device wafers were prepared by NBS. Junctions were fabricated by diffusing boron or phosphorus into 5- to 10-Ω·cm silicon wafers. This was followed by impurity predeposition, diffusion, and then metallization. The last three columns of the table indicate the predeposition technique and the temperature and time for the diffusion.

Table 2-4 compares some of the data of table 2-3 to activation energies published in the literature. The quoted references either used capacitance transient techniques (i.e., DLTS) or thermally stimulated measurement techniques.

The discrepancies between the various results coupled with further discrepancies between results obtained by transient spectroscopy, Hall effect, and optical absorption measurements for the levels of sulfur [2-19], platinum [2-12] and gold [2-20] in silicon illustrate the need for a better understanding of the measurement processes. A further examination by comparing DLTS and ITCAP measurements with each other and with Hall measurements and optical absorption measurements is planned.

2.3.3 Correlation of Deep-Level Defects with Device Electrical Parameters (Objective 2.3)

2.3.3.1 Introduction

A strong correlation between the gold acceptor defect density and electrical parameters such as forward voltage drop and reverse leakage current was re-

Table 2-3. A Summary of Some Deep-Level Characterization Measurements.

Impurity	Substrate Type	ΔE (meV)	B ($\times 10^6$) ($s^{-1} \cdot K^{-2}$)	Measurement Method	Defect Density (cm^{-3})	Impurity Introduction Process		
						Predep.	Diffusion Temp. (°C)	Diffusion Time (h)
Au	*n*	545 ± 5	20 ± 50%	DLTS	4×10^{13}	Evap. (back)	800	24
	p	342 ± 10	200 ± 50%	ITCAP	3×10^{13}	Evap. (back)	825	24
^{32}S	*n*	526 ± 2	9 ± 5%	ITCAP	1.5×10^{13}	Implant (front)	1000	0.42
		235 ± 2	0.01 ± 17%	ITCAP	1.5×10^{13}			
^{34}S	*n*	512 ± 2.6	3.8 ± 15%	ITCAP	1×10^{13}	Implant (front)	1000	0.42
		235 ± 4	0.009 ± 40%	ITCAP	2×10^{12}			
Pt	*n*	197 ± 5	2 ± 6%	DLTS/ ITCAP	5×10^{14}	Spin-on (back)	850	2
	p	300 ± 3	8 ± 3%	DLTS/ ITCAP	5×10^{14}	Spin-on (back)	900	1
Pd	*n*	198 ± 8	4 ± 18%	DLTS	6×10^{14}	Spin-on (back)	1000	2
	p	100 ± 8	4 ± 20%	DLTS	1.5×10^{14}	Spin-on (back)	1000	2
		313 ± 8	7 ± 15%	DLTS	1.5×10^{14}			
Mn	*n*	5.59 ± 8	30 ± 20%	DLTS	1×10^{14}	Spin-on (back)	1000	2

Table 2-4. Comparison of a Selection of Observed Activation Energies Taken from Published Literature With the Results of the Present Measurements.

Impurity	n	p	Reference
Au	0.545	0.342	This Work
	0.56	0.346	[2-13]
	0.547	0.345	[2-14]
^{32}S	0.235, 0.526	-	This Work
	0.276, 0.528	-	[2-15]
Pt	0.197	0.300	This Work
	0.23	0.317	[2-13]
	0.26	0.32	[2-16]
	0.231	0.321	[2-12]
	0.23, 0.34	0.41, 0.33, 0.28, 0.19	[2-17]
Pd	0.198	0.313, 0.100	This Work
	0.22	0.300	[2-13]
Mn	0.56	-	This Work
	-	0.51, 0.44, 0.33, 0.22, 0.17	[2-18]

ported previously [2-6, p. 31]. This implies that it is the deep level which primarily controls these device parameters. In order to explore this relationship further, detailed deep-level measurements were made on a commercial power-rectifier wafer. These results are reported below.

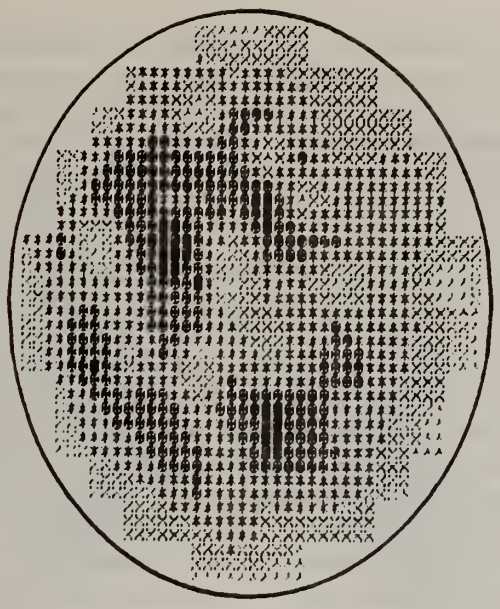
One important aspect of power device operation is the internal power dissipation. In the "on" condition, this dissipation is directly proportional to the forward voltage drop at high injection, whereas for the "off" condition, it is proportional to the reverse leakage current. In section 2.3.3.3, the effect of deep-level defects on these operating parameters is considered.

The wafer mapping of deep-level defects has become an effective technique for visualizing defect density variations and for relating these variations to the measured electrical parameters. In section 2.3.3.4, an efficient means for performing this measurement with the high frequency bridge and a digital processor is described.

2.3.3.2 Defect Density Wafer Maps

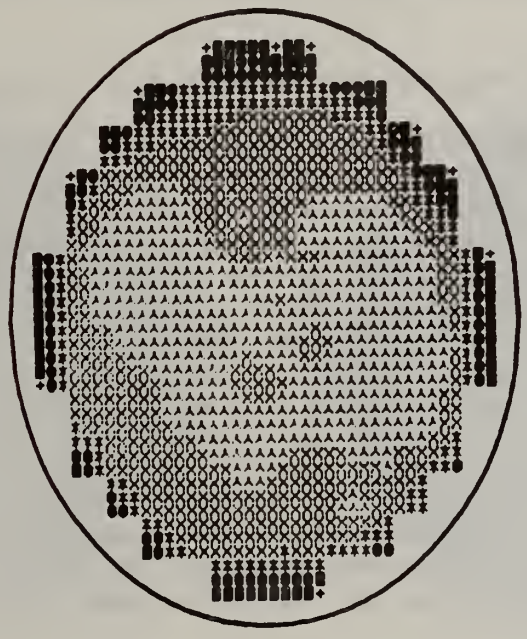
DLTS measurements were performed on a commercial power rectifier wafer. This 50-mm diameter wafer consists of an array of approximately 150 devices capable of handling 16 A, when suitably packaged, with a nominal reverse voltage capability of 600 V. A typical DLTS curve for a device on this wafer shows two well-behaved peaks at low temperatures and more complex behavior at higher temperatures. The two low-temperature peaks indicate the presence of at least two separate levels. The measured activation energies of these levels are 0.191 and 0.301 eV. The level at 0.301 eV exhibits a distortion on its low-temperature side and thus may originate from more than a single level. As the temperature was raised above the level of the 0.301-eV peak, the DLTS signal first passed through a region where its behavior is not fully understood and then exhibited a peak with an apparent activation energy of 0.560 eV.

In order to understand the relationship of these two levels to the device electrical parameters, wafer maps of the defect density corresponding to the two low-temperature peaks were measured. The technique that was used was essentially an ITCAP measurement utilizing the high frequency DLTS bridge and the wafer-probing apparatus (additional details are given in section 2.3.3.4). The wafer maps, shown in figure 2-12, are each labeled with the the corresponding activation energy and the approximate range of the defect density. The defect density range was estimated by scaling the relative values to a determination by a thermally stimulated capacitance measurement of the stronger level (ΔE = 0.301 eV) in one device. Even a casual glance at figure 2-12 indicates that the density variations of the two levels are unrelated. There is neither a correspondence in the distribution nor the range of the defect density. This would suggest that these two levels probably arise from two distinct impurities, impurity complexes, or other defects. Figure 2-13 displays the wafer maps of several electrically measured parameters for the same wafer; these results were reported and discussed previously [2-6, p. 27]. These maps were prepared using the wafer chuck [2-3,2-4]. The density of the defect is indicated by the symbol at the corresponding map position. The measurements were made on a grid corresponding to every third symbol position in figure 2-13 and the intermediate results interpolated and



$\Delta E = 0.191$ eV

$N_t \sim 5\text{-}10 \times 10^9$ cm^{-3}



$\Delta E = 0.301$ eV

$N_t \sim 2.5\text{-}6 \times 10^{10}$ cm^{-3}

Figure 2-12. Wafer maps of the defect density corresponding to two levels of a commercial power-rectifier wafer. Each map is labeled by the activation energy of the level mapped and the approximate range of the defect density for that level. The darkest areas correspond to the highest density and the lightest areas to the lowest density.

plotted to give a clearer picture of the observed variations. The darkest symbols correspond to the highest density and the lightest symbols to the lowest density. Notice that all of these electrical parameters have a very similar distribution across the wafer. In each of these maps, there is an unmistakable radial variation with a contrasting region in the lower left area of the wafer.

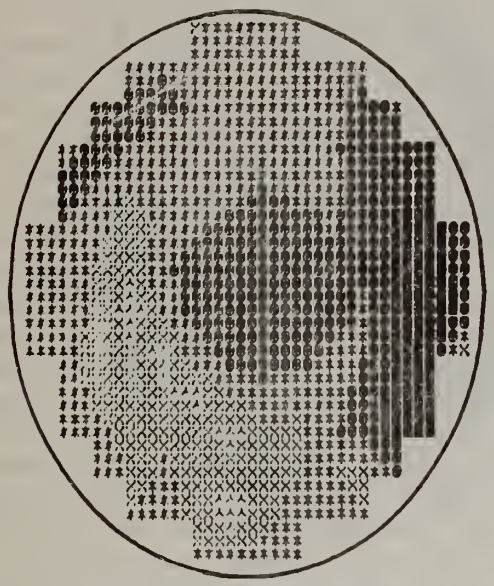
In comparing the features of the electrical parameter maps (fig. 2-13) to the defect density maps (fig. 2-12), the fundamental question to ask is: "Which level (if any) is responsible for the observed electrical behavior?" Inspection of the defect density maps of figure 2-12 with the maps of lifetime-related properties in figure 2-13 reveals little, if any, correlation. This could arise if the lifetime depends on the deeper states that give rise to the higher temperature region of the DLTS signal that is not yet fully understood, or if the lifetime was not dominated by a single level. In principle, the lifetime depends on all deep levels in a multicomponent system such as found in this power rectifier material. In a previous control experiment with a gold-diffused wafer [2-6, p. 27], a single, midgap, majority-carrier level dominated the generation-recombination process, and regions of high defect density had high leakage (i.e., low lifetime). It would appear that this power rectifier material is more complex and its higher temperature DLTS behavior will have to be resolved and interpreted in teams of deep levels before a satisfactory correlation with lifetime-related parameters can be obtained.

2.3.3.3 Forward Voltage Drop and the Onset of High Injection Conditions

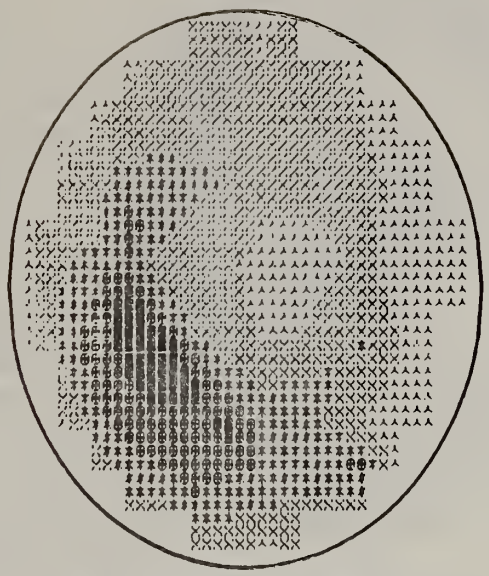
When a rectifier is in its "off" state, the reverse voltage is essentially sustained by the space charge depletion width which forms in the lightly doped region of the junction. Under this condition, the power loss is determined by the reverse leakage current. The reverse leakage current map (fig. 2-13) is seen to be directly related to the lifetime maps: in regions of low leakage (central spot), the minority carrier lifetime is high. The forward voltage drop map of figure 2-13 was made with a current of 10 μA. This is certainly a condition of low injection for these 16-A devices. Figure 2-14 shows a series of forward voltage drop maps of the same wafer at four additional current levels. For currents up to 10^4 μA, the wafer map essentially remains the same. This suggests that, for this range of injection current, the mechanism which controls the forward drop remains the same. At an injection level of 10^5 μA, the distribution has completely changed. The regime of high injection was achieved somewhere between 10^4 and 10^5 μA and the mechanism which controls the forward voltage drop has dramatically changed.

2.3.3.4 An Efficient Technique for Wafer Mapping of Defect Density

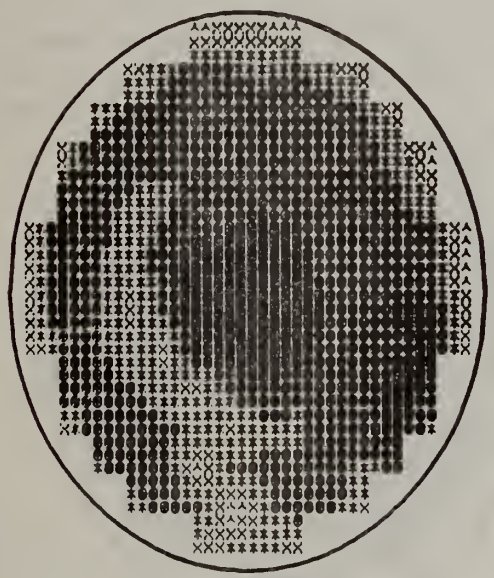
The development of the hot/cold wafer mapping apparatus [2-21, p. 26; 2-3] provided the basis for performing deep-level measurements on whole processed wafers. Early deep-level measurement techniques were limited to thermally stimulated current and capacitance measurements. Wafer mapping of defect density using the thermally stimulated capacitance technique required the thermal cycling of each device on the wafer. Although this technique is straightforward and provides absolute capacitance data, it is very time-



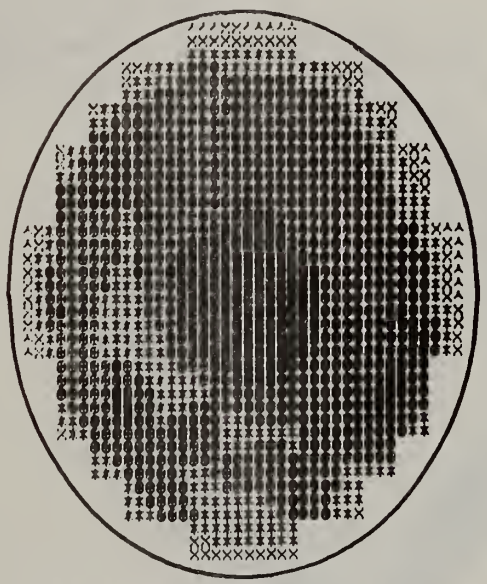
FORWARD VOLTAGE DROP
0.285 - 0.309 V



REVERSE LEAKAGE CURRENT
3.5 - 19.1 nA

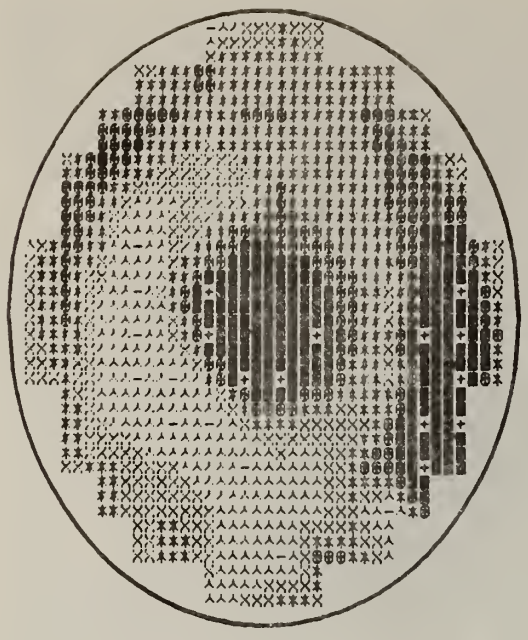


OPEN CIRCUIT VOLTAGE DECAY
LIFETIME 4.9 - 9.4 μs

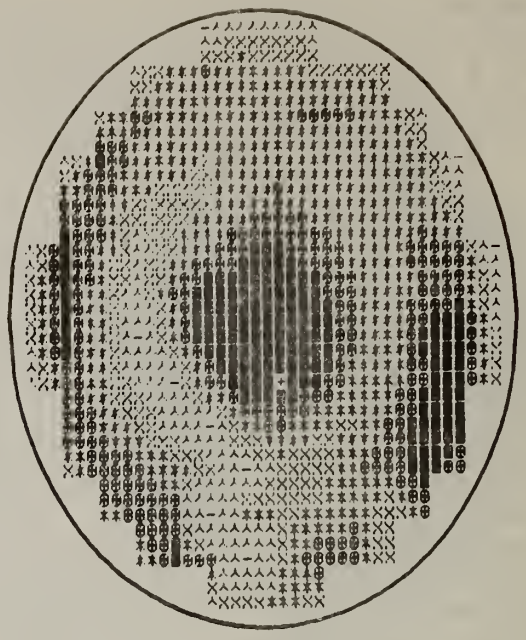


REVERSE RECOVERY LIFETIME
6.8 - 12.7 μs

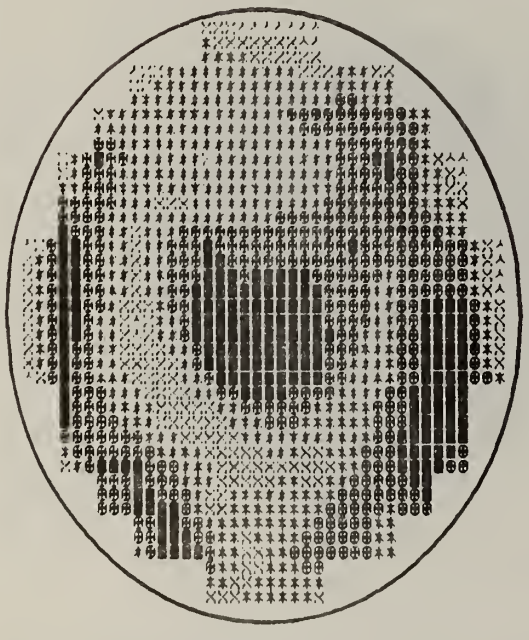
Figure 2-13. Wafer maps of the forward voltage drop (at 10 μA), reverse leakage current (at -15 V), and results for two different minority carrier lifetime measurements. In each case, the darkest regions correspond to the highest values of the parameter mapped.



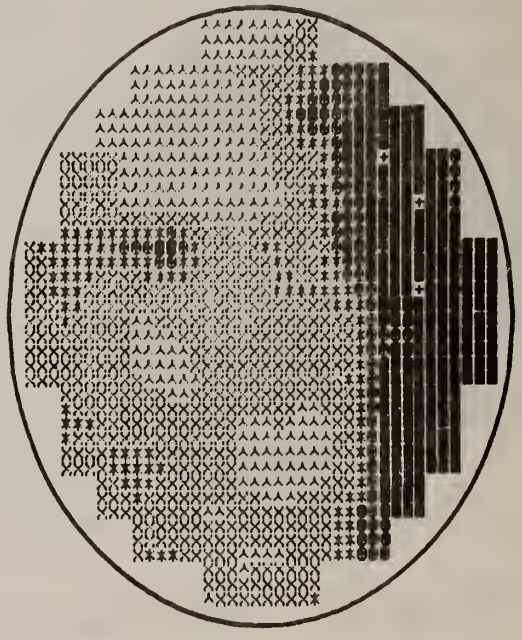
0.368 - 0.376 V
@ 10^2 μA



0.452 - 0.462 V
@ 10^3 μA



0.568 - 0.577 V
@ 10^4 μA



0.729 - 0.750 V
@ 10^5 μA

Figure 2-14. Forward voltage drop maps of the rectifier wafer at different current levels. The highest current, 10^5 µA, corresponds to a current density of about 1.6 x 10^6 µA cm^{-2}.

consuming because thermal cycling is required for the measurement of each device.

The latest addition of the high frequency bridge capability of figure 2-2 brought with it a new method for performing the wafer mapping measurement. The method utilizes the high frequency bridge and makes the measurement under isothermal conditions. The wafer is maintained at constant temperature (its variation could be plus or minus a few degrees). This temperature is maintained by a control system which provides heating power to balance the cooling produced by a constant flow of cold nitrogen vapor. Slight variations in the temperature are not serious because only the relatively insensitive magnitude of the capacitance transient ($[C_f - C_i]$ in fig. 2-1) and not the exponentially dependent decay rate is the important factor. The temperature is adjusted to achieve capacitance decay time of 20 to 30 ms with a 50-ms repetition period. This capacitance transient signal is captured directly by a digital processor which can be programmed to store and average many transients. In this way, the signal-to-noise ratio (which could be less than one for situations involving low defect densities) can easily be improved a hundred- to a thousand-fold. Generally, sampling a 50-ms transient for times ranging from 20 to 200 s is sufficient to obtain the magnitude of the transient with the desired accuracy. This compares with the nominal time of 15 min to cycle each device using the thermally stimulated technique. The combination of the high frequency bridge and the digital processor has allowed the measurement of defect densities more than 10^{-4} below the bulk carrier concentration. The sensitivity of the high frequency bridge and the arithmetic capability of the digital processor provides the capability for improved deep-level characterization of trace impurities. It is anticipated that these techniques will find future application to the characterization of impurities at concentrations below the level where the transient behavior can be observed directly.

3. Spreading Resistance Measurements

by

J. R. Ehrstein

3.1 Objectives

The overall objective of this task is to coordinate standardization activities of preferred procedures for specimen preparation prior to spreading resistance measurements on thyristor-grade silicon and on related thyristor structures. The specific objectives are as follows:

3.1 Prepare proposed standard practice for preparation of spreading resistance specimens in ASTM format; submit to ASTM Committee F-1 for consideration.

3.2 Coordinate multilaboratory study to test effectiveness of chosen specimen preparation for spreading resistance measurements.

3.2 Background

The importance of dopant distribution in thyristor substrate material and in fabricated devices, as well as the traditional use of spreading resistance as a semiquantitative measure of these distributions, was detailed in last year's report [3-1]. A specimen surface preparation procedure for high resistivity *n*-type silicon, polishing with diamond (0.5- and 3-μm nominal particle size) in nonaqueous fluid, was identified and discussed in last year's report. This procedure offers 1) improved reproducibility of average spreading resistance compared to results on specimens prepared with colloidal silica polishing and 2) reduced scatter of individual measurements compared with results on lapped specimens. Tests were also performed on the effect of using 0.5-μm diamond polishing on a range of (111) *n*-type and (111) *p*-type bulk calibration specimens covering nearly 6 decades of resistivity. Diamond polishing of these specimens was shown to give nearly the same calibration response as colloidal-silica polishing, except that more repeatable results were obtained for the high resistivity *n*-type specimens when using diamond polishing.

3.3 Accomplishments This Year

3.3.1 Documentation of Preferred Procedures

A summary of the results of the use of diamond polishing for high resistivity *n*-type silicon was presented at the February 1979 meeting of ASTM Committee F-1 on Electronics in San Diego. As a result of this presentation, preparation of a draft procedure detailing such specimen preparation prior to spreading resistance measurements was approved by the Electrical and Optical Measurements Subcommittee of Committee F-1. The initial draft was slightly modified following discussion at the Philadelphia Committee meeting in June.

The revised draft, which is included as Appendix C of this report,* is scheduled to be formally letter balloted for Committee approval in the first quarter of FY-80.

3.3.2 Multilaboratory Pilot Study

A multilaboratory study of the repeatability and reproducibility of spreading resistance measurements has been agreed upon by ASTM Subcommittee F-1.06. Eleven laboratories have agreed to participate. Use of any one of three surface preparation procedures is allowed in the study: colloidal silica polishing, diamond polishing, and alumina lapping. The test has been designed to include specimens covering a wide range of resistivities in both *n*- and *p*-type silicon and both (100) and (111) crystallographic orientations. Specimens for this test have been collected and are in the final stages of preparation. The design of the test requires that replicate sets of specimens be sent to each laboratory to speed completion of the test. The replicate sets are being obtained by cutting the individual silicon slices into a number of rectangular chips; the chips from the central region of the slices are being used to generate the replicate specimen sets. The design requires analysis of repeatability and reproducibility as a function of specimen preparation, conductivity type, and resistivity.

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4. Neutron Transmutation Doped Silicon Studies

by

D. R. Myers

4.1 Objective

The objective of this task is to determine the technical impediments to a more effective utilization of neutron transmutation doped (NTD) silicon for thyristor production.

4.2 Background

The major use of neutron transmutation doped (NTD) silicon at present is for the fabrication of high-voltage thyristors. These devices are used, for example, as elements in systems that convert power from alternating current to direct current and the reverse [4-1]. Direct-current power transmission systems are being viewed with increasing favor as a potential solution to such problems as grid connections, underwater power transmission, and long-distance overhead power transmission [4-1]. As the attractiveness of dc power transmission grows, demands on absolute thyristor performance also grow, with an ever-increasing need for higher voltage ratings, higher current-carrying capability, and improved efficiency.

A major advance in raising the ultimate performance of the thyristor came with the application of the neutron transmutation doping process [4-2] to silicon thyristor fabrication [4-3]. The NTD process involves the irradiation of a silicon ingot inside a nuclear reactor, where the capture of a thermal neutron by the naturally occurring isotope ^{30}Si leads to the formation of a ^{31}P atom by radioactive decay. Since the isotope ^{30}Si is uniformly distributed within the crystal, the NTD process has the potential of producing an extremely uniform phosphorus doping concentration. The unprecedented uniformity in doping level possible with the use of transmutation doping holds great promise for significant improvements in yield and also for ultimate device performance [4-4].

The benefits associated with the neutron transmutation doping process do not come without disadvantages, all of which are related to the fact that the production of NTD silicon requires exposing the silicon to a neutron flux inside an atomic reactor. Specifically, these disadvantages are the irradiation costs and procedures, radioactivity safeguard considerations, and the radiation damage produced inside the silicon. Detailed estimates of the cost of neutron doping are not available. However, barring a major change in technology, this cost is expected to follow traditional inflationary trends [4-5] unless it is influenced by the increased use of NTD silicon for devices other than thyristors. Effective radiation safeguards which have been developed and are in use limit the maximum dopant density which can be introduced into the silicon, but this limit exceeds the dopant density ordinarily required for high power devices.

The major technical concern in the use of NTD silicon is the radiation damage produced in the silicon lattice by the irradiation and the effects that this

damage has on device fabrication and on ultimate device performance. In this regard, neutron transmutation doping is very similar to another particle irradiation technology that produces extensive lattice damage in silicon — namely, ion implantation. Many of the difficulties in using implantation have been solved; as a result, ion implantation has become the accepted means of dopant introduction for silicon device fabrication, due to its increased capability over conventional predeposition technology for dopant uniformity and absolute dopant-level control. While differences exist between the types of damage produced by ion implantation and that produced by neutron transmutation doping, the development of effective procedures for annealing of ion-implanted silicon suggests that equally effective techniques can be developed for NTD silicon.

4.3 Accomplishments

During this reporting period, a survey was conducted involving manufacturers and users of NTD silicon, as well as research workers in universities, government laboratories, and private industry involved with the NTD process. The major needs identified by this study are:

(1) Development of a fast yet effective way to characterize the neutron velocity distribution in a reactor that avoids the limitations of the commonly used copper-cadmium ratio test.

(2) A comprehensive study to determine the interaction of chemical and structural imperfections during annealing of NTD silicon and their effects on subsequent doping or lifetime control measures, especially for annealing in the temperature range 700°C to 1200°C. This research should focus on assessing ultimate performance and yield limitations, as well as on developing a more complete understanding of the radiation-damage recovery process in silicon.

(3) The development of effective techniques for qualifying NTD silicon production, involving the evaluation of high-level minority-carrier lifetime, low-level minority-carrier lifetime, and space-charge generation lifetime, and the correlation of these quantities to lifetime as measured by such commonly applied techniques as diode reverse-recovery, open-circuit voltage decay, and surface photovoltage.

A separate report detailing the results of this study has been published [4-6].

5. Zinc Oxide Varistor Studies

by

R. I. Scace

5.1 Objectives

The objective of this task is to determine the measurements and analysis needs to aid in the application of zinc oxide varistor technology to the manufacture of high-voltage limiters for surge arrester applications.

5.2 Background

A varistor is an electrical resistor whose resistance is not constant, but is a function of some externally imposed variable. The varistors under discussion have a resistance which is strongly dependent on the applied voltage, or electric field. The sense of the resistance change is such that the resistance drops with increasing voltage.

Devices of this kind have found wide use as voltage limiters for many applications. When the applied voltage rises, the resulting decrease in the resistance of the device causes the current through it to increase much more rapidly than Ohm's law would predict; the voltage drops in the source impedances in the circuit likewise increase, and the voltage rise at the varistor location is held to a lower value than would otherwise be the case. The energy of the voltage surge is dissipated as heat in the varistor and in other resistive parts of the circuit.

There are many types of devices which are useful for voltage limiting. They include Zener diodes, spark gaps, and varistors made from silicon carbide or carbon blocks, as well as varistors made with zinc oxide. It should be recognized that each of these kinds of voltage limiters has particular areas of application for which it excels over the others.

For transmission line service, the standard product for surge limiting (called an "arrester") is an silicon carbide varistor in series with a spark gap. The gap is needed because the varistor has only a limited variation in its resistance. It cannot meet the simultaneous requirements that its conducting resistance be low enough for effective voltage limiting and that its standby resistance be high enough that no significant heating of the varistor occurs. The varistor is only connected to the transmission line when a voltage surge has broken down the gap.

This device thus has two principal shortcomings. First, the gap must fire, which requires a substantial overvoltage; further, the limited resistance range of silicon carbide does not allow the varistor to clamp the voltage as well as one would like. Both of these factors lead to the overall result that these arresters can only hold the maximum voltage during a surge to about 1.8 times nominal at best; twice nominal is common.

5.3 Accomplishments

During FY-79, visits were made to several manufacturers to discuss their programs for development of zinc oxide lightning arresters and to learn about measurement problems that they may be experiencing. The literature on zinc oxide varistors has been critically reviewed to determine how well the behavior of the devices is understood and in which direction new research should go. The major findings identified by this study are:

(1) A model for varistor action, based on recognized semiconductor theory and free of arbitrary constants, has recently appeared in the literature. It is successful in explaining all of the observed electrical phenomena in the varistor except polarization effects.

(2) Knowledge relating the formal model and varistor electrical properties to the structure of the ceramic and the distribution of charges in the interface region is deficient.

(3) Some of the companies working in the field report difficulty in making accurate electrical measurements on such highly nonlinear devices over the very wide range of currents involved.

(4) There are concerns among these companies regarding how the results of accelerated life tests should be used as predictors of service life for this new product.

A separate report detailing the results of this study has been published as an NBS Interagency Report [5-1].

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APPENDIX A

The Analog Gate Circuit

An analog gate circuit for suppressing the DLTS signal during the zero-bias charging period is shown in figure A-1. The integrated circuit, IC1, has a TTL-compatible input for initiating the synchronizing pulse. A monostable multivibrator triggers on the rising edge of the input signal (arrow). The optical isolator, IC2, acts as a level shifter and initiates the action of IC3, IC4, and IC5. IC3 and IC4 are adjustable width monostable multivibrators, with IC4 triggering on the rising edge of the IC3 output. Thus, IC3 provides an adjustable delay while IC4 provides an adjustable gate width. IC5 is an open collector driver which provides the necessary drive for the actual analog gate device (IC6). As long as the gate input to IC6 remains at -5 V, the output signal is clamped at zero; with the gate at +5 V, the output signal is unaffected by the presence of IC6.

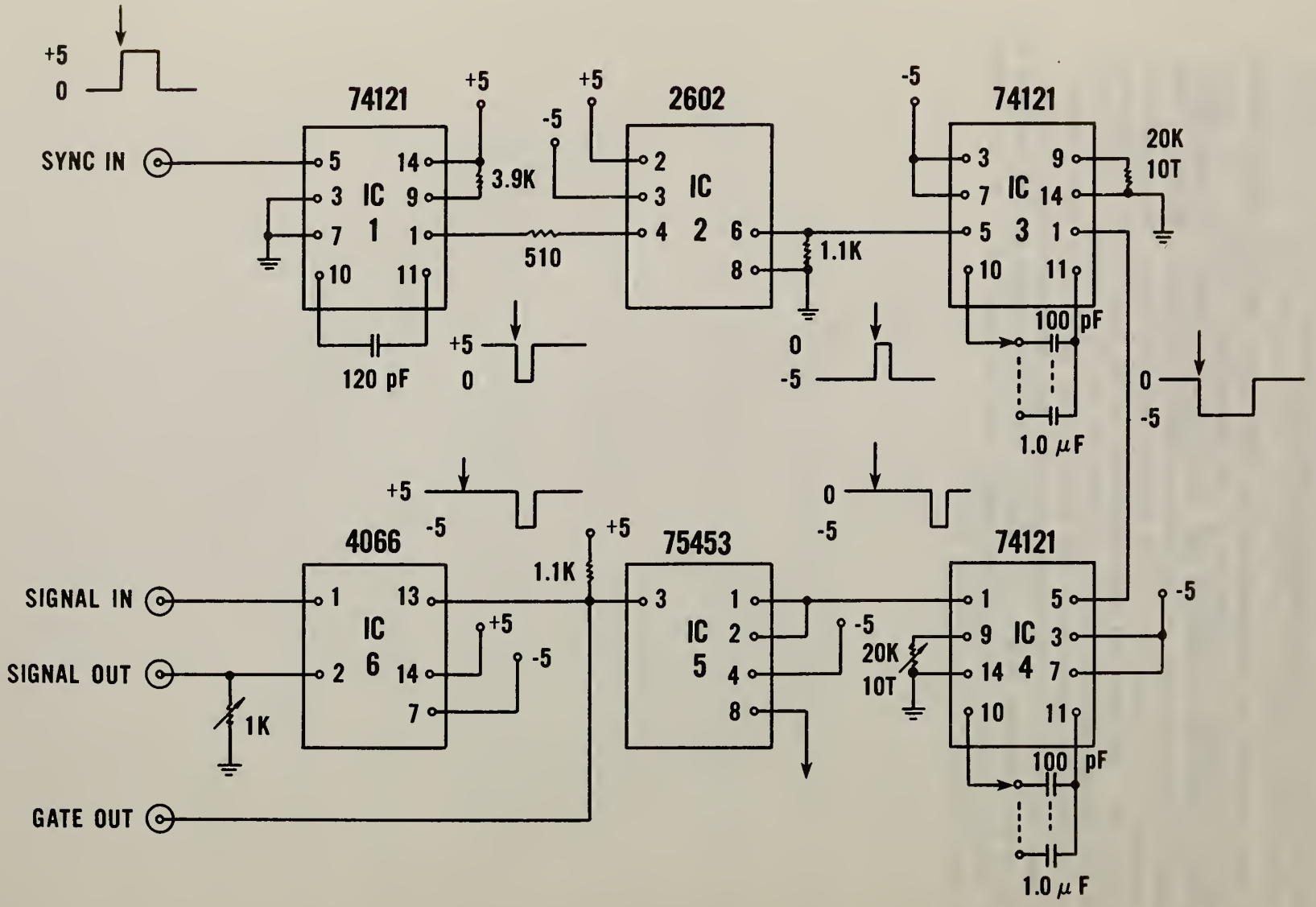

Figure A-1. Schematic diagram for the analog gate circuit.

APPENDIX B

Modified Bridge Circuit*

A very simple modification to the bridge circuit of figure 2-2 is discussed here. It offers a simplification in the operation of the bridge and a simple way to get absolute values of differential capacitance. The modified circuit is shown in figure B-1. In this circuit, the pulse generator output is connected to the center tap of the rf transformer rather than the device under test. The advantage of this configuration is that the pulse generator impedance is now isolated from the device impedance. Hence, the operation of the bridge is independent of the pulse generator impedance. The second modification is the addition of capacitor C_C in parallel with the device under test. This capacitor is a carefully calibrated variable capacitor (0 to 4 pF) which can be added to the depletion capacitance of the device under test to accurately measure the amplitude of the capacitance transient as viewed on the oscilloscope screen.

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*These modifications were suggested and implemented by R. D. Larrabee.

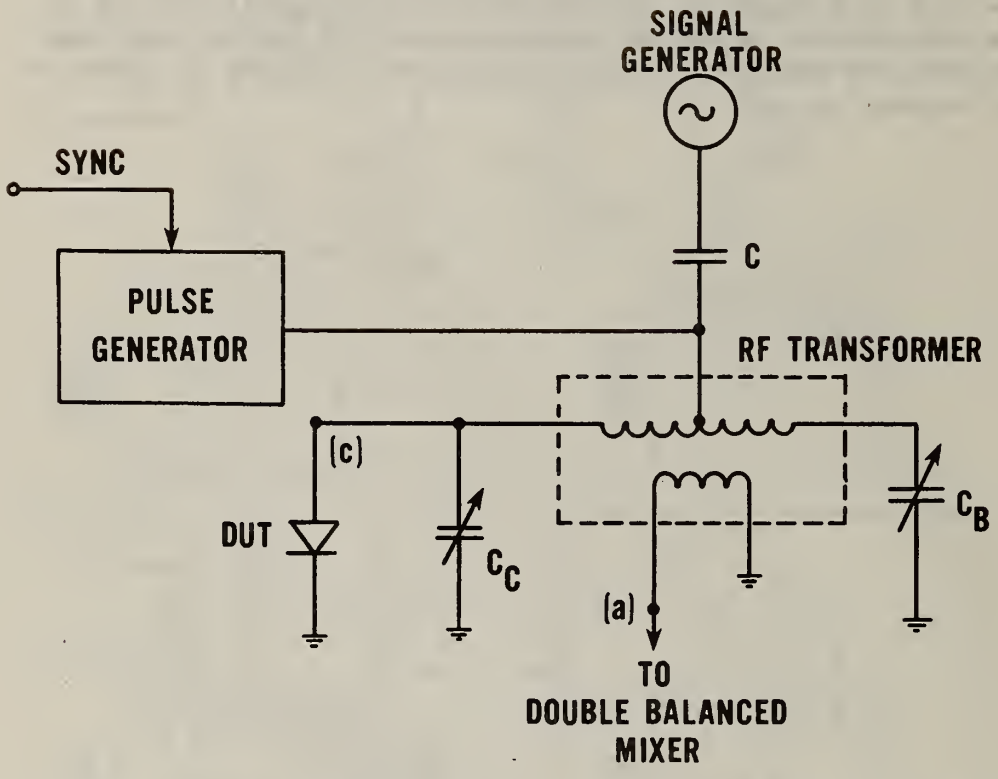


Figure B-1. A simple modification to the high frequency bridge which improves its operation and calibration.

APPENDIX C

Draft of Proposed Recommended Practice

Preparation of High Resistivity n-type Silicon for Spreading Resistance Measurements[1]

ASTM Committee F-1 Document No. 6B41
Draft No. 2
Date: June 28, 1979
Prepared by: J. R. Ehrstein
(301) 921-3625

ASTM Committee F-1 on Electronics
Subcommittee 6 on Electrical and Optical Measurements

1. Scope

1.1 This recommended practice covers the surface preparation of (111) n-type silicon prior to measurement of resistivity variation by the spreading resistance technique. This procedure offers improved reproducibility of spreading resistance measurements for (111) n-type silicon specimens with room temperature resistivity above 1 Ω·cm. No upper limit is known on resistivity values for which this procedure provides improved spreading resistance measurements on (111) n-type specimens. This procedure can also be applied to (111) n-type silicon specimens below 1 Ω·cm, and to p-type silicon specimens. Separate procedures are given for preparation of large area specimens for measurement of lateral resistivity variation and for preparation of bevel-sectioned specimens for measurement of vertical variation of resistivity.

2. Summary of Practice

Silicon specimens are polished using fine grain diamond compound in a nonaqueous fluid. Following polishing, residual polishing is removed by organic solvent. Polishing of silicon slices of other large area specimens is done against a nonwoven polishing cloth. Bevel polishing of small specimens is done against a frosted glass surface.

3. Significance

3.1 Spreading Resistance Measurements are used to measure resistivity variation in silicon crystals and semiconductor devices. The reproducibility of spreading resistance measurements on silicon specimens is known to depend on the manner of specimen preparation. Interpretation of spreading resistance measurements depends in turn on the reproducibility of test specimen measurements and on the reproducibility of calibration specimen measurements.

3.2 This procedure gives a high degree of reproducibility to spreading resistance measurements and offers particular improvement over other preparation techniques on (111) n-type material with resistivity above 1 Ω·cm.

4. Interferences

4.1 Polishing of silicon with diamond causes light but controllable and uniform scratch damage to the silicon surface. Nevertheless, such uniform damage is compatible with spreading resistance measurements having very low scatter. Contamination of the polishing medium with hard foreign particles can cause random heavy scratch damage to the specimen. Such heavily damaged regions, if encountered by the spreading resistance probes, may yield erratic measurements.

4.2 Contamination of the specimen with water subsequent to polishing may adversely affect the reproducibility of spreading resistance measurements and should be avoided.

5. Apparatus

5.1 Top surface diamond polishing

5.1.1 Oscillating tub polisher or similar small laboratory-scale polishing machine capable of providing randomized motion of silicon specimen over polishing pad.

5.1.2 Mounting fixtures to support and apply vertical load to silicon specimen during polishing.

5.1.3 Nonwoven cloth polishing pad of a texture specified as compatible with the grain size of diamond used during polishing. Polishing pad should be adhesive-backed for attaching to a plate of glass, or similar hard material which provides flat rigid support during polishing.

Note 1: The preferred material is of a type called a "chemotextile" and sold under such names as Pellon Cloth, Kempad, or Texmet.[2]

5.1.4 Plate of glass or similar hard material compatible with chosen polishing machine.

5.2 Diamond bevel polishing

5.2.1 Glass plate of suitable area for convenient use, which has been given a frosted surface by lapping with water slurry of nominal 5 to 12 μm aluminum oxide, or similar abrasive, and thoroughly cleaned subsequent to lapping.

5.2.2 Mounting fixtures for holding silicon specimen at desired beveling angle during bevel-polishing process.

5.3 Hot plate capable of 150°C.

6. Reagents and Materials

6.1 Synthetic or natural diamond with grain size in the range 0.5 to 3 μm, inclusive, for top surface polishing of large area specimens. Such diamond should be bought already suspended in a nonaqueous liquid or paste carrier.

6.2 Synthetic or natural diamond with grain size in the range 0.1 to 0.5 μm, inclusive, for bevel sectioning of small silicon chips prior to depth profiling. Such diamond should be bought already suspended in liquid or paste carrier.

Note 2: For fixed diamond grain size, little difference should be found in the surface finish of the silicon as a function of whether the diamond is natural, single crystal synthetic, or poly crystal synthetic. The

[2]Pellon Cloth is available from the Pellon Corp., Chelmsford, MA 01824; Kempad is available from the Glennel Corp., Chester Springs, PA 19425; Texmet is available from Buehler Ltd., Evanston, IL 60204.

predominant causes of variation in silicon finish are expected to result from 1) the uniformity of particle size in the diamond grit, 2) the inclusion of a large fraction of needle-shaped grains called "fines," in addition to the preferred symmetric grains called "blocky diamond," and 3) in the case of diamond suspended in paste, the uniformity of the diamond distribution in the paste.

6.3 Suitable nonaqueous solvent for removing diamond slurry subsequent to polishing. The choice of solvent is governed in part by the composition of the carrier liquid or paste. The supplier of the diamond compound should be consulted regarding appropriate solvent. However, acetone ($(CH_3)_2CO$) and methanol (CH_3OH) are known to work well for removing many commercial diamond compounds.

6.4 Glycol phthalate or other wax of similar low melting temperature.

7. Procedure

7.1 Top surface polishing

7.1.1 If not previously done, place several drops of diamond polishing slurry at random locations of polishing pad surface. Spread drops of slurry reasonably uniformly over pad to give damp pad surface. When the slurry is properly distributed, there should be no freestanding layers of slurry. If the diamond is suspended in paste, application of paste to the pad should also be sparing.

Note 3: For use with large area specimens, the appropriate diamond grain and, in part, the type of diamond to be used should be compatible with the starting surface texture of the silicon, which may range from as-sawed to prepolished, and the load which is applied during polishing. The breakdown mechanisms differ somewhat for the different types of diamond. Consequently, the size and type of diamond should be chosen to give acceptable cutting rate for the specimen and machine conditions which will be used.

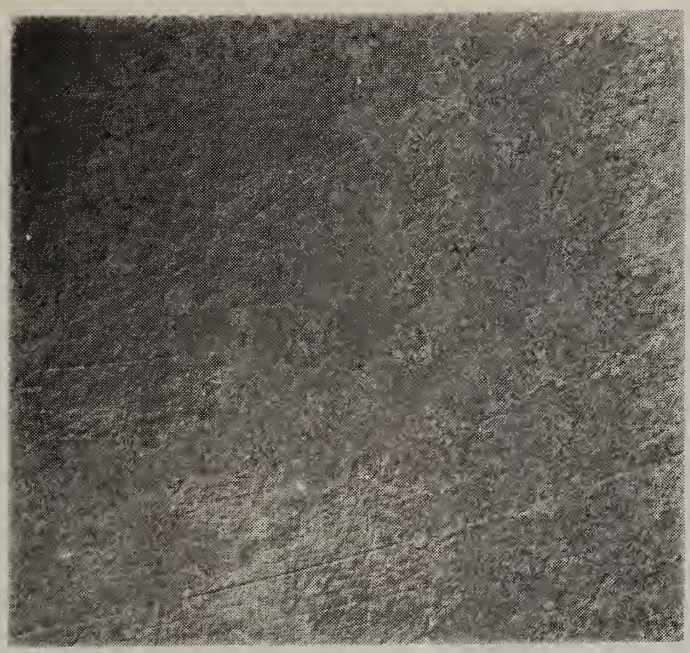
7.1.2 Mount silicon specimen on mounting block using chosen wax. Allow to cool.

7.1.3 Assemble specimen, mounting-block, and mounting fixture and place on polishing machine.

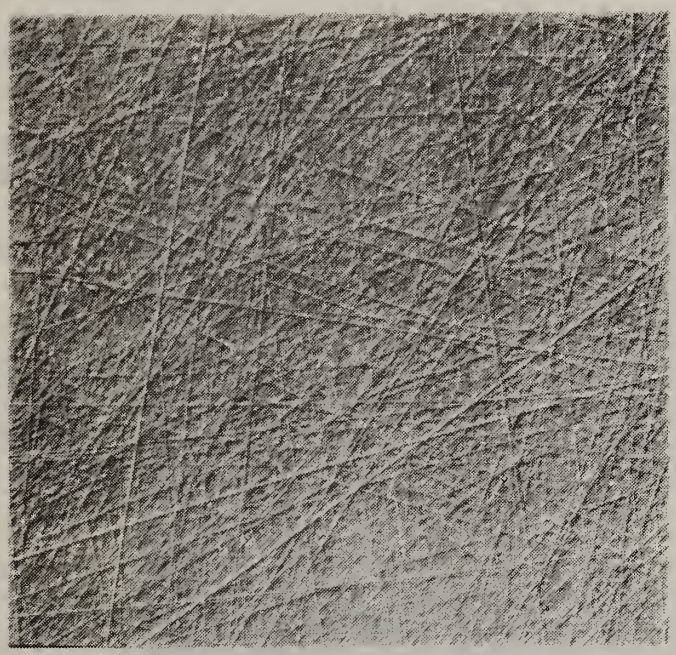
7.1.4 Polish until specimen surface exhibits a uniform density of random-direction scratches comparable to that shown in figure 1. Inspection should be under at least 30X magnification with oblique illumination after polishing slurry has been removed from the silicon surface.

Note 4: The time required to reach a uniform surface finish will depend on specimen surface area size of diamond grains, static load applied, and rate of movement of the specimen surface over the polishing pad.

7.1.5 When an acceptable surface finish has been reached, thoroughly swab or flush the specimen with suitable organic solvent (as determined from



(a)



(b)

Figure 1. Surface texture of large area silicon specimen polished with diamond against chemotextile pad, (a) 0.5-μm diamond, (b) 3-μm diamond. 220X magnification.

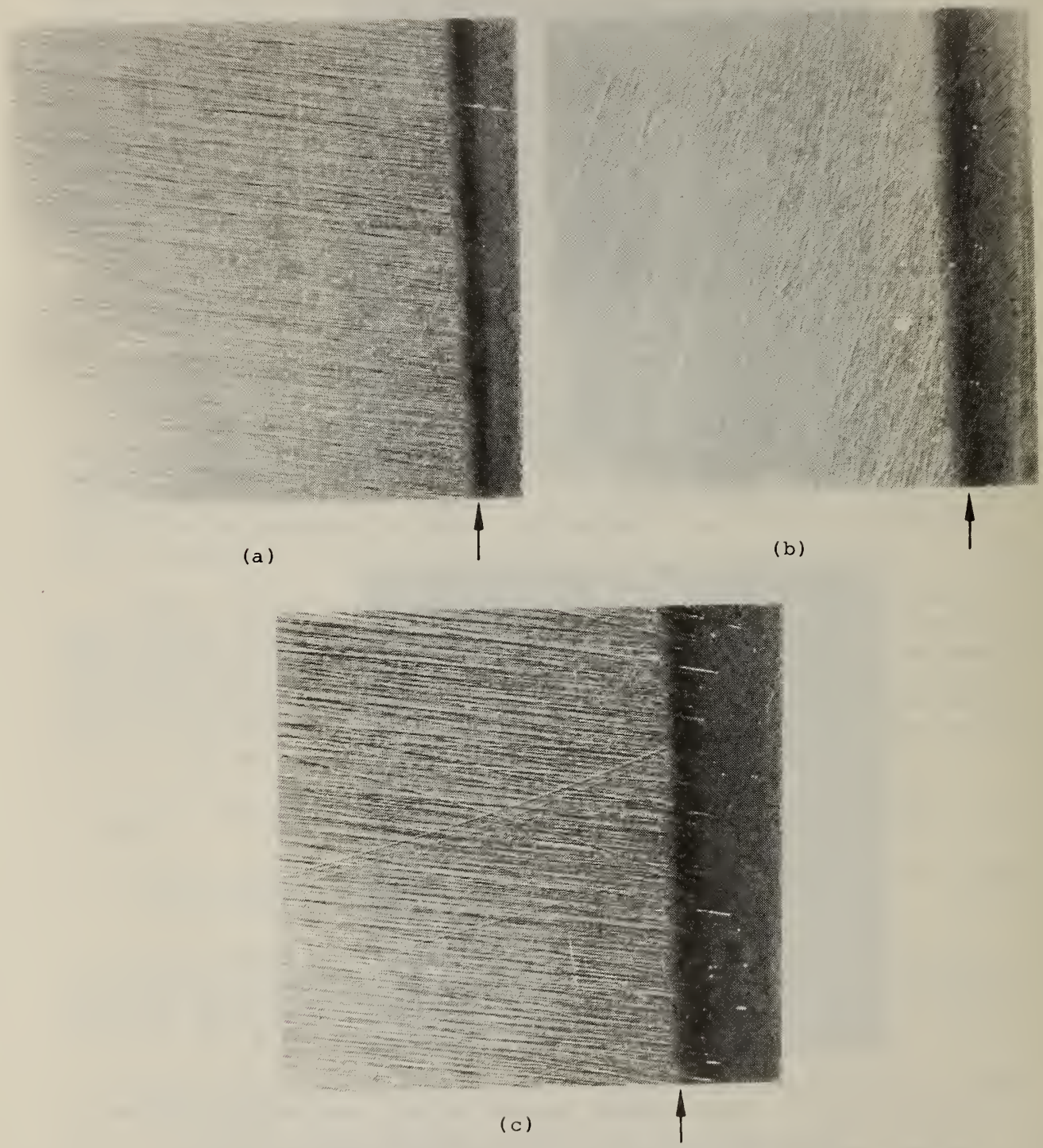


Figure 2. Surface texture of silicon specimens bevel-sectioned with diamond against ground glass surface, (a) 0.1-μm diamond, reciprocating motion, (b) 0.1-μm diamond, figure-eight motion, (c) 0.5-μm diamond, reciprocating motion. 220X magnification. (Vertical arrows denote edge of bevel.)

supplier of diamond slurry) to remove all diamond slurry residues. Blow specimen surface dry prior to measurement.

Note 5: Some polishing slurry adheres to the specimen and mounting fixture and is lost every time a specimen is removed and cleaned. It is necessary therefore to replenish the slurry on the pad regularly with a few drops of fresh slurry.

Note 6: The coarseness of the scratch damage on the specimen surface is related to the size of diamond grit used.

7.2 Bevel angle polishing

7.2.1 Prior to each specimen beveling, clean the frosted glass surface by swabbing with appropriate solvent using a lint-free paper or cloth.

Note 7: Because of the rigidity of the glass surface, extreme excess damage to the beveled silicon surface can result from contamination of the polishing slurry with foreign material whose size is larger than the diamond grit.

7.2.2 Apply a small amount of diamond slurry or paste to the surface of the glass and distribute uniformly by use of a clean cotton swab or other clean soft applicator. The distribution of the polishing compound should leave a thin film over an area whose dimensions are several times larger than the lateral dimensions of the fixture used to support the beveling block.

7.2.3 Polish the specimen by orbital, figure-eight, or reciprocating movement of the polishing fixture over the glass plate.

7.2.4 Clean and inspect specimen periodically to determine whether an adequate amount of specimen surface has been exposed by beveling.

7.2.5 Repeat 7.2.3 and 7.2.4 as necessary to obtain adequate bevel surface.

Note 8: At the beginning of the beveling process, an extremely small area of silicon supports the static load of the polishing assembly, and pressures on the silicon are extremely high. To minimize the possibility of fracture of the edge of the silicon chip, it has been found advisable to begin bevel polishing with a relatively slow rate of motion of the polishing assembly.

7.2.6 When the desired amount of specimen surface has been exposed by beveling, thoroughly clean the specimen by flushing or swabbing with the appropriate organic solvent. Inspect the beveled surface for quality of finish using at least 30X magnification and oblique or dark-field illumination. Compare with figure 2 which shows results obtainable with different size diamond in the range specified and for two types of motion during polishing.

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15. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from the rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes.

The major tasks under this project are (1) to evaluate procedures for the effective utilization of deep-level measurements to detect and characterize defects which reduce lifetime or contribute to leakage current in power-device- grade silicon, (2) to coordinate standardization activities of preferred procedures for specimen preparation for spreading resistance measurements on thyristor-grade silicon and structures, (3) to determine technical impediments to a more effective utilization of neutron transmutation doped silicon for thyristor production, and (4) to determine the measurement and analysis needs to aid in the application of zinc oxide varistor technology for the manufacture of high voltage limiters for lightning arrester application.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

dc transmission; deep-level measurements; energy conservation; measurement methods; neutron transmutation doped silicon; power-device grade silicon; resistivity variations; silicon; spreading resistance measurements; thermally stimulated measurements; thyristor materials measurements; thyristor measurements; zinc oxide varistors.

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