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Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened Charge-Coupled Device (CCD) Imagers: Annual Report, December 1, 1978 to November 30, 1979

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Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
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U.S. Department of Commerce
Washington, D.C. 20234

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Prepared for
The Charles Stark Draper Laboratory, Inc.
Cambridge, MA 02139

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Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened Charge-Coupled Device (CCD) Imagers: Annual Report, December 1, 1978 to November 30, 1979

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Abstract

This project is to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. During the period covered by this report, consultation was provided to The Charles Stark Draper Laboratory, Inc. (CSDL) and to CSDL contractors on the implementation of test structures developed during the previous year of this project. In addition, the results of measurements on buried channel gated diodes and buried layer metal-oxide-semiconductor field-effect transistor (MOSFET) direct-current (dc) profilers are reported. Further advances in the development of the integrated gated-diode electrometer are also reported.

1. Introduction

This report describes work performed for The Charles Stark Draper Laboratory, Inc. (CSDL) under CSDL Prime Contract N00030-79-C-0096 issued by the Department of the Navy, Strategic Systems Project Office, for the period beginning December 1, 1978 and ending November 30, 1979. This work constitutes a program entitled "Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers." The present program is a continuation of activities initiated in FY-1978.

2. Objective

This project is intended to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. The goals are to develop the tools which enable CCD manufacturers to measure critical device and process parameters and which provide the end users with information based upon measurements which accurately characterize critical CCD performance. In addition, the test structures and test methods developed are directed at minimizing the hardware and software required to fully implement a suitable test program at CCD manufacturing facilities.

3. Summary of Work Completed in FY-1978

Two new production-compatible advanced test structures were developed during the first year of the program. The new test structures are the integrated gated-diode electrometer and the MOSFET dc profiler. The first annual report for this project outlines the conceptual and experimental background of the new advanced test structures, describes the associated theory and analysis, and de-

tails the test methods. It also includes a collection of test structure designs and specifications for production-compatible test structures [1].

4. Results of Work During This Period

The following activities were carried during the period covered by this report.

Consultation to CSDL was provided on the design and inclusion of advanced test structures in new CCD mask sets, the measurement and analysis of radiation test effects in these devices and correlation with CCD performance, and general aspects of the use of test devices for process verification and analysis.

In addition, interactions occurred with CSDL contractors concerning implementation of the test structures developed during the first year of this program [1], layout of test structures on CCD chips and in test patterns, and metrology associated with test structures.

A variety of technical efforts were carried out to meet needs arising from contractors' activities or from CSDL requests. For example, contractor-designed gated diodes were measured on six CCD chips which were received from CSDL (see sec. 4.1) while buried layer ion implantation used for radiation-hardened CCD imagers was profiled using the MOSFET dc profiler (see sec. 4.2).

Continued development of the integrated gated-diode electrometer was carried out as detailed in section 4.3.

Several technical talks were presented and papers were prepared for publication on the integrated gated-diode electrometer and on the analysis and applications of test structures in general as detailed in section 4.4.

4.1 Gated Diode Measurements

Two buried-channel gated-diode structures were measured on each of six CCD chips. The reverse-bias leakage current measured as a function of gate voltage for these devices is shown in figures 1 through 7. The curves show that for reverse-bias voltages greater than about 2 V, the buried layer under the gate can be depleted through to the substrate without inverting the surface. The shapes of the curves and the leakage current amplitudes for the devices on different chips, and in some cases on the same chip, are different. Since the shape of the curve depends on device parameters such as the buried layer dopant density and lifetime profile and the surface state density, the variations between curves indicate variations in material properties, or process parameters, or both.

From the leakage current measurements, values of the bulk generation lifetime and the surface recombination velocity were obtained. (See Appendix B in ref. [2] for an explanation of the analysis of buried channel gated diodes.) The lifetime and surface recombination velocity results are given in table 1. The results show that the value of the lifetime and of the surface recombination velocity changes significantly from device to device. This may imply that significant variations in processing occurred for different chips and that substantial nonuniformity exists between different portions of the same chip.

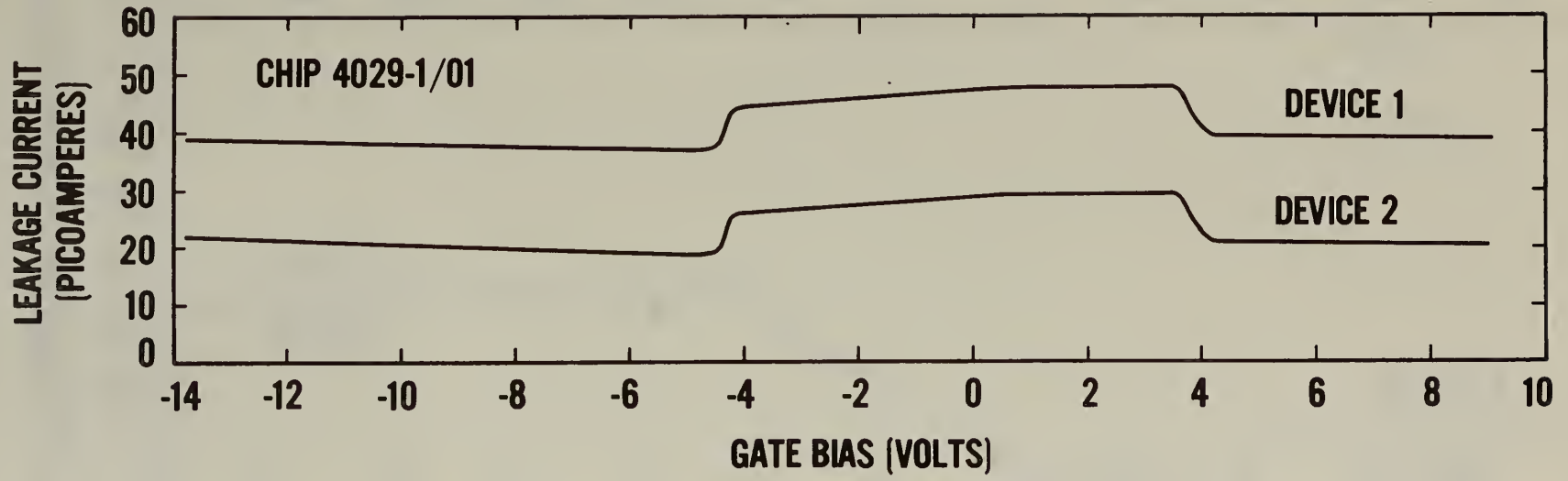

Figure 1. Leakage current as a function of gate bias voltage for devices 1 and 2 on chip 4029-1/01. The data were measured at a reverse-bias voltage V_R equal to 6 V.

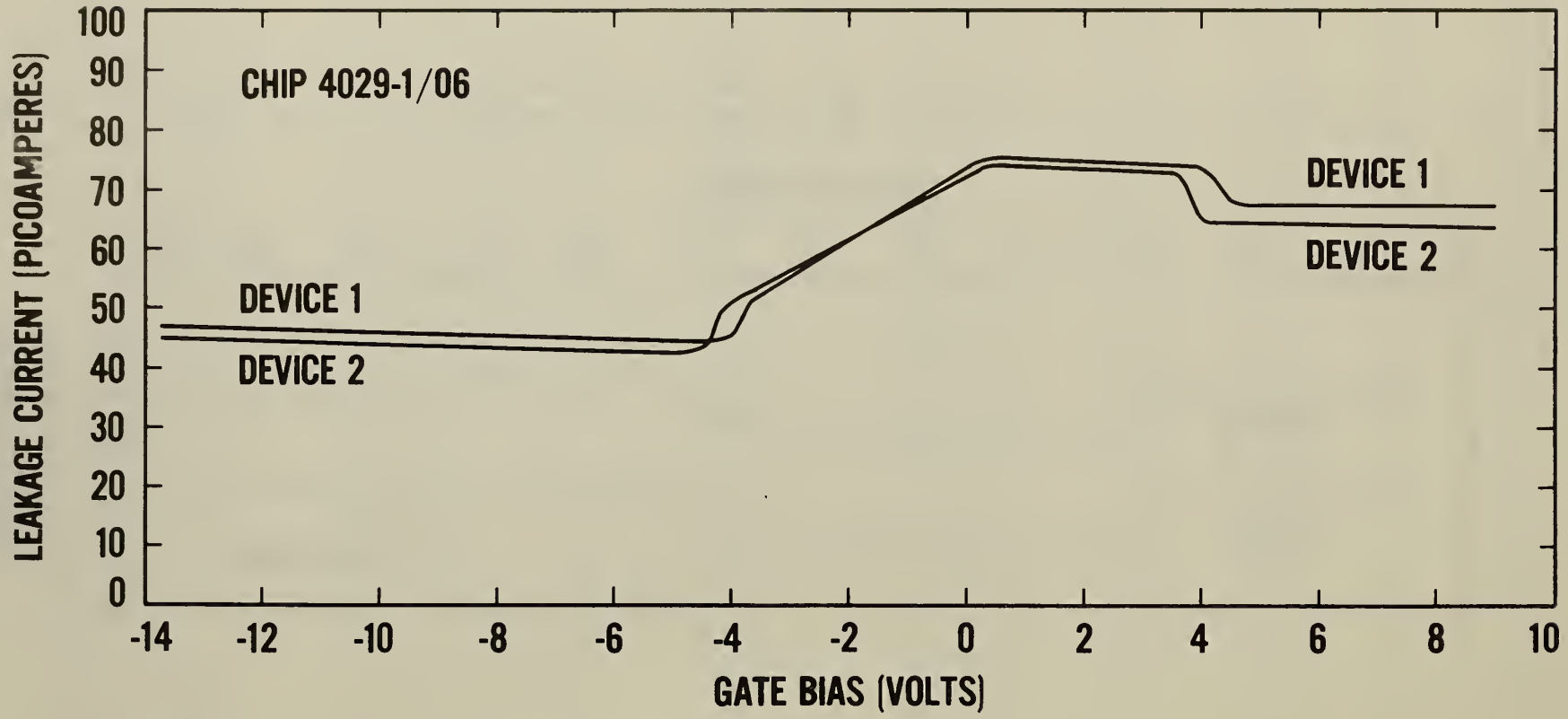

Figure 2. Leakage current as a function of gate bias voltage for devices 1 and 2 on chip 4029-1/06. The reverse-bias voltage V_R was 5 V.

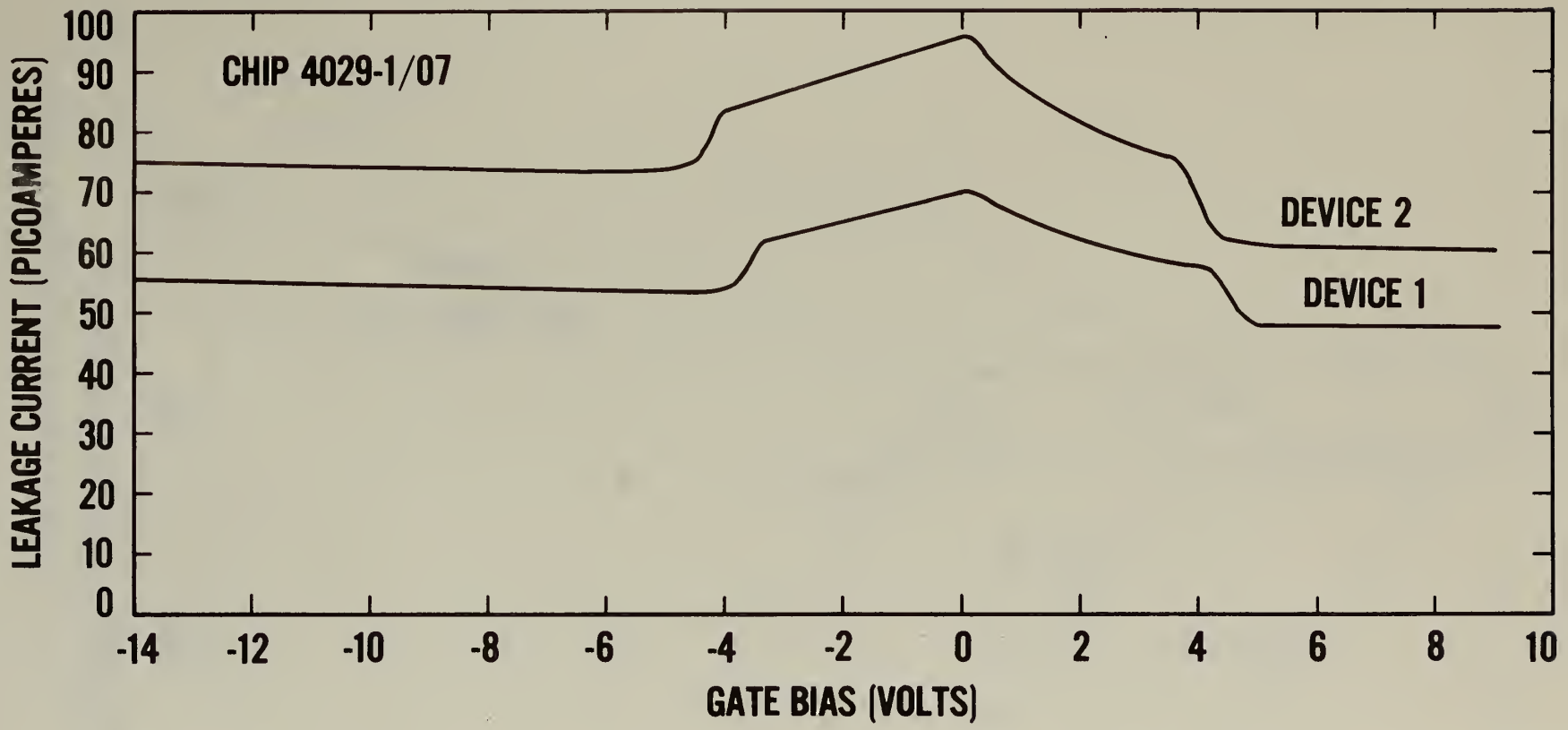

Figure 3. Leakage current as a function of gate bias voltage for devices 1 and 2 on chip 4029-1/07. The reverse-bias voltage V_R was 6 V.

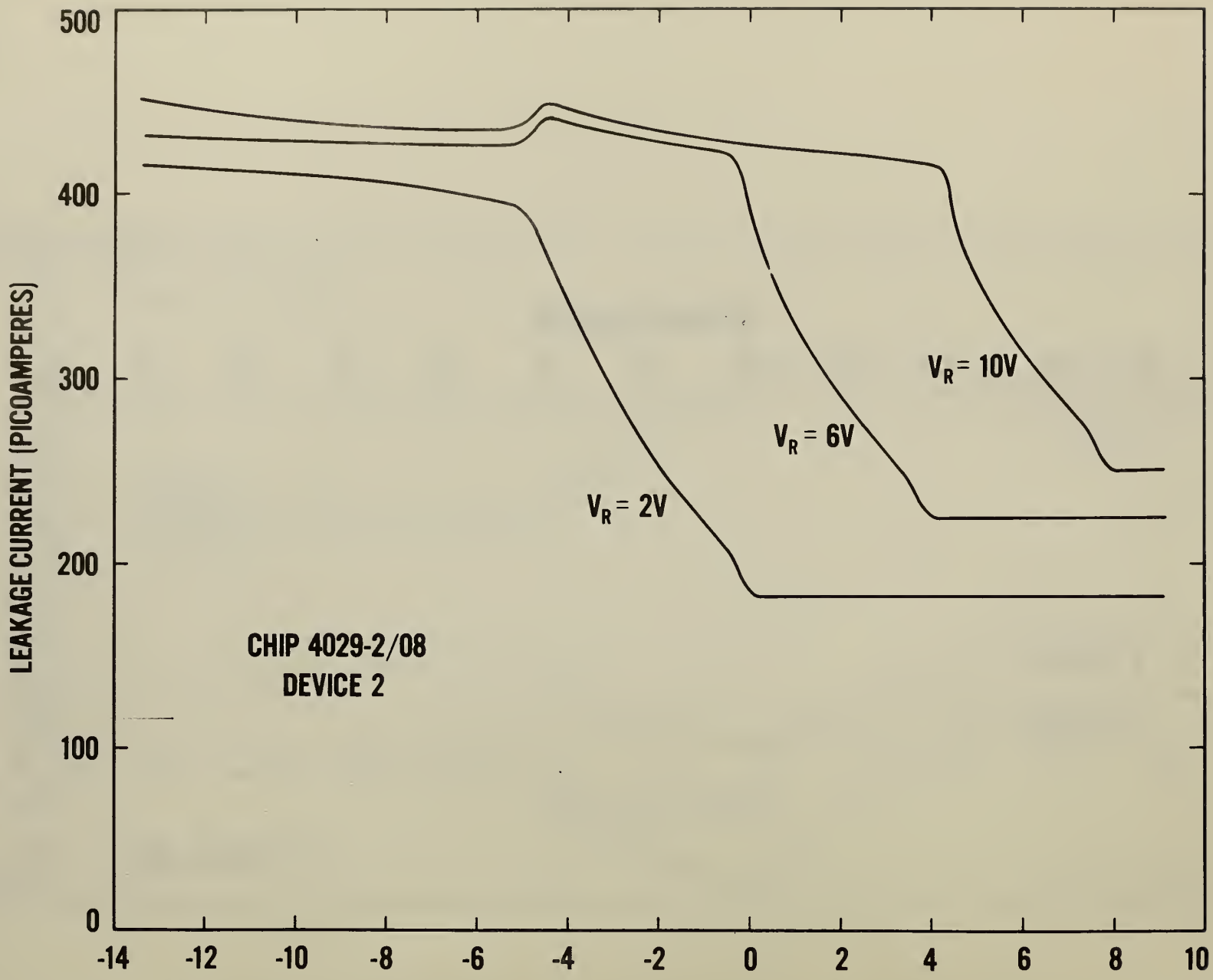

Figure 4. Leakage current as a function of gate bias voltage for device 2 on chip 4029-2/08 measured at three values of reverse-bias voltage V_R.

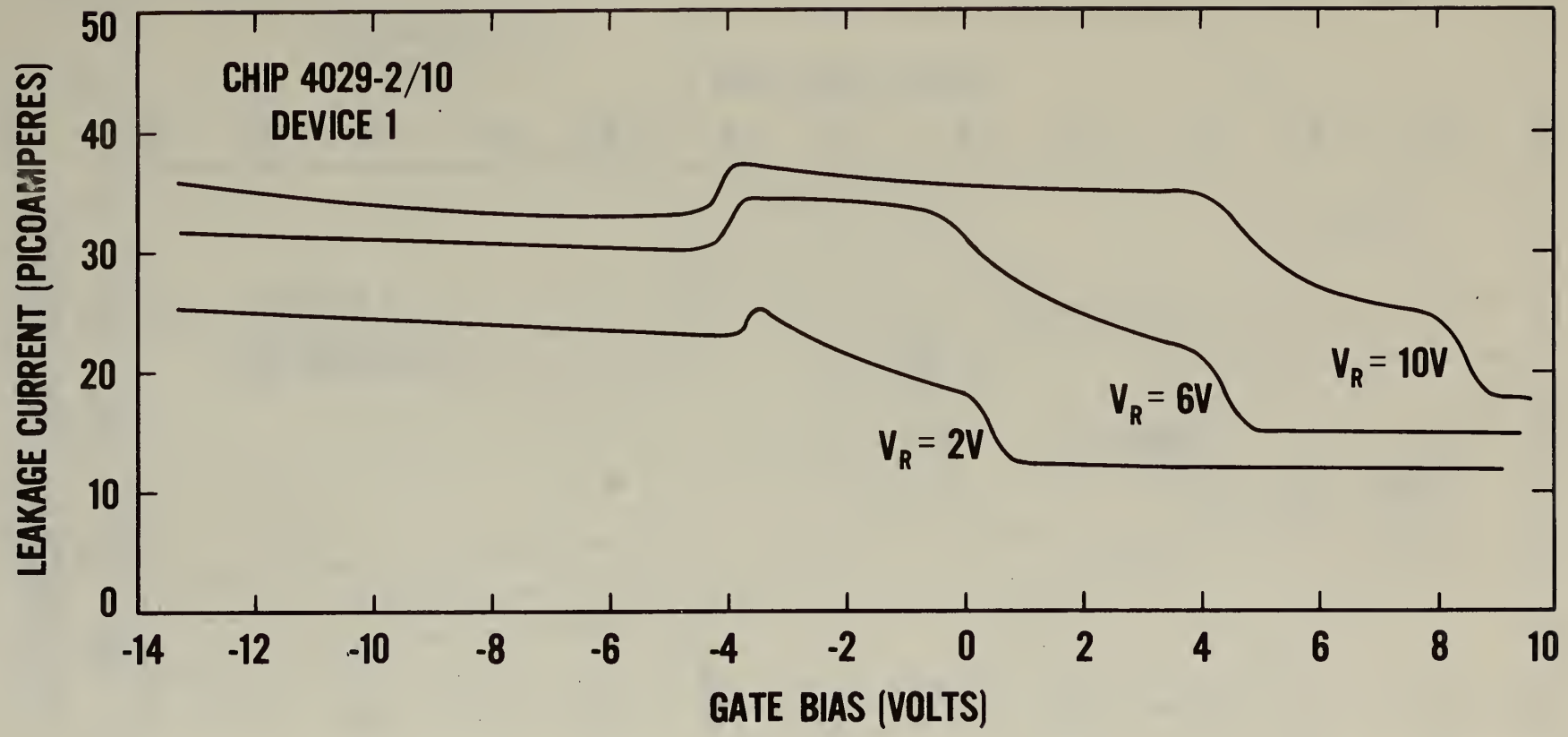

Figure 5. Leakage current as a function of gate bias voltage for device 1 on chip 4029-2/10 measured at three values of reverse-bias voltage V_R.

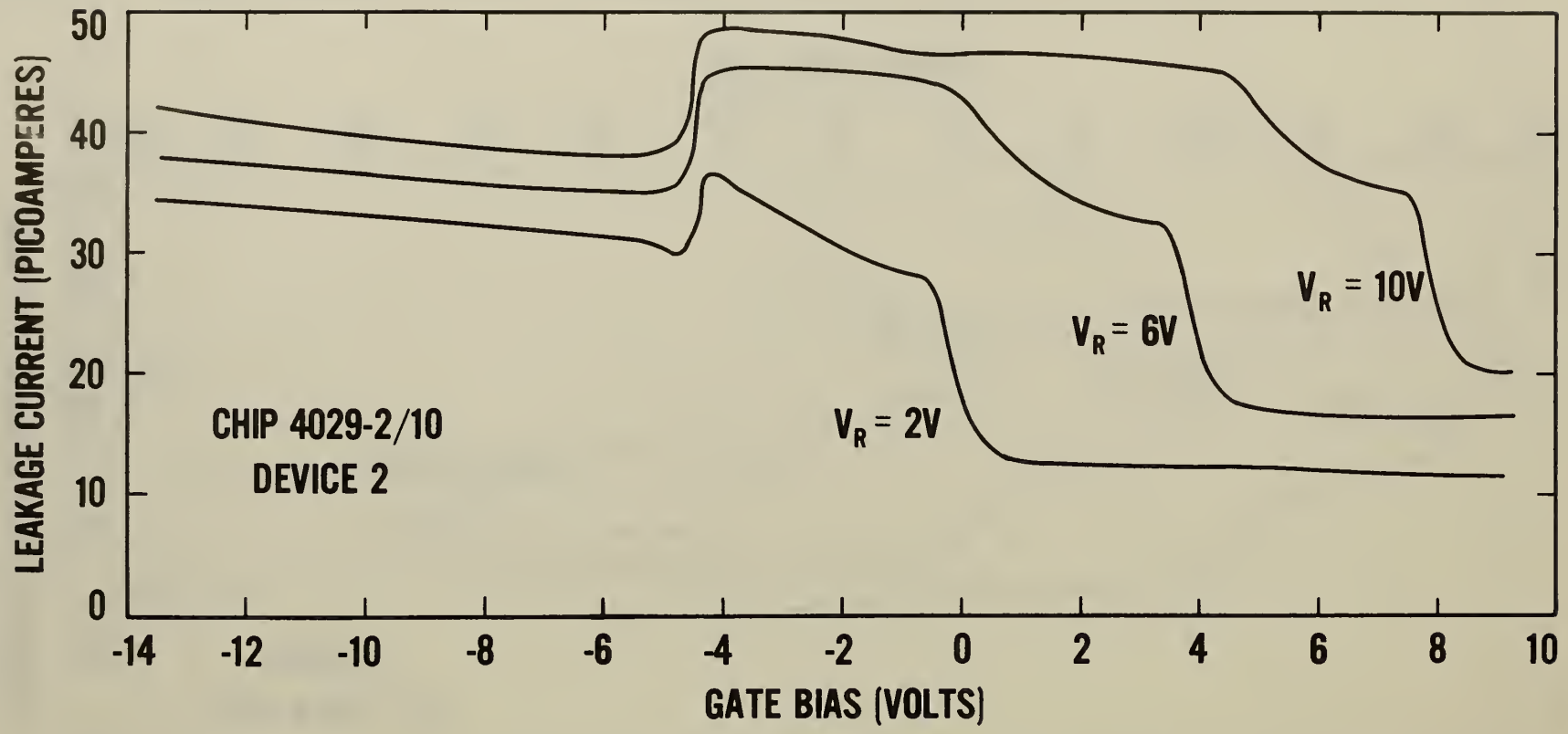

Figure 6. Leakage current as a function of gate bias voltage for device 2 on chip 4029-2/10 measured at three values of reverse-bias voltage V_R.

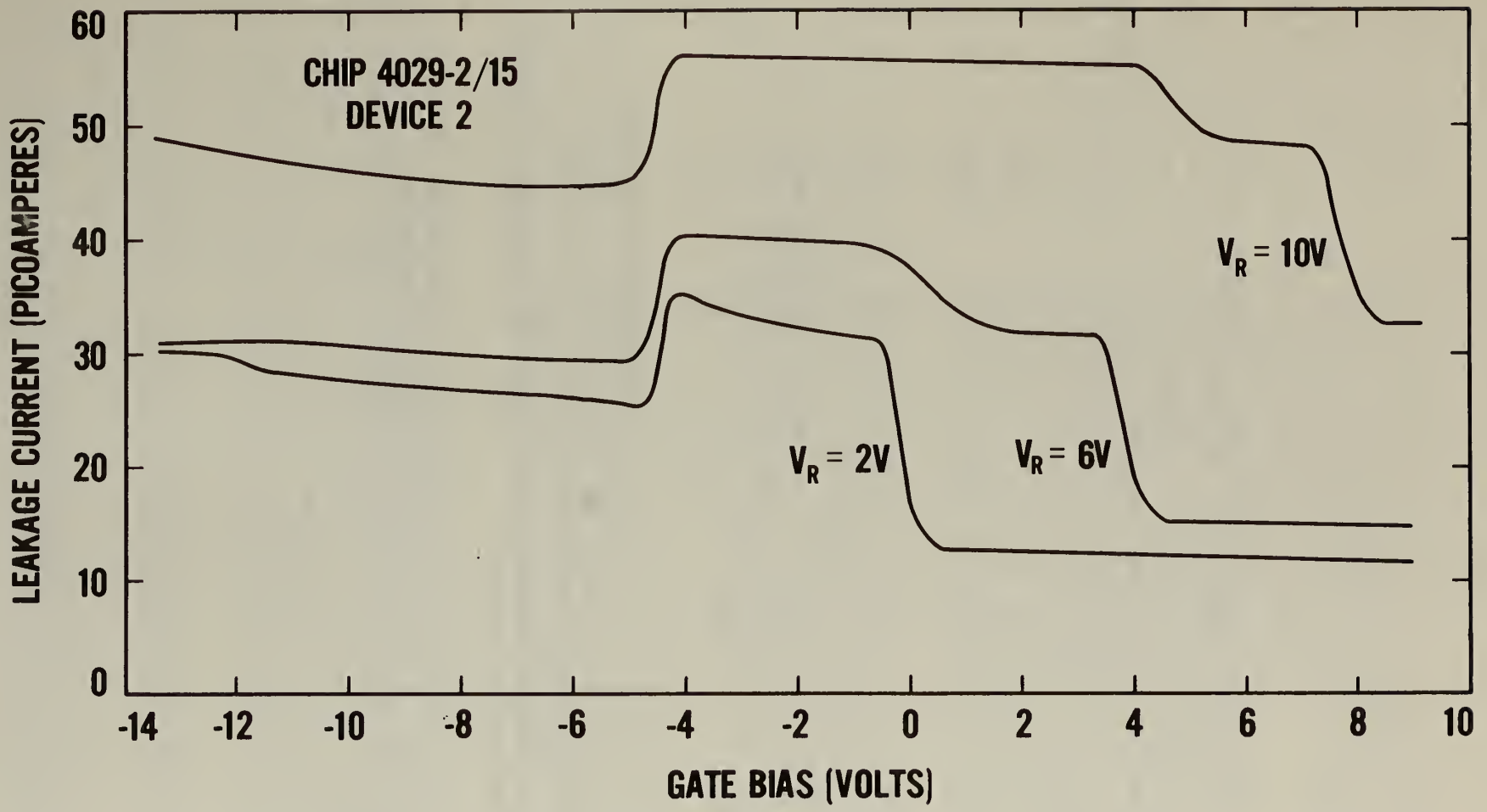

Figure 7. Leakage current as a function of gate bias voltage for device 2 on chip 4029-2/15 measured at three values of reverse-bias voltage V_R.

Table 1 - Bulk Generation Lifetime τ_{bulk} and Surface Recombination Velocity s_o Results for Six CCD Chips.

Chip Designation	Device No.	I_g(pA)[1]	I_s(pA)[2]	τ_{bulk}(μs)	s_o(cm/s)
4029-1/01	1	39	9	23	4.7
	2	21	8	43	4.2
4029-1/06	1	67	6	13	3.1
	2	64	8	14	4.2
4029-1/07	1	48	10	19	5.2
	2	61	15	15	7.9
4029-2/08	1	Gate-to-junction short			
	2	225	20	4.0	10
4029-2/10	1	15	6	60	3.1
	2	17	15	53	7.9
4029-2/15	1	No response to gate bias			
	2	15	17	60	8.9

1. I_g is the leakage current measured when the gate bias is adjusted to accumulate the surface.

2. I_s is the leakage current component due to the effect of the surface states. It can be determined from the increase in total leakage current when the surface condition changes from accumulation to depletion.

4.2 Buried Layer Profiling

The MOSFET dc profiler [3,4] was used to profile a buried layer implant used for radiation-hardened CCD imagers. The profiler is a rectangular MOSFET with a channel length of 28 μm. This work is aimed at characterizing a variety of buried layer implants under simulated CCD processing steps.* This information may lead to an improved implant schedule which will yield greater CCD radiation tolerance without sacrificing full well capacity.

The profilers were fabricated on an n-type <111> silicon wafer with a nominal room temperature resistivity of 10 Ω·cm. The fabrication process was interrupted after the channel stop and source/drain diffusion steps were completed. Then an approximately 0.01-μm thick oxide was grown in the gate oxide regions to cause randomization of the ion beam during implantation. The remainder of the wafer was masked with approximately 0.8 μm of aluminum. The wafer was then sent to a CCD vendor for implantation of the buried layer. After the wafer was returned, the aluminum was removed and an implant activation anneal was performed. The anneal was at 1100°C for 5 min in an oxygen atmosphere and 55 min in a nitrogen atmosphere. The gate oxide was stripped and the normal process sequence was continued. The final gate oxide was approximately 0.1 μm thick.

The data obtained from four profilers on one wafer are shown in figure 8. Four profilers were measured to check for uniformity across the wafer. The data indicate that the peak doping density of the implant is approximately 5×10^{16} cm^{-3} at a depth of approximately 0.14 μm. The junction depth which would have resulted had the implant been made into a p-type wafer can be estimated to be the depth at which the implanted dopant density equals the value of the background dopant density. From the data, this depth would have been about 1.3 μm.

Additional wafers have been sent to a CCD vendor for implanting. The implants will be variations of the presently used implant. The results of the profiling will be used to optimize the implant specifications. These wafers also have regions which can be used to perform spreading resistance measurements. The profiles obtained using the MOSFET dc profiler will be compared to the spreading resistance profiles.

4.3 Further Development of the Integrated Gated-Diode Electrometer

A complete and exact analytically derived solution to the simultaneous differential equations which describe the behavior of the integrated gated-diode electrometer has been obtained. The solution can be used to calculate the leakage current and, from values for the leakage current, the generation lifetime and surface recombination velocity. A manuscript which outlines the analysis and operation of the integrated gated-diode electrometer has been submitted for publication (see sec. 4.4).

The derivation is based upon a linear model for the electrometer MOSFET and the use of voltage independent equivalent circuit elements for the gated diode. An

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*In order to profile the buried channel of actual CCDs, a dual gate MOSFET is required [1]. This is because the CCD buried channel is of opposite conductivity type than the substrate.

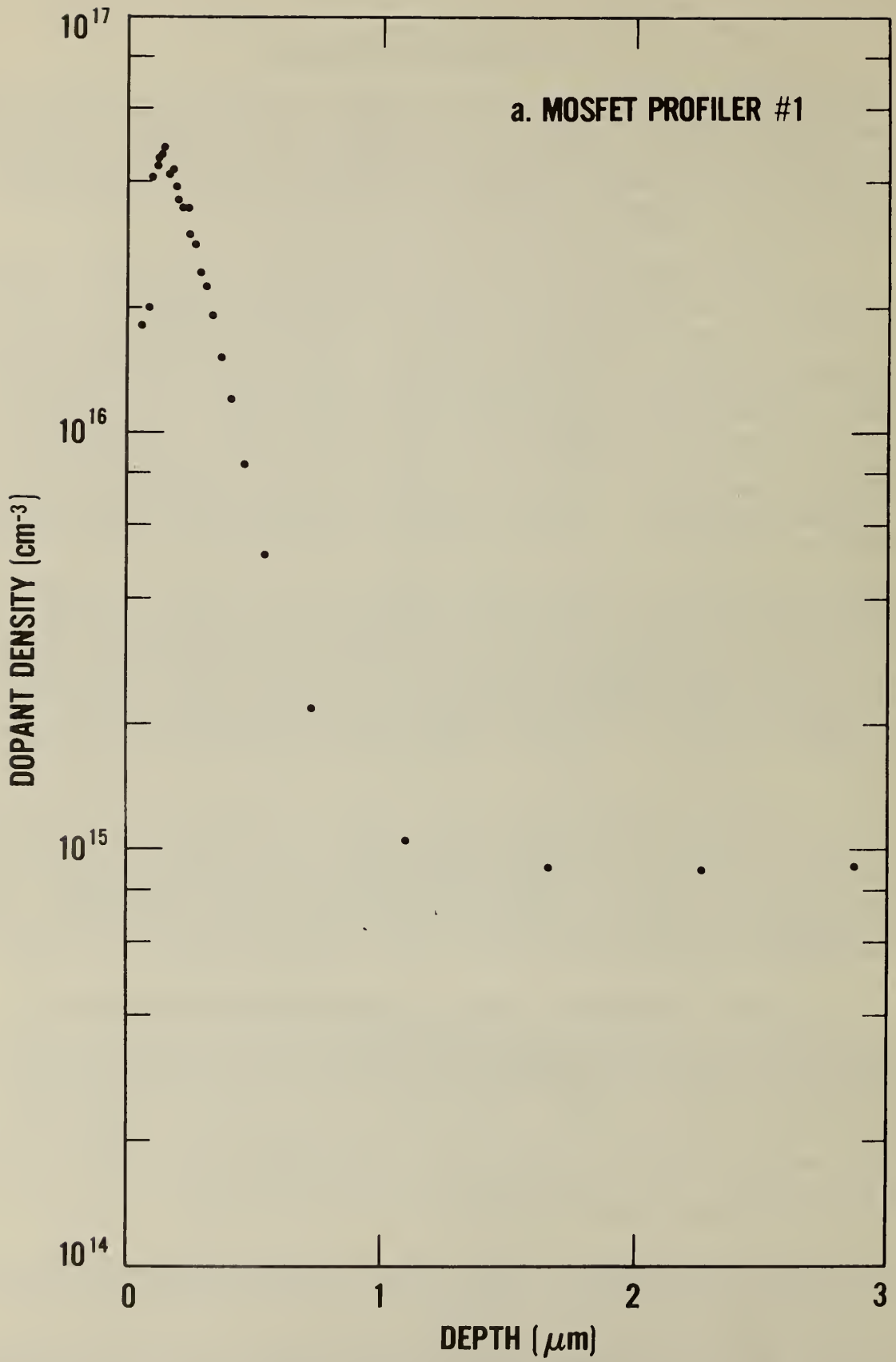
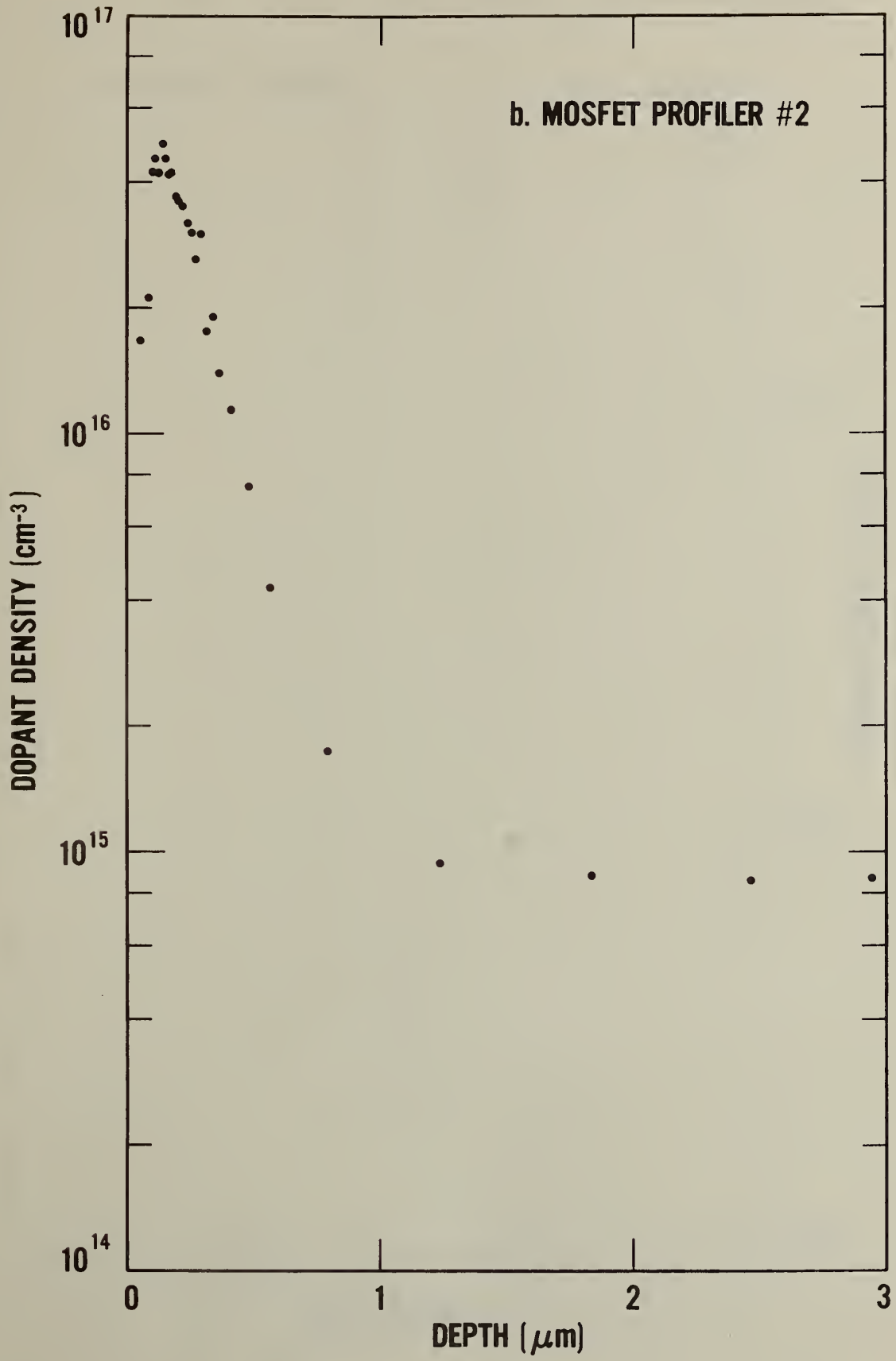
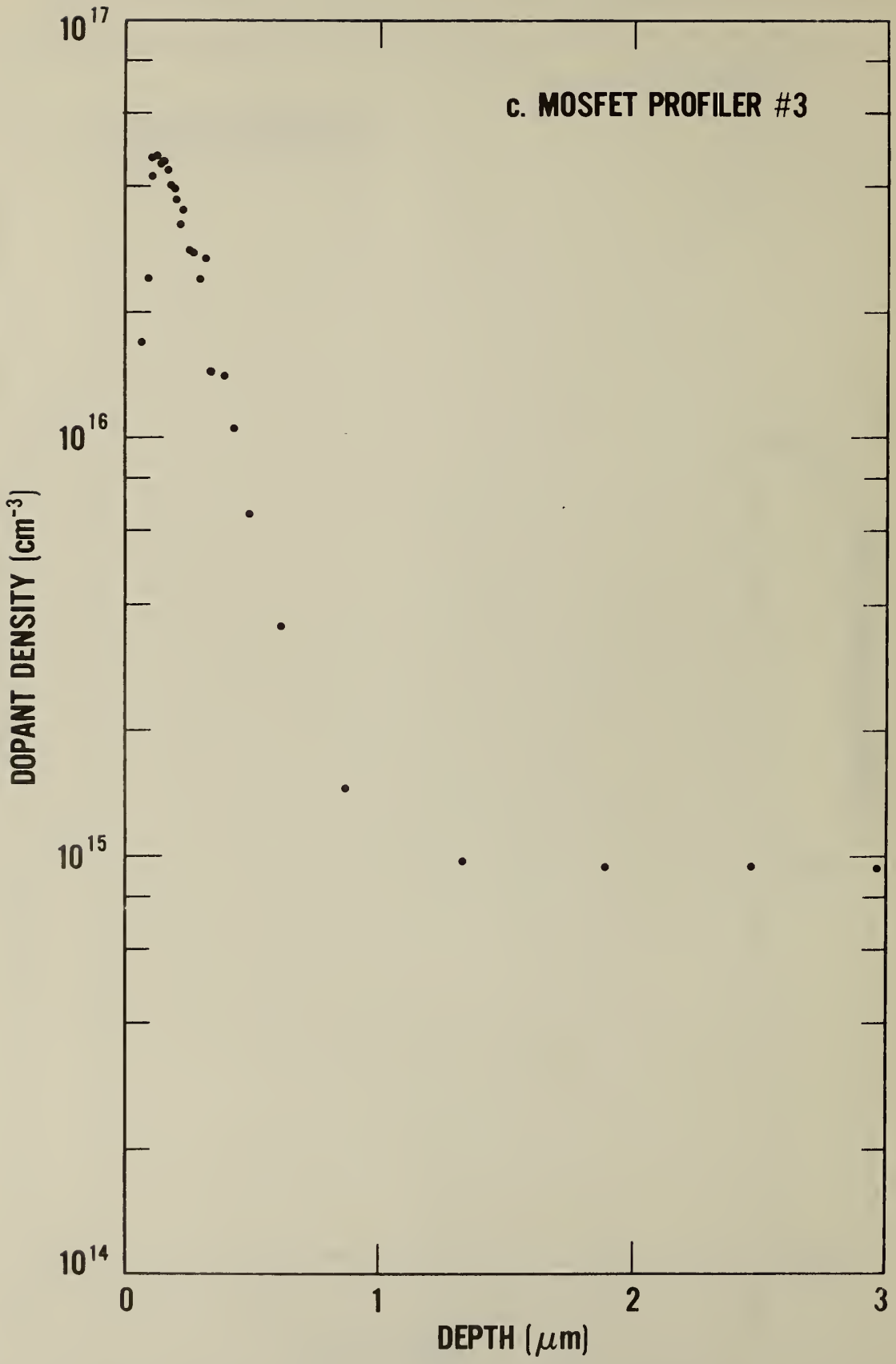
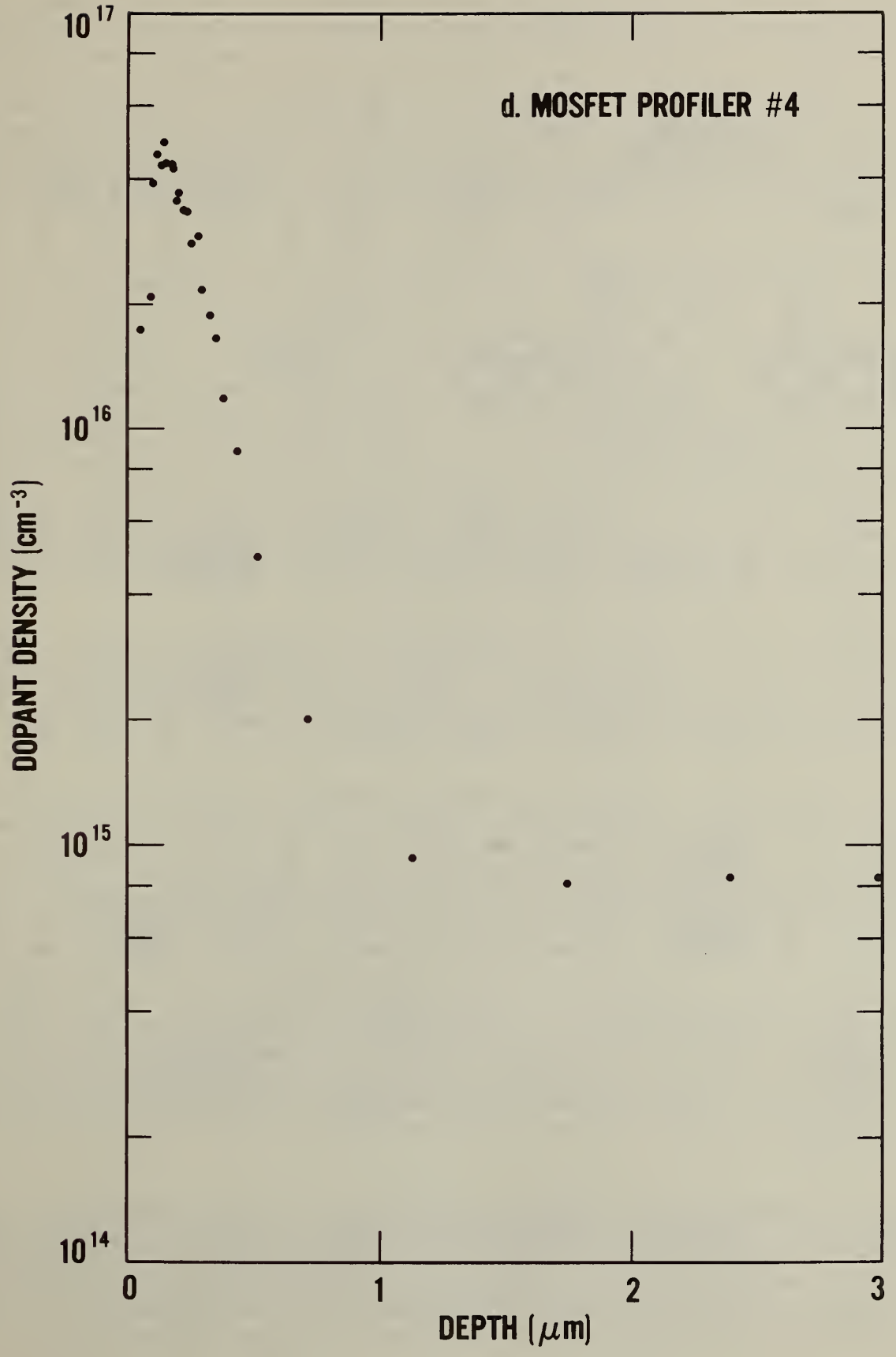


Figure 8. Dopant density *versus* depth profile obtained from measurements on the MOSFET dc profiler. Plots (a) through (d) show data from four devices on the same n-type wafer.


b. MOSFET PROFILER #2
10^{17}
10^{16}
10^{15}
10^{14}
DOPANT DENSITY (cm^{-3})
0
1
2
3
DEPTH (μm)


c. MOSFET PROFILER #3
10^{17}
10^{16}
10^{15}
10^{14}
DOPANT DENSITY (cm^{-3})
0
1
2
3
DEPTH (μm)


d. MOSFET PROFILER #4
10^{17}
10^{16}
10^{15}
10^{14}
DOPANT DENSITY (cm^{-3})
0
1
2
3
DEPTH (μm)

extension of the solution is not easily achieved when the electrometer MOSFET is represented by a more complex model to more precisely reflect saturated MOSFET behavior. However, such an extension is not necessary because the operating range of the MOSFET is very small during the measurement and the linear approximation is adequate. The use of voltage independent equivalent-current-source and equivalent-junction-capacitor for the gated diode is also not a serious limitation. The resulting restriction is that the measurements are performed over a sufficiently short time span so that the reverse-bias voltage change is small during the measurement.

Detailed measurements of the integrated gated-diode electrometer test structure have provided an explanation of the previously observed deviations [1] between the leakage currents derived from the electrometer amplifier output voltage rate-of-decay and the leakage measured directly from the diode under test. The dominant deviations can be accounted for by considering all parasitic capacitance sources. Sources of parasitic capacitance include the capacitance between the input MOSFET gate and the inversion layer and the overlap capacitance between the input MOSFET gate and its source and drain, etc. These capacitances are especially important in the gated-diode electrometer test structure because its metrology involves determining the leakage current from the decay of the voltage across the diode junction capacitor. Because the diode capacitance is a depletion capacitance and the parasitic capacitors are gate oxide capacitors, the parasitic capacitors may have relatively large values even though they may be relatively smaller in area.

A variety of new designs for the integrated gated-diode electrometer were tested during this period. The structures are on test pattern NBS-24, shown in figure 9, which was fabricated for the first time during this period. The structures on NBS-24 include those which were recommended for inclusion on the CCD chips [1].

The initial lots of wafers fabricated with NBS-24 had unusually high bulk generation rates and excessive surface generation rates under the polysilicon gates. The electrometer MOSFETs on some wafers suffered from high subthreshold current and did not completely turn off at zero input voltages. Also, the gain (β) of the source-follower was nonlinear and averaged about one-half its design value. Despite these processing deficiencies, significant results were obtained. The metrology of the integrated gated-diode electrometer involves a determination of the value of β at the operating point. It is this value which is used in the computation of the leakage currents. Other characteristics of the source-follower MOSFET are not important for evaluation of the leakage current because these factors do not alter the relationship between the output voltage rate-of-decay and the leakage current. These results verified the suitability of the new designs for the integrated test structure and demonstrated that the metrology can handle deficiencies in the material or process parameters.

The new designs, which include gated diodes that can be probed directly, have been used to compare the leakage current deduced from the electrometer output voltage with the leakage current measured with an external current meter. There is generally no larger than about a 20-percent disagreement; this value is within the expected combined uncertainties in both measurements. It is expected that these results will be published in the near future.

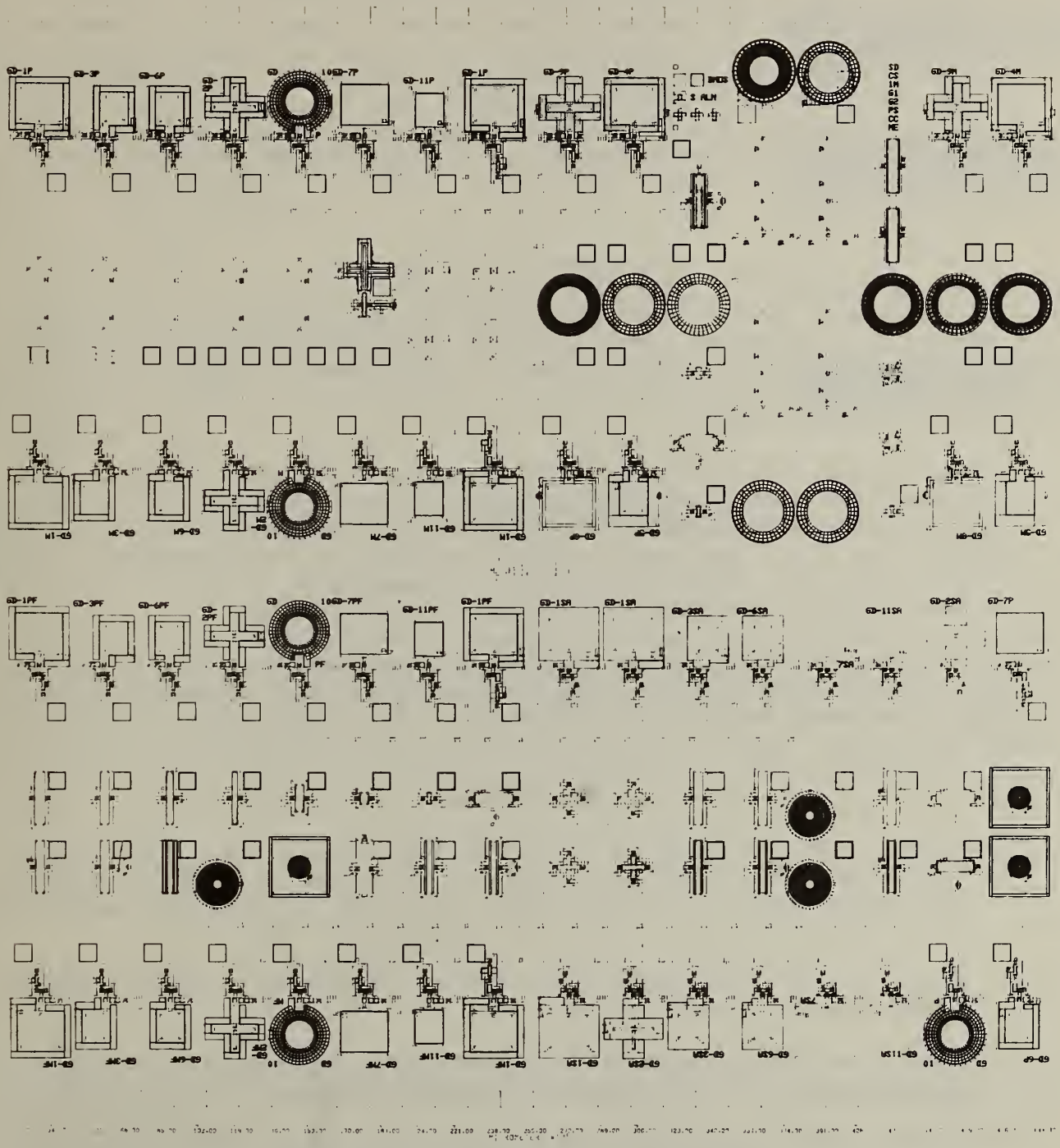


Figure 9. Computer plot of test pattern NBS-24 which is 200 mil (5.1 mm) by 200 mil (5.1 mm) in size. The integrated gated-diode electrometers are in the top rows, the center rows, and the bottom rows.

The junction capacitance was further studied and characterized on these new wafers. The junction capacitance is a component of the total parallel capacitance which must be known to evaluate the leakage current. The capacitance of the junction can be calculated using a model such as the abrupt junction approximation [1]. It was determined that for the devices on NBS-24, the abrupt junction approximation predicts too low a value for the junction capacitance, implying a significant peripheral capacitance component. The probeable designs for the integrated gated-diode electrometer allow actual measurement of the junction capacitance as a function of reverse-bias voltage. The measured values are uniform across each wafer so that a single capacitance measurement can provide a value of the capacitance for all devices of a given geometry on a wafer.

4.4 Talks and Publications

A paper entitled "Design Considerations for the Integrated Gated-Diode Electrometer" by G. P. Carver and M. G. Buehler was presented at the Spring Meeting of the Electrochemical Society in Boston, Masssachusetts on May 10, 1979. The paper, Abstract No. 193, is reproduced in *Electrochemical Society, Extended Abstracts* (October 1978).

A paper entitled "The Use of Microelectronic Test Structures to Characterize IC Materials, Processes, and Processing Equipment" by G. P. Carver, L. W. Linholm, and T. J. Russell was presented at SEMICON/East '79 (Boston, Masschusetts) on September 19, 1979. This paper was also presented at the Measurement Sciences Conference (San Luis Obispo, California) on November 30, 1979. The manuscript has been accepted for publication in *Solid State Technology*.

A paper entitled "An Analytical Expression for the Evaluation of Leakage Currents in the Integrated Gated-Diode Electrometer" by G. P. Carver and M. G. Buehler has been submitted for publication in *IEEE Transactions on Electron Devices*.

5. References

1. Carver, G. P., and Buehler, M. G., The Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers, NBSIR 79-1744 (May 1979). [Available from the National Technical Information Service (NTIS), Springfield, VA 22161]

2. Hartsell, G. A., New Memory Device Structures, Technical Report AFAL-TR-76-39, Vol. III (December 1977).

3. Buehler, M. G., Dopant Profiles Determined from Enhancement-Mode MOSFET dc Measurements, *Appl. Phys. Letters* 31, 848-850 (1977).

4. Buehler, M. G., Limitations and Applications of the dc MOSFET Dopant Profile Method, *J. Electrochem. Soc.* (to be published).

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15. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This project is to evaluate new test structures and test methods useful for the characterization of radiation-hardened CCD imagers. During the period covered by this report, consultation was provided to The Charles Stark Draper Laboratory, Inc. (CSDL) and to CSDL contractors on the implementation of test structures developed during the previous year of this project. In addition, the results of measurements on buried channel gated diodes and buried layer metal-oxide-semiconductor field-effect transistor (MOSFET) direct-current (dc) profilers are reported. Further advances in the development of the integrated gated-diode electrometer are also reported.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*
CCD; electrical test structure; gated diode; integrated gated-diode electrometer; integrated test structure; leakage current; test structure.

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