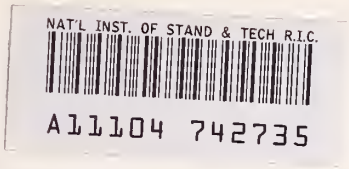

NBSIR 79-1744

The Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers

G. P. Carver and M. G. Buehler

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, DC 20234

May 1979

Prepared for
The Charles Stark Draper Laboratory, Inc.
Cambridge, MA 02139

NBSIR 79-1744

THE DEVELOPMENT OF TEST STRUCTURES FOR CHARACTERIZATION OF THE FABRICATION AND PERFORMANCE OF RADIATION-HARDENED CCD IMAGERS

G. P. Carver and M. G Buehler

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, DC 20234

May 1979

Prepared for
The Charles Stark Draper Laboratory, Inc.
Cambridge, MA 02139

U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, *Secretary*
Jordan J. Baruch, *Assistant Secretary for Science and Technology*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

Table of Contents

List of Figures

The Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers

G. P. Carver and M. G. Buehler

Electron Devices Division
Center for Electronics and Electrical Engineering
National Bureau of Standards
Washington, D.C. 20234

1. Introduction

The objective of this project is to develop new test structures and new test methods which will be useful for the characterization of radiation-hardened CCD imagers and the processes by which they are made. The test structures and test methods will enable manufacturers of radiation-hardened CCDs to measure critical process and device parameters and will provide end users with information based upon measurements which accurately and reliably reflect critical CCD performance. In addition, the test structures and test methods are designed to minimize the hardware and software required to fully implement a suitable test program at the CCD manufacturing facilities.

In response to the above goals, existing test structures were improved and modified for the radiation-hardened processes, and two new production-compatible advanced test structures were developed. The new test structures are the Integrated Gated-Diode Electrometer and the MOSFET dc Profiler.

The Integrated Gated-Diode Electrometer provides a measure of the bulk generation lifetime and the surface recombination velocity. In addition, it can be used to detect sources of leakage current which contribute to the dark current in CCDs. The metrology of this new test structure involves the convenient measurement of voltage changes due to leakage currents which are extremely small and difficult to measure directly.

The MOSFET dc Profiler furnishes dopant density versus depth information. Unlike conventional profiling techniques, the MOSFET Profiler involves dc signals and can be measured with high-speed automated equipment compatible with production test instruments.

This report outlines the conceptual and experimental background of the new advanced test structures, describes the associated theory and analysis, and details the test methods. It also includes a collection of test structure designs and specifications for production-compatible test structures.

2. Integrated Gated-Diode Electrometer

2.1 Leakage Currents

Leakage currents in microelectronic devices arise from mobile charge carriers which are generated in the vicinity of device active regions. Common generation mechanisms include thermal generation of minority carriers by trap centers located in the bulk of the semiconductor, within depletion regions or within a diffusion length of depletion regions; thermal generation by trap centers at the semiconductor-insulator interface, within depletion regions or within a diffusion length of depletion regions; and electric-field-induced generation such as Zener tunneling and impact ionization. In addition, radiation-induced defects which behave as generation centers can lead to excessive current leakage. Large array CCD imagers are particularly sensitive to leakage currents which increase the dark current and may affect the full well capacity and the noise amplitude.

Gate-controlled diode structures, called gated diodes, are often employed to investigate leakage currents. In contrast to capacitance-voltage measurements on MOS or junction capacitors, which can supply data on numerical trap density, gated diode measurements provide information on the rate of carrier generation. Different mechanisms of carrier generation may be emphasized by differences in the geometry of gated diode structures. If a value for the capture cross section is assumed, data from gated diodes may also be used to estimate the numerical trap density.

Gated diode measurements typically require the use of a diode which is large in comparison with the size of integrated circuit elements. This may restrict the value of such measurements for the design engineer. A more serious drawback, however, is the experimental situation. Measurement procedures associated with gated diodes as test structures involve low current levels (typically picoamperes), extremely high output impedances associated with the reverse-biased junction (typically $\sim 10^{12}\ \Omega$), and data rates slow enough to avoid effects of displacement currents (so that a measurement usually requires ten minutes or more). This experimental situation restricts the use of gated diodes as viable test structures to a laboratory environment.

Use of the Integrated Gated-Diode Electrometer overcomes the restrictions associated with conventional, stand-alone gated diode measurements. The advantages of this advanced test structure include the practicability of reducing diode dimensions to sizes typical of integrated circuit elements and the compatibility with high-speed data acquisition techniques.

2.2 Gated Diode Measurements

Stand-alone gated diode studies were undertaken during this program to support the development of the Integrated Gated-Diode Electrometer and to aid in the interpretation of data obtained from an initial advanced

test structure design, structure 127 on test pattern NBS-12. The results from structure 127 are described in the next section.

The reverse-bias leakage current versus gate voltage characteristics of a gated diode are well known and will be reviewed only briefly here. This current, measured between the diode junction and ground, usually exhibits three distinct regimes depending upon the magnitude of the voltage applied to the diode gate [1]. When the gate voltage is adjusted so that the surface of the semiconductor under the gate is accumulated, the diode leakage current, under ideal conditions, is the current generated by bulk generation centers in or near the depletion region under the metallurgical junction. For an abrupt one-sided junction, this generation current I_g may be written

$$I_g = q\, g\, A(W - W_f) \tag{1}$$

where q is the electronic charge, g is the generation rate per unit volume in the semiconductor, A is the area of the metallurgical junction, W is the width of the depletion region when a given reverse-bias voltage is applied, and W_f is the width of the depletion region when zero external bias voltage is applied.

When the gate voltage is adjusted so that the semiconductor under the gate is depleted, the total leakage current increases. The larger leakage current includes two additional currents: the surface current generated by interface states at the semiconductor-insulator interface under the gate and the generation current from the depleted volume under the gate. The surface current, I_s, is given by

$$I_s = q\, g_s\, A_g\ , \tag{2}$$

where g_s is the area generation rate at the surface beneath the gate and A_g is the gate area. The generation current from the depletion volume under the gate, I_{gg}, is

$$I_{gg} = q\, g_g\, A_g\, W\ , \tag{3}$$

where g_g is the volume generation rate beneath the gate.

In the third operating regime of the gated diode, the gate is biased to invert the semiconductor beneath the gate. The leakage current in the inversion regime is composed of the two bulk generation currents (from under the junction and under the gate). The surface state contribution is blocked by the presence of the inversion layer.

In summary, the gate accumulation, depletion, and inversion regimes result, respectively, in leakage currents due to generation in the bulk under the junction (accumulation), in the bulk under the junction and at the surface and in the bulk under the gate (depletion), and in the bulk under both the junction and the gate (inversion) as shown in figure 1.

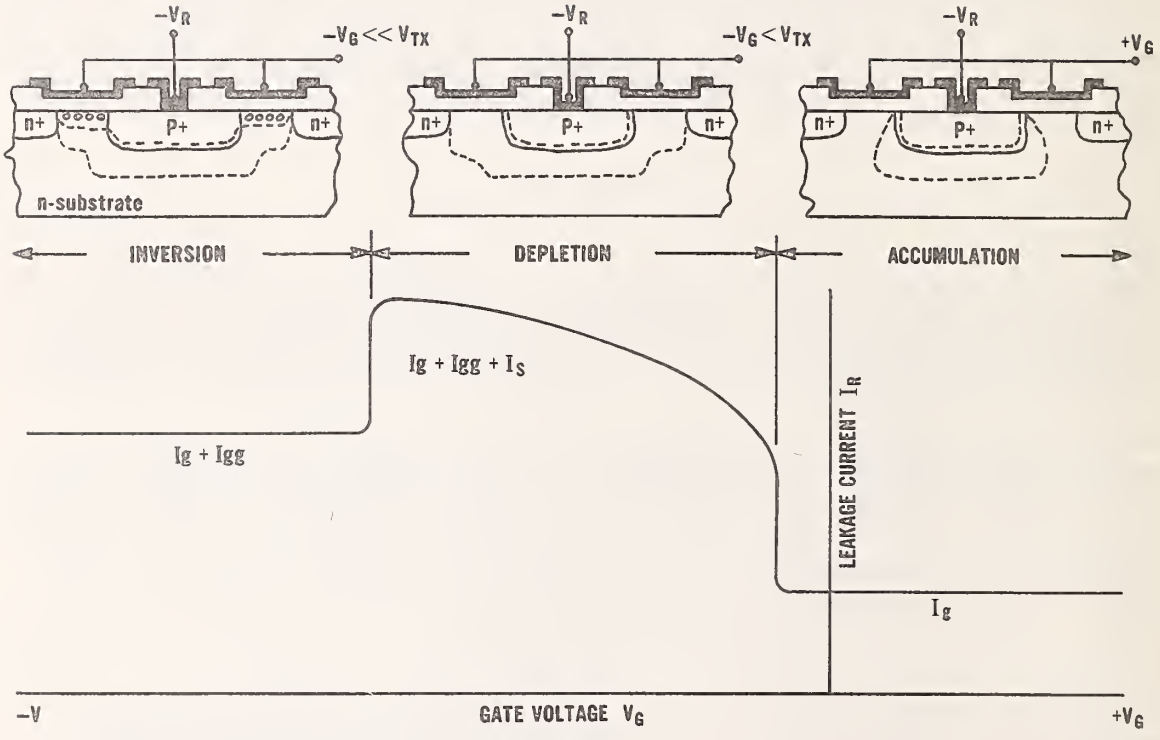

Figure 1. Idealized curve of reverse-bias leakage current I_L for a gated diode as a function of gate voltage V_G showing the regimes where the condition of the material under the gate is accumulated, depleted, or inverted. The symbols are identified in the text. The insets at the top schematically illustrate the spatial extent of the depletion region for the case of a p^+n junction.

The generation rates are usually expressed in relation to the intrinsic carrier concentration in the semiconductor, n_i:

$$g = \frac{1}{2\tau} n_i \ , \tag{4a}$$

$$g_s = \frac{S_o}{2} n_i \ , \tag{4b}$$

and

$$g_g = \frac{1}{2\tau_g} n_i \ . \tag{4c}$$

The proportionality constants in these relations define the lifetime τ in the depletion region beneath the junction, the surface recombination velocity S_o, and the lifetime τ_g in the depletion region induced by the voltage applied to the gate.

Gated diodes are affected by all leakage current sources, and therefore in addition to the "classical" behavior due to generation currents as described above, the total gated diode leakage current also reflects current from the field-induced generation mechanisms alluded to earlier. This additional current was observed during our study on stand-alone gated diodes.

Measurements were carried out on several types of gated diodes with a range of gate oxide types and thicknesses. The gated diodes were the cross-shaped diode on test pattern NBS-12 and one large and one small diameter circular diode on test pattern NBS-4 [2]. Also, two rectangular MOSFETs, operated as gated diodes by connecting the source and drain and measuring the leakage to ground as the gate voltage is varied, were included in the study. Specifications of the devices are given in table 1. All of the structures measured were fabricated on *n*-type wafers which were processed together.

The results obtained show the classical behavior, but in addition show deviations which are sometimes large enough to overwhelm and prevent determination of the generation currents. An example is shown in figure 2.

The deviations, or excess currents, have the characteristic that the leakage current increases rapidly with gate voltage. That is, when the gate is biased into strong accumulation or strong inversion, the leakage current is increased greatly. The results are qualitatively in accord with an explanation based on soft breakdown at the periphery of the diode gate. Soft breakdown is meant to imply the lowering of the junction breakdown voltage, as evidenced by greatly increased leakage current. In this case, soft breakdown occurs when the gate voltage is large. The mechanisms by which soft breakdown occurs involve the increased current leakage at the field-induced junction near the heavily doped diode diffusion (in accumulation) or near the channel-stop diffusion (in inversion),

Table 1

Specifications of Structures Used as Stand-Alone Gated Diodes

Structure Designation	Structure Description	Junction Area $(mm)^2$	Junction Perimeter (mm)	Gate Area $(mm)^2$
4.16	Rectangular MOSFET	0.00645	0.127	0.00113
12.115	Rectangular MOSFET	0.00472	0.448	0.00627
4.14	Small Round Gated Diode	0.0182	0.479	0.0182
12.127	Cross-shaped Gated Diode	0.0137	0.792	0.00802
4.10	Large Round Gated Diode	0.146	1.36	0.146

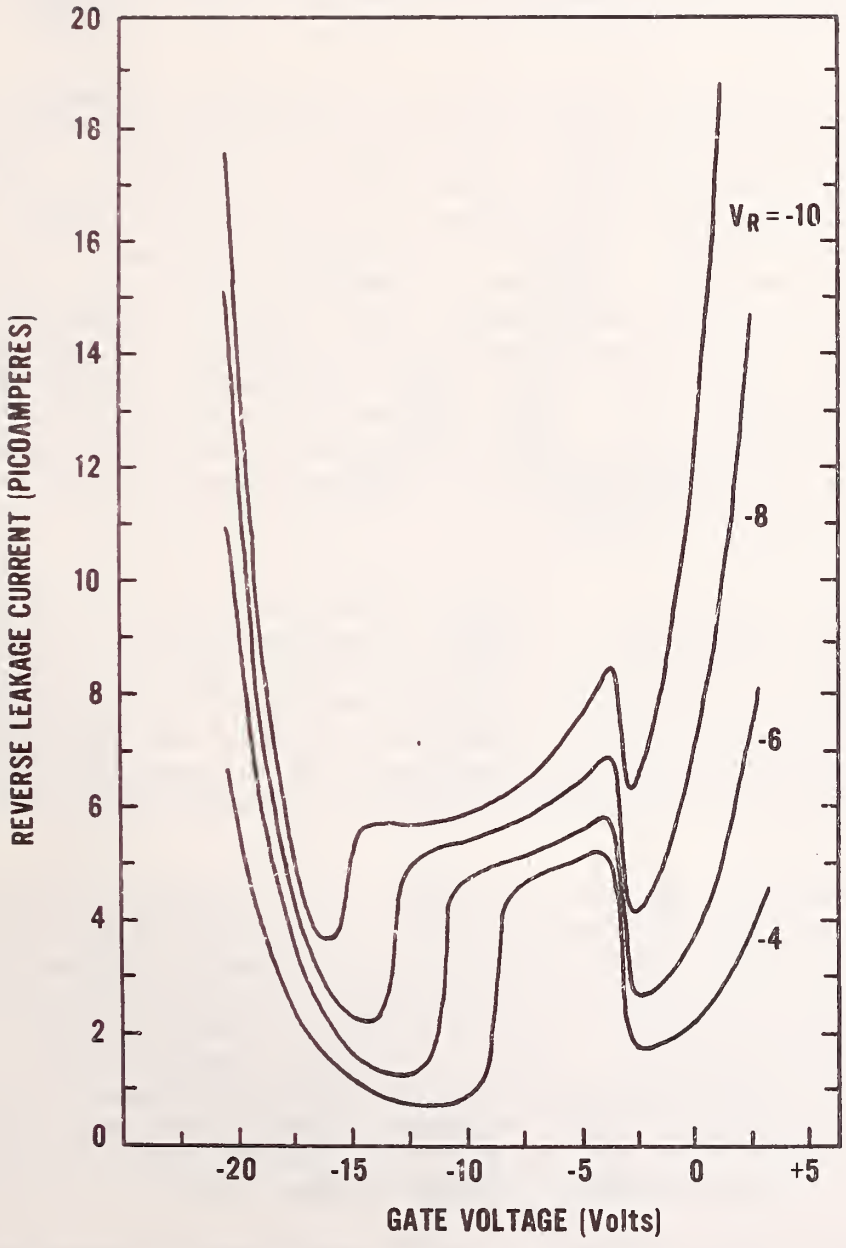

Figure 2. An example of the actual leakage current *vs.* gate voltage obtained from a cross-shaped gated diode. The excess leakage currents discussed in the text are seen to increase rapidly as the gate is biased into strong accumulation or inversion.

and at the inner and outer peripheries of the gate, respectively. In either case, there is a tendency for the gate field-induced junction to penetrate into a region of high doping density, forming a p^+n^+ diode, and to increase the probability of carrier creation by Zener emission, impact ionization (avalanching), or both.

We have verified that the magnitude of the excess leakage currents in accumulation is proportional to the electric field intensity between the diode junction and the gate. The data for one device are shown in figure 3. We have also demonstrated that the excess current in accumulation is directly proportional to the length of the diode junction-to-gate boundary. This is shown in figure 4. Similar results were obtained when the gate was biased into inversion. The MOSFET structures operated as gated diodes do not show excess leakage in the inversion regime because the gate is an interior element and does not adjoin the channel-stop diffusion. The factors which cause large field-induced currents include structure geometry (e.g., large perimeter-to-area ratio, large gate-to-junction overlap, large gate-to-channel-stop overlap, and the presence of corners on the gate) and high reverse-bias voltages. If the generation currents are relatively small for a given device, the effect of field-induced currents is greater.

Although the magnitude of each of the various leakage current contributions varies from device to device, there were many devices where the field-induced currents were relatively small, and the bulk generation currents and the surface current components could be determined accurately. For these devices, the generation currents were found to be directly proportional to the junction and gate areas as expected. Average measured values of the lifetimes and surface recombination velocities are given in table 2.

These results are extremely important to the radiation-hardened CCD program because they indicate that new and very relevant information can be obtained with gated diodes and because they suggest new and unique design possibilities to acquire this information. Certainly, the field-induced excess boundary-perimeter leakage currents are exhibited by all gate-controlled MOS devices. In most cases, such leakage is not a severe problem. The gated diode structures we tested necessarily emphasize leakage currents, including perimeter leakage. However, this situation is also likely to occur in CCDs and CCD readout registers where gate perimeter lengths are large relative to gate areas.

Thus, gated diode measurements take on additional relevance and usefulness. Gated diodes of proper design, large perimeter-to-area ratios for example, magnify field-induced leakage of the type which can be troublesome in CCDs. Furthermore, this particular source of unwanted dark current in CCDs may be intensified by exposure to radiation [3].

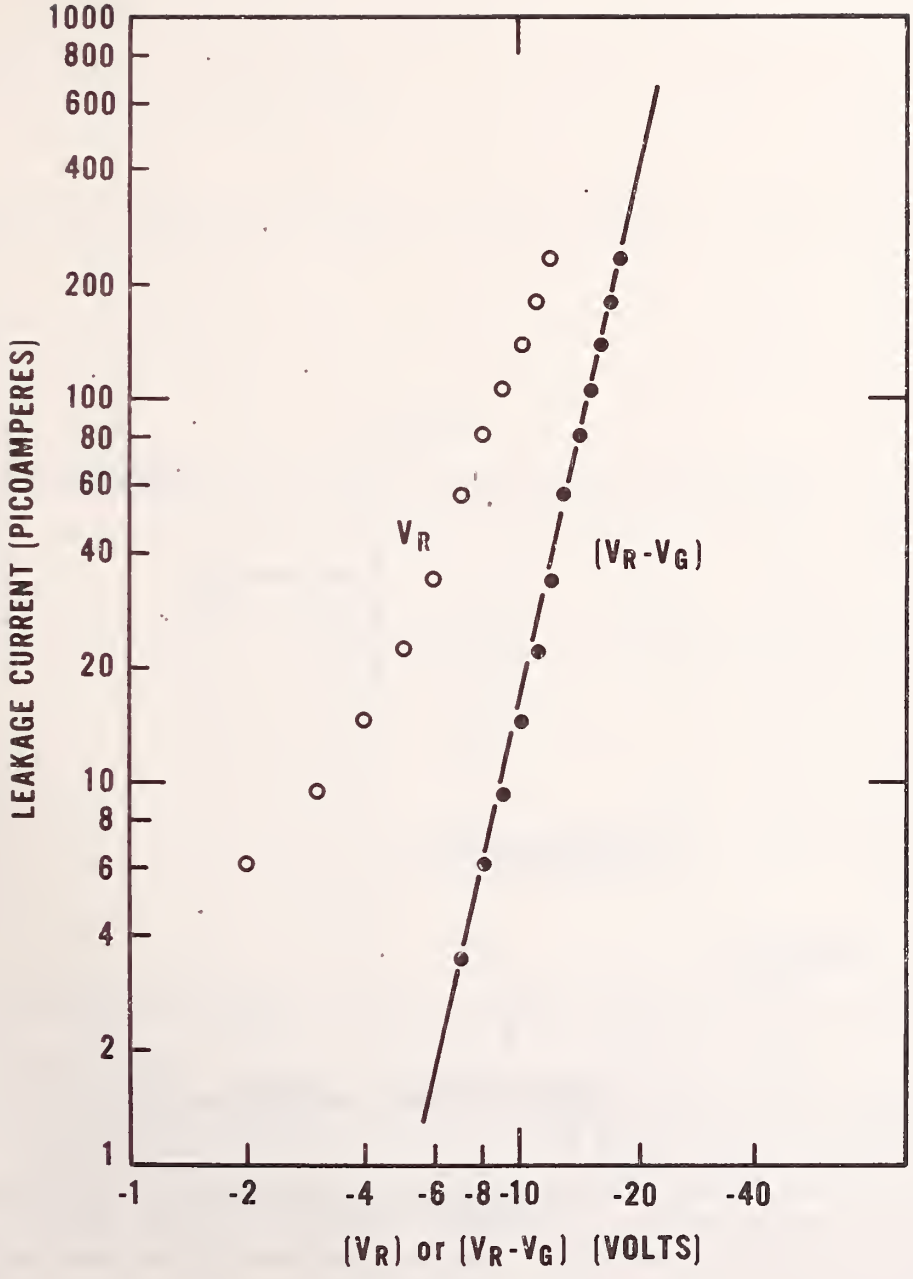

Figure 3. The excess leakage current in accumulation plotted against the junction reverse-bias voltage V_R and the junction-to-gate voltage $(V_R - V_G)$ for a cross-shaped gated diode. The latter quantity is proportional to the perimeter field strength.

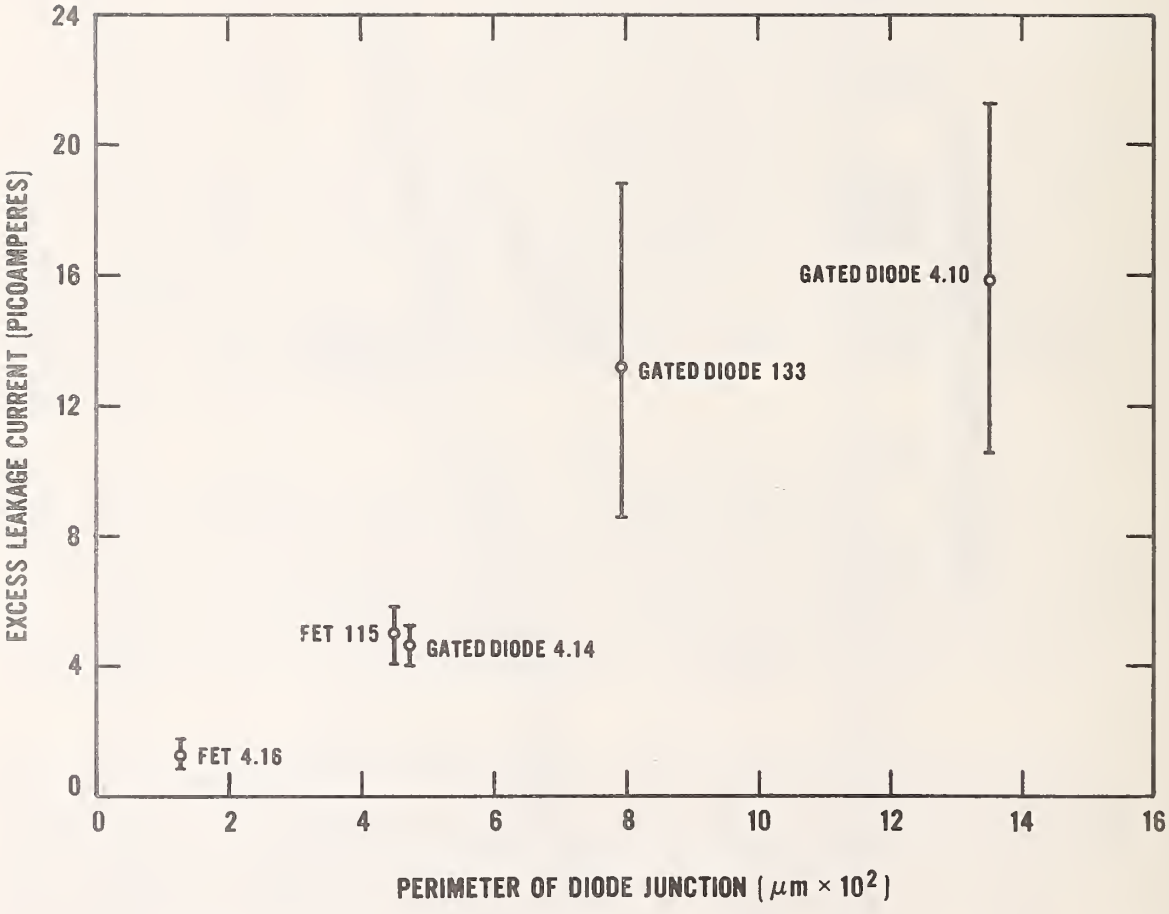

Figure 4. The excess leakage current as a function of junction perimeter for several gated diodes and MOSFETs operated as gated diodes. The reverse-bias voltage was 10 V. The proportionality between excess leakage and junction perimeter length provides further evidence for a field-induced soft breakdown mechanism at the junction-to-gate perimeter.

Table 2

Lifetime and Surface Recombination Velocities[a]

Structure Designation	I_g (pA)	τ (μs)	I_s (pA)	S_o (cm/s)	I_{gg} (pA)	τ_g (μs)
4.16	6.2	6.3	0.23	16	6.8	1.0
12.115	8.0	3.6	3.1	39	6.0	6.3
4.14	1.7	64.0	2.1	9	1.0	109.0
12.133	3.0	28.0	1.2	12	-	-
4.10	11.0	80.0	22.0	12	28.0	31.4

[a]The tabulated values represent averages from several devices. No attempt was made to analyze the results statistically. The range in measured values from different samples of a particular structure was about a factor of two. The numbers here are presented to show the approximate value of measured quantities.

2.3 Concept of the Integrated Test Structure

The Integrated Gated-Diode Electrometer consists of a gated diode with an on-chip, integrally connected, electrometer amplifier and a reset MOSFET [4,5]. The circuit diagram is shown in figure 5. The circuit elements are connected to external components through the probe or bonding pads represented by the square symbols.

The essence of the gated-diode electrometer is that the measurement of extremely small leakage currents is transformed into a much more convenient measurement of voltage signals. Thus, a very delicate, difficult, and slow measurement becomes a tolerant one which is amenable to automated data acquisition. The conversion occurs through the strategy of measuring the voltage decay of the diode. The diode junction is initially reverse biased, a MOSFET switch which connects the diode to the bias supply is opened, and the voltage across the junction is monitored as the leakage currents begin to dissipate the charge stored in the depletion region under the junction and gate.

The circuit analysis of the integrated test structure can be approached from two perspectives: 1) either the inclusive equivalent circuit can be analyzed or 2) the time evolution of the diode voltage can be treated as an input signal to the amplifier, which in turn operates via a transfer function to convert the input signal to an output. The latter approach is more attractive in that it suggests a building block analysis which could be very revealing phenomenologically. Unfortunately, it suffers from the failing that there is no reliable way to include interferences (such as loading) between the diode and the amplifier. As will be seen, capacitive loading of the diode is a major interference.

We choose a hybrid analytical path. We first examine the open-circuit voltage decay (OCVD) of the diode as this is the ideal condition. We then outline a mathematical analysis of the equivalent circuit.

It should be mentioned at the outset that it is not feasible to measure the reverse-bias OCVD of the diode directly using off-chip instruments because the diode output impedance is very large and its capacitance is very small.

2.3.1 Open-Circuit Voltage Decay of an Initially Reverse-Biased *pn* Junction

For a one-sided abrupt junction, the electric field E_o at the junction is

$$E_o = \frac{qNW}{\varepsilon} \tag{5}$$

where q is the electronic charge, N is the dopant density, W is the depletion layer width, and ε is the semiconductor dielectric constant times the permittivity of free space. The displacement current I_d at the junction is given by

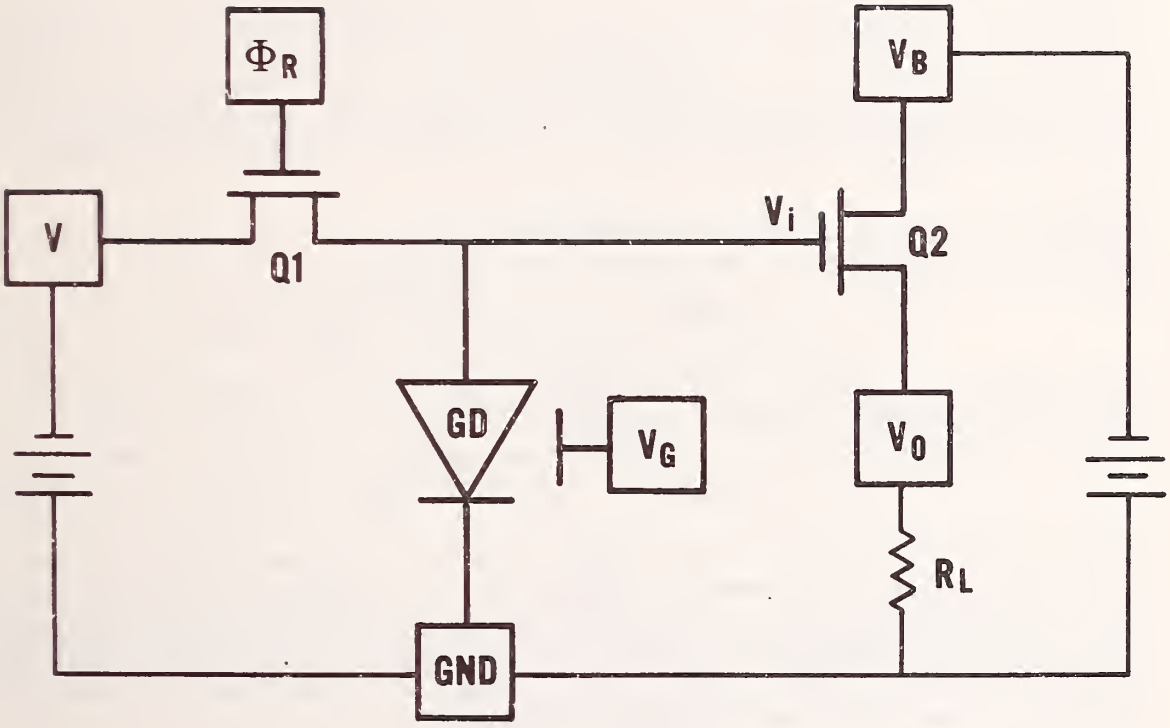

Figure 5. Schematic circuit diagram for the Integrated Gated-Diode Electrometer with a source-follower electrometer. The squares represent probe pads. The heavy lines denote portions of the circuit which are contained on the wafer.

$$I_d = \varepsilon A_j \frac{dE_o}{dt} \tag{6}$$

where A_j is the junction area. The combination of the above relations leads to

$$I_d = qA_jN \frac{dW}{dt} . \tag{7}$$

The depletion layer width of a one-sided abrupt junction is

$$W = \sqrt{\frac{2\varepsilon}{qN}} \left(V_R + V_b \right)^{1/2} \tag{8}$$

where V_R is the externally applied reverse-bias voltage and V_b is the built-in voltage.

Differentiation of eq (8) and substitution into eq (7) yields an expression for I_d in terms of the reverse-bias voltage:

$$I_d = \sqrt{\frac{qN\varepsilon}{2}} \; A_j \left(V_R + V_b \right)^{-1/2} \frac{dV_R}{dt} . \tag{9}$$

When $V_R >> V_b$, this expression reduces to

$$I_d = \sqrt{\frac{qN\varepsilon}{2}} \; A_j \, V_R^{-1/2} \frac{dV_R}{dt} . \tag{10}$$

The voltage of an open-circuit diode, initially reverse biased to voltage V_R, decays due to the leakage current I_L. The leakage current discharges the junction capacitance, collapsing the depletion region. If the leakage current is therefore set equal to the negative of the expression for the displacement current (they flow in opposite directions), a relation between I_L and the diode voltage is obtained,

$$I_L = -\sqrt{\frac{qN\varepsilon}{2}} \; A_j \, V_R^{-1/2} \frac{dV_R}{dt} . \tag{11}$$

It is significant that this expression is equivalent to

$$- I_L = \frac{\varepsilon A_j}{W} \frac{dV_R}{dt} , \tag{12}$$

where $\frac{\varepsilon A_j}{W}$ is the small-signal capacitance of the junction C. That is,

$$- I_L = C \frac{dV_R}{dt} . \tag{13}$$

It must be recognized that the small-signal capacitance C, the quantity usually measured by an ac capacitance bridge, is an incremental capacitance whose value is given by the expression

$$C = \frac{\Delta Q}{\Delta V_R} , \tag{14}$$

where ΔQ is the change in stored charge Q associated with a change in voltage ΔV_R. The total junction capacitance C_T, given by

$$C_T = \frac{Q}{V_T} \tag{15}$$

[where V_T is the total voltage ($V_R + V_b$) across the junction], is twice the small-signal capacitance. The necessity to understand this difference is due to the form of eq (13) which might cause confusion because C is voltage dependent although it is not included in the derivative. If I_L is written in terms of C_T, the corresponding expression would be

$$I_L = \frac{d(C_T V_T)}{dt} . \tag{16}$$

The exact time evolution of the diode OCVD may be calculated by inserting the proper expression for the leakage current into eq (11).

As an illustration, we show the calculation for the simplest case, when I_L is a pure generation current, say from an ideal gated diode with its gate biased so that the surface beneath the gate is accumulated. The generation current is given by eq (1). If $V_R >> V_b$, then $W >> W_f$ and I_g may be simplified to

$$I_g = qgA_j W . \tag{17}$$

Substituting for W from eq (8) and neglecting V_b, one obtains the generation current as

$$I_g = A_j\, g \sqrt{\frac{2\varepsilon q}{N}} \sqrt{V_R} . \tag{18}$$

The OCVD follows from eq (11) with $I_L = I_g$:

$$A_j\, g \sqrt{\frac{2\varepsilon q}{N}} \sqrt{V_R} = -\sqrt{\frac{qN\varepsilon}{2}}\; A_j \frac{1}{\sqrt{V_R}} \frac{dV_R}{dt} , \tag{19}$$

which simplifies to the following differential equation:

$$-\frac{2g}{N}\, dt = \frac{dV_R}{V_R} . \tag{20}$$

The solution provides the evolution of the diode reverse-bias voltage:

$$V_R = V_R(0)\, \exp\left(-\frac{2g}{N}\, t\right), \tag{21}$$

where $V_R(0)$ is the initial reverse-bias voltage impressed across the diode junction and t is time. In this case, there is a characteristic

time constant for the decaying diode voltage. Since $g = n_i/2\tau$, from eq (4a), the time constant T is given by

$$T = \frac{N}{n_i}\tau \quad . \tag{22}$$

Thus, the time constant for the diode voltage decay when the gate is biased into accumulation is N/n_i times longer than the lifetime.

The voltage decay is not described by an exponential with a single characteristic time constant except when the leakage current is a pure bulk generation current, as in the simple case described above. For any other leakage current mechanism or combination of mechanisms, eq (1) remains correct, although the exact expression for V_R as a function of t may not be easily obtained. However, the diode reverse-bias voltage and the voltage decay rate at any particular time are the only experimental parameters necessary to calculate the total leakage current under any condition.

The OCVD of the diode was derived above for the ideal condition. As mentioned earlier, it is not possible to directly measure the voltage decay without having the measurement instruments affect the measurement, that is, distort the decay in some way.

2.3.2 Equivalent Circuit for the Gated Diode

From the above discussion, it should be evident that a simple equivalent circuit for the gated diode is a current source in parallel with a capacitor. Both elements will, in general, be voltage dependent due to the changing depletion layer width as the junction voltage decays. The current source, which represents the leakage current, may have several components with different voltage dependences, each component corresponding to a different source of leakage current. The capacitor, which reflects the charge stored in the depletion region, does not depend on the leakage current mechanism, but does have two components when the gate is biased into inversion. In that regime, the capacitance of the depletion region under the gate must be included additively. For all other regimes, the capacitance is just the diode junction small-signal capacitance.

Again, the situation is most simply illustrated for the case when the diode gate is biased into accumulation and the leakage current is the bulk generation current I_g. The value of the current source I is then

$$I = A_j\, g \sqrt{\frac{2\varepsilon q}{N}} \sqrt{V_R} \quad . \tag{23}$$

The value of the capacitance C is

$$C = \frac{\varepsilon A_j}{W} \tag{24}$$

or, from eq (8)

$$C = \sqrt{\frac{qN\varepsilon}{2}}\, A_j \frac{1}{\sqrt{V_R}} . \tag{25}$$

In the equivalent circuit for the gated diode, a current source in parallel with a capacitor, the node equation may be simply written:

$$-I = C \frac{dV_R}{dt} \tag{26}$$

or

$$\frac{d(\ln V_R)}{dt} = -\frac{2g}{N} . \tag{27}$$

The solution is

$$V_R = V_R(0) \exp\left[-\frac{2g}{N} t\right], \tag{28}$$

and the time constant T is, as before,

$$T = \frac{N}{2g} \tag{29}$$

or

$$T = \frac{N}{n_i} \tau . \tag{30}$$

2.4 Equivalent Circuit for the Integrated Gated-Diode Electrometer

We analyze a configuration which uses a source-follower amplifier to convert the leakage current to a voltage signal. One would suppose that the source-follower configuration is more desirable than other amplifier configurations because its input capacitance is less than the others and because its output impedance can be easily tailored to match the low input impedances of measuring instruments. These advantages are borne out by the analysis, but it will be evident shortly that consideration of the OCVD of the diode as an input signal to the source-follower is not a correct method of analysis. Nor is it correct to consider the input capacitance of the source-follower as an impedance load on the diode. The capacitance of the source-follower does influence the behavior of the diode voltage decay, but not in the way a passive load would affect it. Specifically, the decay rate of the diode with the amplifier is not that deduced by considering the total input capacitance of the source-follower as a single capacitance.

An equivalent circuit for the Integrated Gated-Diode Electrometer is shown in figure 6. The gated diode elements, I and C, are shown within the dotted box at the left. The electrometer MOSFET is replaced by a current source representing the drain current I_{DS} and appropriate resistors and capacitors. Resistors representing the source, drain, and drain-to-source resistance are omitted. The load is a resistive load of value R_L. The equivalent capacitances are the MOSFET gate-to-source

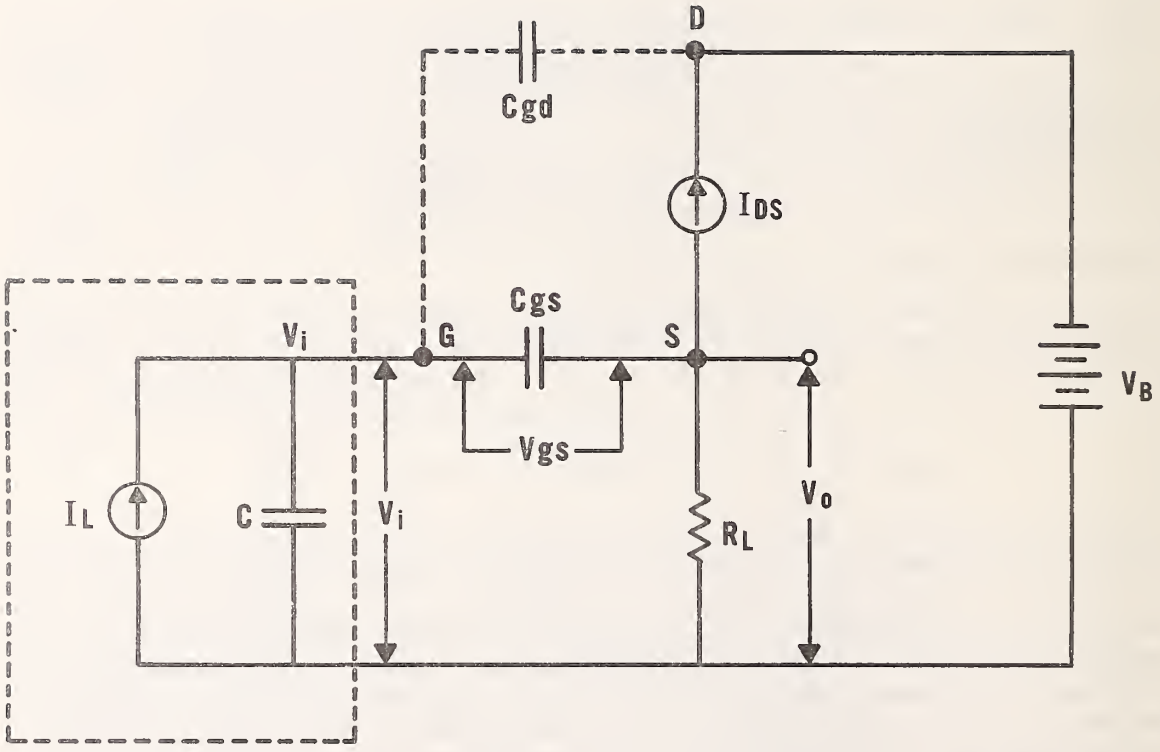

Figure 6. Equivalent circuit for the Integrated Gated-Diode Electrometer. The current source and capacitor within the dotted rectangle represent the gated diode. The gate, source, and drain of the MOSFET electrometer are identified by the symbols G, S, and D, respectively. I_{DS} is the MOSFET drain-to-source current, C_{gs} is the MOSFET gate-to-source capacitance, and R_L is the resistive load. The capacitor, C_{gd} represents the MOSFET gate-to-drain capacitance which is dotted because it is in parallel with the diode junction capacitance C and may therefore be omitted from the analysis. The input voltage V_i, the output voltage V_o, the MOSFET gate-to-source voltage V_{gs}, and the MOSFET drain bias voltage V_B are indicated in the circuit.

capacitance C_{gs} and the gate-to-drain capacitance C_{gd}. Both capacitances include intrinsic and parasitic contributions and are the dominant MOSFET capacitance components in the case of saturated operation. All other capacitances are either referenced to the source or the drain (capacitances between the input and the wafer, or ground, are referenced to the drain) and are added in parallel with C_{gs} or C_{gd}. It should also be noted that C_{gd} is in parallel with C and can be omitted from the mathematical relations so long as it is added to C at the end. The voltages are V_i, the MOSFET input voltage given by the reverse-bias voltage across the diode junction; V_o, the output voltage developed across R_L; and V_{gs}, the MOSFET gate-to-source voltage. It is apparent from the circuit that

$$V_i = V_{gs} + V_o \ . \tag{31}$$

For the source-follower with a resistive load, the current source I_{DS} may be approximated by the linear expression

$$I_{DS} = g_m \ (V_{gs} - V_{TX}) \tag{32}$$

or

$$I_{DS} = g_m \ (V_i - V_o - V_{TX}) \tag{33}$$

where g_m is the MOSFET mutual transconductance and V_{TX} is the extrapolated threshold voltage.

The node equations for the input and output nodes are:

$$\text{input node:} \quad -I = C \frac{dV_i}{dt} + C_{gs} \frac{dV_i}{dt} - C_{gs} \frac{dV_o}{dt} \tag{34}$$

$$\text{output node:} \quad I_{DS} = \frac{1}{R_L} V_o + C_{gs} \frac{dV_o}{dt} - C_{gs} \frac{dV_i}{dt} \ . \tag{35}$$

The mathematical description of the time evolution of the input and output voltage signals in the integrated test structure is constrained by the following condition: The voltage across the diode junction is held constant by the reset switch until t = 0. At that time, the reset switch is opened and the charge stored in the diode depletion regions is allowed to dissipate. At t = 0, the node equations are subject to the initial conditions

$$V_i = V_R(0) \tag{36}$$

and

$$V_o = \beta(V_i - V_{TX}) \ , \tag{37}$$

where β is the dc voltage gain, defined by

$$\beta = \frac{g_m}{g_m + \frac{1}{R_L}} . \tag{38}$$

Until t = 0, dc conditions obtain. Before continuing with the mathematical description of the behavior of the node equations, it is instructive to make a few observations. First, if $C_{gs} = 0$, V_i is just the OCVD and $V_o = \beta(V_i - V_{TX})$ for all times. That is, when $C_{gs} = 0$, the MOSFET does not load the diode and the voltage gain of the source follower is just the dc voltage gain. The loading is represented by the terms involving C_{gs} (plus C_{gd}, which we have not explicitly included and which acts only to increase C). It is these terms which complicate the analysis.

Another interesting observation is that the output node equation, in combination with eq (31), gives the voltage gain A_v of the source follower when time-varying signals are present:

$$A_v = \frac{V_o}{(V_i - V_{TX})} = \frac{g_m + C_{gs}\frac{dV_i}{dt}\frac{1}{(V_i - V_{TX})}}{\frac{1}{R_L} + g_m + C_{gs}\frac{dV_o}{dt}\frac{1}{V_o}} . \tag{39}$$

When C_{gs} approaches 0, the ac and dc gains are equal, that is, $A_v = \beta$.

It is tempting to define A_v as a constant and incorporate $V_o = A_v(V_i - V_{TX})$ into eq (33). This procedure, however, is incorrect. In fact, it is precisely because the effective voltage gain is dependent upon the rate of change of V_i and V_o that the solution to the node equations is not straightforward.

In practice, it is not necessary to obtain the complete solution to the pair of simultaneous differential equations produced by the node analysis. Evaluation of eqs (34) and (35) at t = 0 and insertion of the initial conditions [eqs (36) and (37)] lead to the relations

$$-I = C\left.\frac{dV_i}{dt}\right|_{t=0} + C_{gs}\left.\frac{dV_i}{dt}\right|_{t=0} - C_{gs}\left.\frac{dV_o}{dt}\right|_{t=0} \tag{40}$$

and

$$g_m\ V_R(0) - \beta(V_R(0) - V_{TX}) - V_{TX} = \frac{\beta(V_R(0)-V_{TX})}{R_L} + C_{gs}\left.\frac{dV_o}{dt}\right|_{t=0} - C_{gs}\left.\frac{dV_i}{dt}\right|_{t=0} . \tag{41}$$

Simple manipulation shows that the second relation requires that either

$$C_{gs} = 0 \tag{42}$$

or

$$\left.\frac{dV_i}{dt}\right|_{t=0} = \left.\frac{dV_o}{dt}\right|_{t=0} . \tag{43}$$

The latter equality is the more meaningful case. The first differential equation above [eq (40)] then requires that the initial voltage derivatives are simply -I/C; that is,

$$\left.\frac{dV_i}{dt}\right|_{t=0} = \left.\frac{dV_o}{dt}\right|_{t=0} = -\frac{I}{C} , \tag{44}$$

where I and C correspond to values of leakage current and capacitance at t = 0 when the reverse-bias voltage is $V_R(0)$.

The key feature of this result is that at t = 0, immediately after the reset switch is closed and the diode voltage decay begins, the output voltage decay rate is exactly that given by the unloaded diode open circuit voltage decay. The measured voltage is thus determined by the diode leakage current I and the parallel capacitance C.

The above analysis is valid at t = 0 and remains valid for a time after t = 0 which is short compared to the time constant of the exponential terms of the complete solution for the output voltage as a function of time. The time constant T_1 in the exponential terms of the complete solution is

$$T_1 = \frac{R_L C C_{gs}(1 - \beta)}{[C + (1 - \beta)C_{gs}]} . \tag{45}$$

This characteristic time corresponds to the discharging of C_{gs}. Note that the lengthening of T_1 by increasing C_{gs} or decreasing β may have other undesirable effects. Increasing C_{gs} by increasing the area of the electrometer MOSFET gate will also increase C_{gd}, and thus C, by an incompletely controllable amount. It may be advantageous to overlap the MOSFET gate and source by a large amount. Decreasing β has limited value because the output voltage amplitude will decrease and the precision of the measurement will be sacrificed.

A separate consideration, which was mentioned earlier, is the necessity to account for all parasitic capacitances referenced to the MOSFET drain and to ground. These capacitances are in parallel with the junction capacitance C. They include the capacitance due to the connecting regions between the diode and the MOSFET gate over thick field oxide and over the drain and the capacitance due to the overlap of the diode gate over the diffusion. (The latter capacitance is actually in series with the diode gate-to-ground capacitor, which is much larger and may be thought of as a

short to ground.) These capacitances may simply be added algebraically to C, the diode junction capacitor. The difficulty with the parasitic or stray capacitances is that they are hard to calculate accurately and thus cause uncertainty in the results. Furthermore, many of the parasitic capacitors are oxide capacitors and may be large relative to the diode junction capacitance, which is a depletion capacitance. For example, in the case of the Integrated Gated-Diode Electrometer on test pattern NBS-12, the sum of all the parasitic capacitances is more than an order of magnitude larger than the diode junction capacitance at a reverse-bias voltage of 6 V. Results from this test structure are shown in the next section.

2.5 High-Speed Test Methods

The measurement objective is the determination of the leakage current amplitude as a function of the condition (accumulation, depletion, inversion) of the semiconductor surface under the diode gate. From values of the leakage current deduced for the three gate regimes, the parameters s_o, the surface recombination velocity, τ and τ_g, the bulk lifetimes under the junction and under the gate, may be obtained. In addition, the magnitude of leakage current caused by mechanisms other than bulk or surface generation may be determined.

The metrology is outlined in the diagram of figure 7. The parameter β is measured by measuring the dc characteristics of the amplifier. The input voltage is the diode reverse-bias voltage which is held constant by holding the MOSFET reset switch on. The output voltage is measured for various values of the input voltage. The slope of the output voltage versus input voltage curve, which is linear over a range of input voltages, is β. The extrapolated threshold voltage, V_{TX}, may also be obtained from these data by extending the linear fit back to the abscissa. This procedure is just the application of eqs (36) and (37) which apply prior to t = 0.

The measurement of I involves the following steps. The desired bias voltage V_G is applied to the diode gate. The diode reverse-bias voltage V_R is set at a convenient value, preferably near the high end of the amplifier linear operating range, and the diode reset switch is turned off with the pulse ϕ_R. The output voltage V_o is then measured after the reset switch is opened and again shortly thereafter to determine the initial rate of decay of the output voltage $\left.\frac{dV_o}{dt}\right|_{t=0}$. The optimal times to use are dependent upon the available equipment and on the decay itself. It helps to observe the decay curve on an oscilloscope. If the decay is slow, the rate of decay can be determined using two points separated further apart in time than if the decay is rapid and noticeably nonlinear.

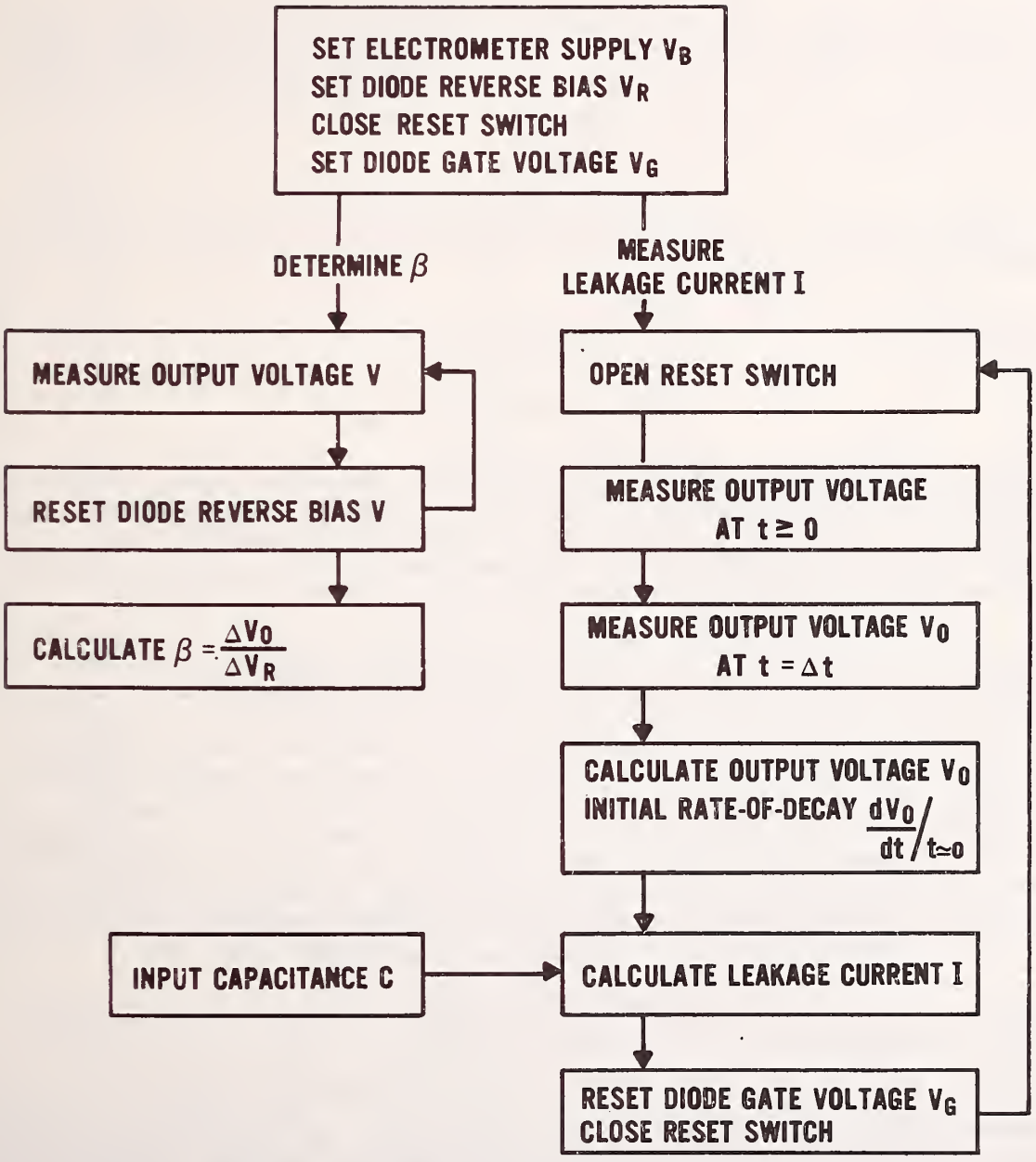

Figure 7. Schematic flow diagram of the measurement procedure for operating the Integrated Gated-Diode Electrometer.

From each value of the output voltage decay, a leakage current can be calculated using a computed value for the small-signal junction capacitance plus all parasitic capacitances referenced to the MOSFET drain and to ground. For the inversion regime, the additional capacitance under the diode gate must also be included. An example of the data for one test structure is shown in figure 8.

In our case, the data were obtained using a digital oscilloscope-based computer system. Examples of the decay which were captured in the computer memory are shown in figure 9.

Values for S_o, τ and τ_g are obtained with the use of eqs (1) through (4).

3. MOSFET dc Profiler

Dopant profiles are usually determined from depletion layer voltage measurements. The measurement traditionally involves use of a 1-MHz signal which is incompatible with production-oriented computerized data-acquisition systems which use relay scanners and probe cards to connect the measuring instruments and power supplies to the test wafer.

The MOSFET dc Profiler is a four-terminal enhancement-mode MOSFET operated in the linear current region. The dopant profile is obtained by dc techniques utilizing the back-gate bias, or body effect. The concept of the method is that the depletion layer is sequentially moved deeper into the semiconductor by increasing the gate voltage and simultaneously increasing the body voltage (both referenced to the source) such that the channel current is held constant. The dopant density as a function of depth is computed from the relation between the pairs of values for the gate and body voltages. The requirement that the channel current is held constant implies that the charge density in the channel is also constant, if field dependent mobility effects are neglected.

The analysis of the MOSFET dc Profiler and a discussion of its limitations are contained in two previous publications [6,7]. Therefore, a detailed discussion of the device is omitted from this report.

The method has been used to profile phosphorus- and boron-implanted layers and uniformly doped substrates and epilayers. Dopant redistribution due to thermal oxidation was easily observed. Studies of the distortion in the computed profile due to a variety of effects, such as high channel conductance which causes an apparent shift in the profile to smaller depths and higher dopant density values, have shown that when the proper corrections are applied dopant density values agree to within 2 percent of junction capacitance-voltage (C-V) values over a wide range of dopant densities.

The region of usefulness of the MOSFET dc dopant profile method has been investigated and is found to roughly conform to the dopant density versus depth region accessible to C-V measurements. But, of course, the dc dop-

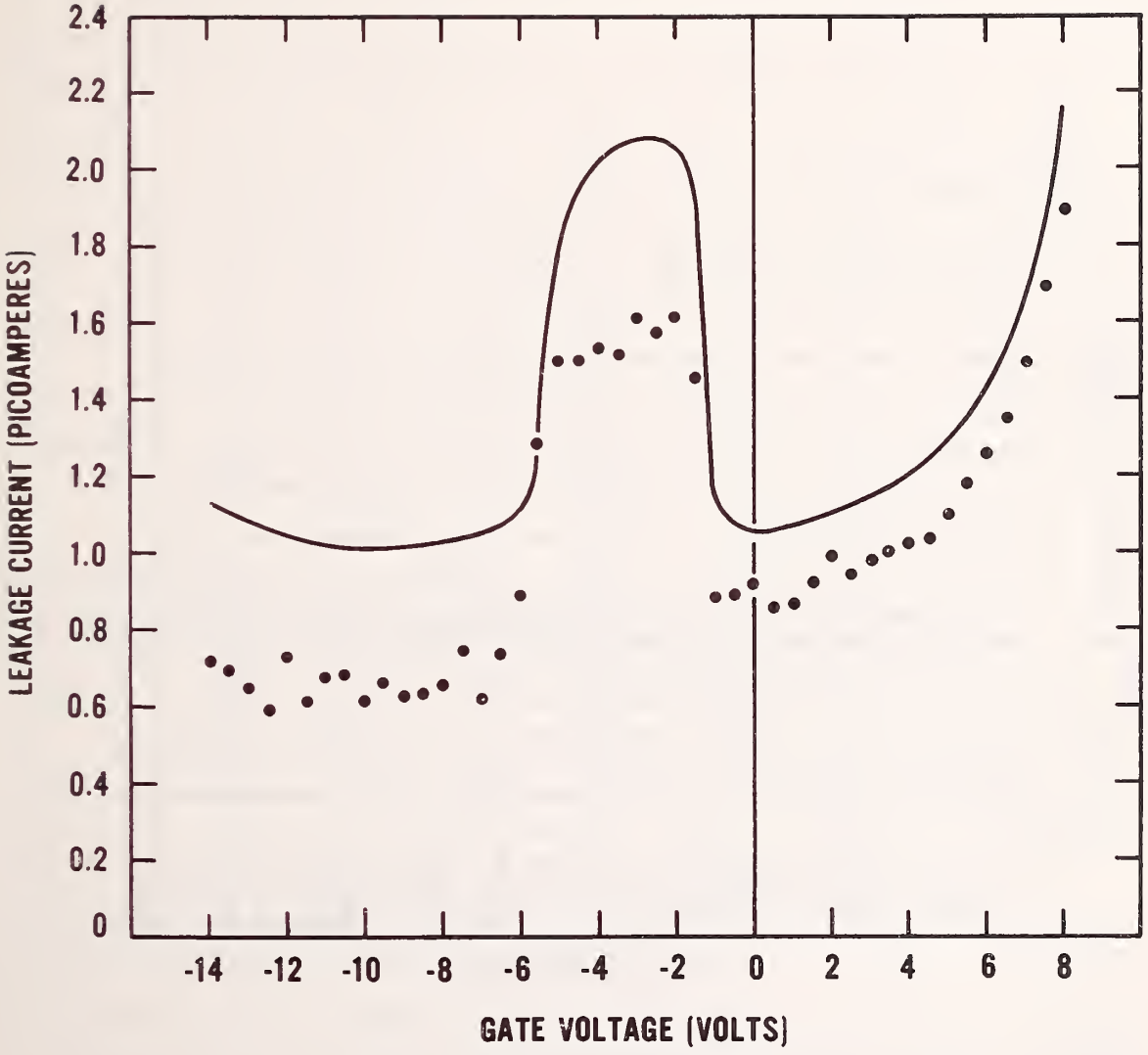

Figure 8. Leakage current *vs.* gate voltage for a cross-shaped Integrated Gated-Diode Electrometer. The solid curve was obtained from the gated diode using an external electrometer by probing the diode directly. The points, which are data obtained by operating the integrated test structure, are computed values of the leakage current obtained using eq (44). Estimated values of the parasitic capacitances were included in the computation.

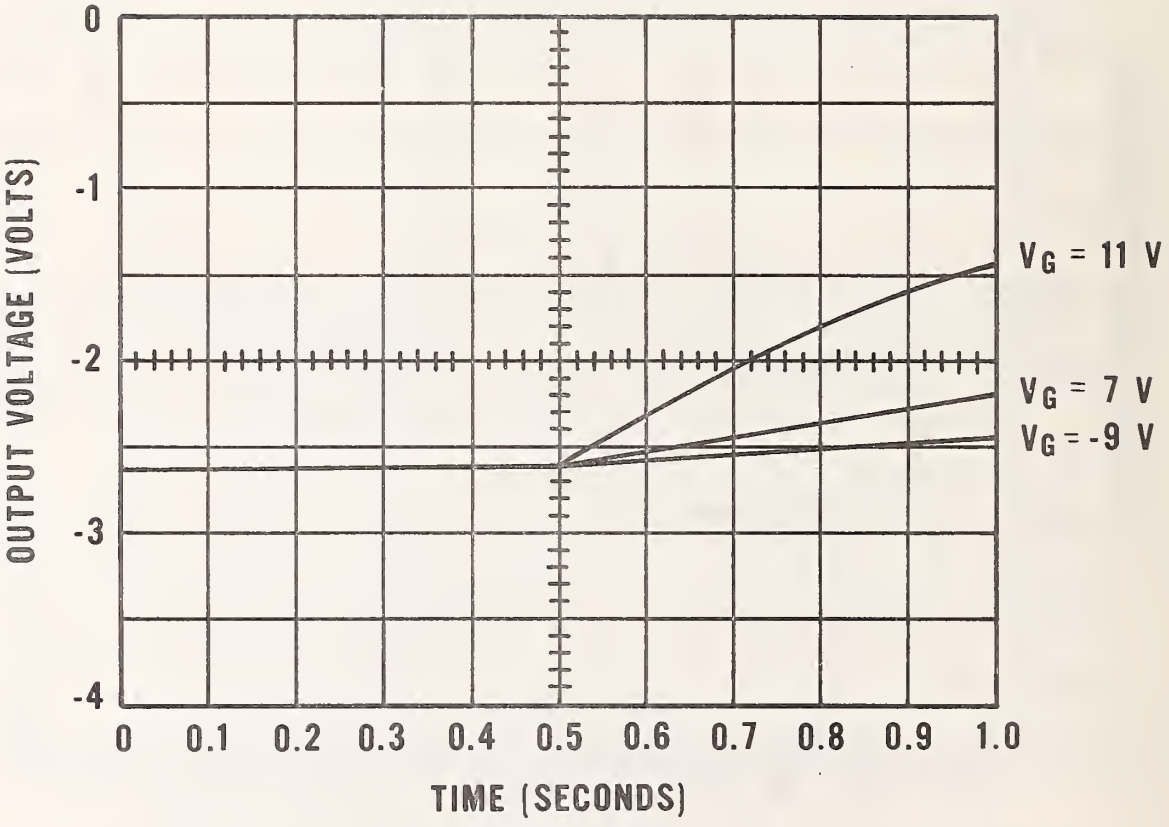

Figure 9. Oscillograms of output voltage *vs.* time for the Integrated Gated-Diode Electrometer. The reset switch was opened at t = 0.5 s. Traces taken at gate voltages V_G of 11, 7, and -9 show examples of how the time-rate-of-change of the output voltage varies as a function of the gate voltage.

ant profile method has the advantage over C-V measurements that it is a high-speed technique.

Data have also been acquired on devices of different channel lengths. A model is being developed to account for small differences which arise between values of dopant density determined by dc profiling and by 1-MHz capacitance measurements when the MOSFET channel length is relatively small. This short-channel effect is most easily visualized by considering the vertical cross section, through the source and the drain, of the depleted volume under the MOSFET gate. The cross section is a trapezoid. As the bottom of the gate field-induced depletion region moves into the semiconductor, the incremental volume of bulk charge which is bound electrostatically to the gate decreases because the area controlled by the gate decreases. For short-channel devices, this decrease is large enough to observe experimentally and must be corrected for. The improved model will include an analytical description of the evolution of the shape of the depletion volume as it is moved to greater depths with increasing gate-to-body voltage, thus allowing greater accuracy in values of the dopant density.

Advanced designs for the MOSFET dc Profiler have been developed which enable it to profile shallow buried layers used in buried channel CCDs. A diagram of the cross section of this device is shown in figure 10. The problem with shallow buried layers is that the source and drain of the MOSFET must be even shallower to obtain an enhancement-mode configuration. The need for additional, very shallow layers is avoided in the new designs by using a dual-gate MOSFET structure. The source and drain are contained within tubs. The second split gate is used to invert the edge of the tub so that the inversion channel, which is created in the buried layer by the control or profiling gate, is electrically coupled to the source and drain. This device should be compatible with radiation-hardened CCD processes if the deep diffusion for the tubs is introduced at the beginning of processing.

The equations for the MOSFET dc Profiler are

$$W = (\varepsilon_s X_o/\varepsilon_o)(dV_{SB}/dV_{GS}) \tag{46}$$

and

$$N(W) = (\varepsilon_o^2/q\varepsilon_s X_o^2)(d^2V_{SB}/dV_{GS}^2) \tag{47}$$

where W is the width of the depletion region in the silicon, ε_s and ε_o are the silicon and oxide dielectric constants times the permittivity of free space, q is the electronic charge, X_o is the oxide thickness, V_{SB} and V_{GS} are the source-to-body and gate-to-source voltages and N(W) is the dopant density at a depth into the silicon corresponding to W. Correction factors for the field dependence of the channel mobility and comments about other limitations are given in reference [7].

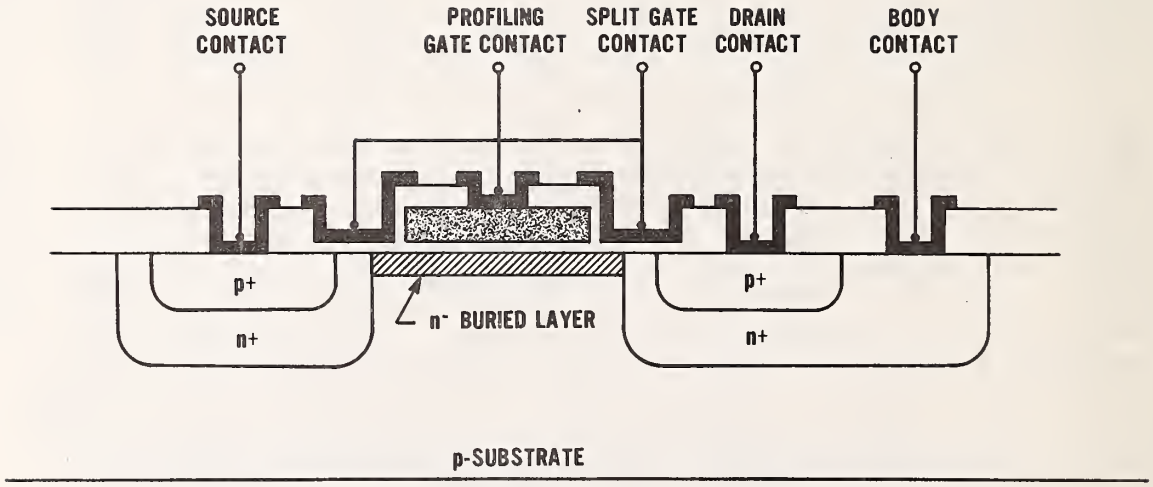

Figure 10. Schematic of the dual-gate MOSFET dc Profiler configuration for profiling a shallow buried layer.

The equations are useful for depletion depths from about three Debye lengths from the surface (where the depletion approximation breaks down and it is not useful to think of a well-defined edge to the depletion region) to a depth where avalanche breakdown occurs somewhere in the device because the voltages are large. Similar constraints govern the accessible profiling range in capacitance-voltage measurements.

The algorithm for profiling using the MOSFET dc Profiler is diagrammed schematically in figure 11. The circuit for the measurement is given in the references [6,7].

4. Recommended Designs for Production-Compatible Test Pattern

4.1 Background

The test pattern effort at NBS is devoted to developing well-designed and well-characterized test structures that can be used to obtain correct results and that are testable with automated test systems. Drawing upon previous results and experience, a selected group of test structures has been assembled for the evaluation of the fabrication and performance of radiation-hardened CCD imagers.

The NBS test structures are arranged in a 2 by N array [8]. The structures are isolated from each other and are modular. The probe pads are an integral part of the test structures. This arrangement allows the development of standard test structures that are accessible with one probe card, are easy to arrange within a test pattern, and provide for a pattern-independent data base. This approach overcomes interferences which may be encountered when common conductors are used between structures.

The dimensions of the 2 by N probe-pad array as used at NBS are a square probe pad 80 μm on a side and separated by 80 μm from its nearest neighbors in the array. A diagram of the 2 by N array is shown in figure 12. The pad-to-pad separation between arrays is 60 μm. The overall width allowed for the array is 300 μm, although the test structures need not always be confined to the area between the probe pads.

Sometimes specific requirements of the test program may lead to modification of the 2 by N arrangement. For example, if it is necessary to bond and package the test structures, the 2 by N probe-pad array is awkward. Larger probe pads may be required in certain situations. In such cases, the dimensions and guidelines referred to may be liberalized.

4.2 Proposed Test Structure Library

A list of proposed parametric test structures for the radiation-hardened CCD program is given in table 3. The test structures include a variety of improved designs of existing NBS-developed devices in addition to new advanced test structures which were developed during this program.

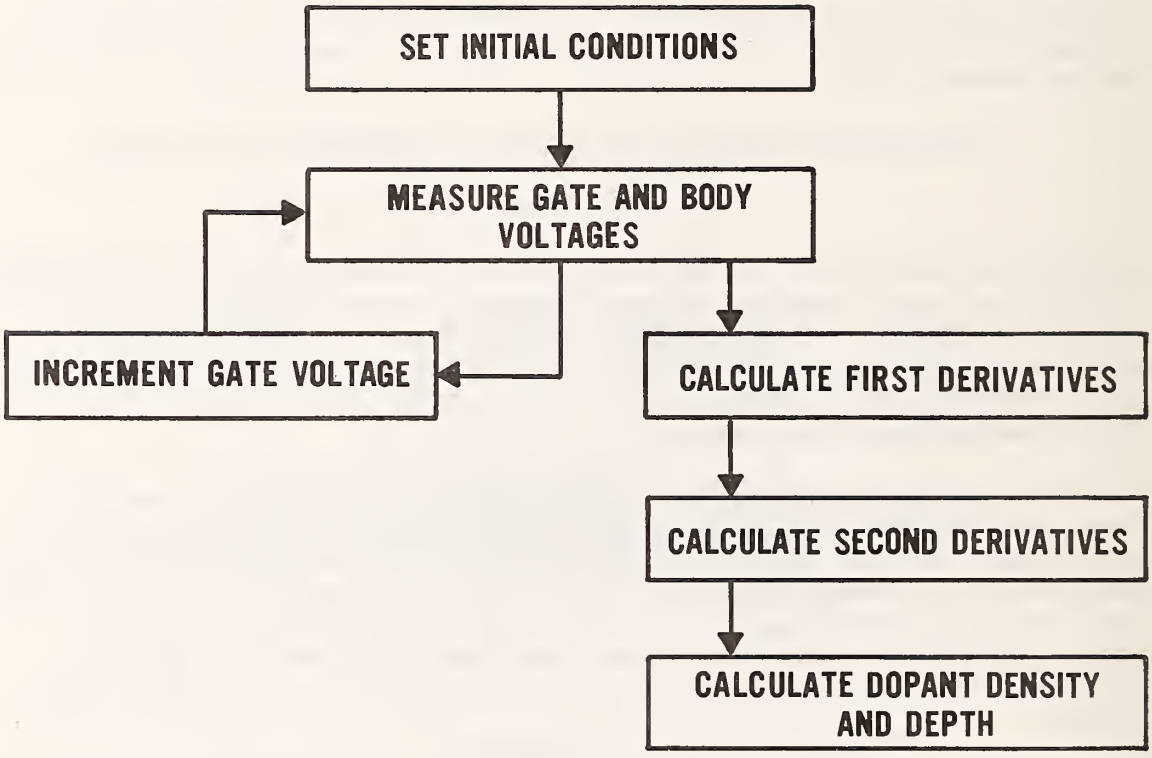

Figure 11. Schematic flow diagram of the measurement procedure for operating the MOSFET dc Profiler.

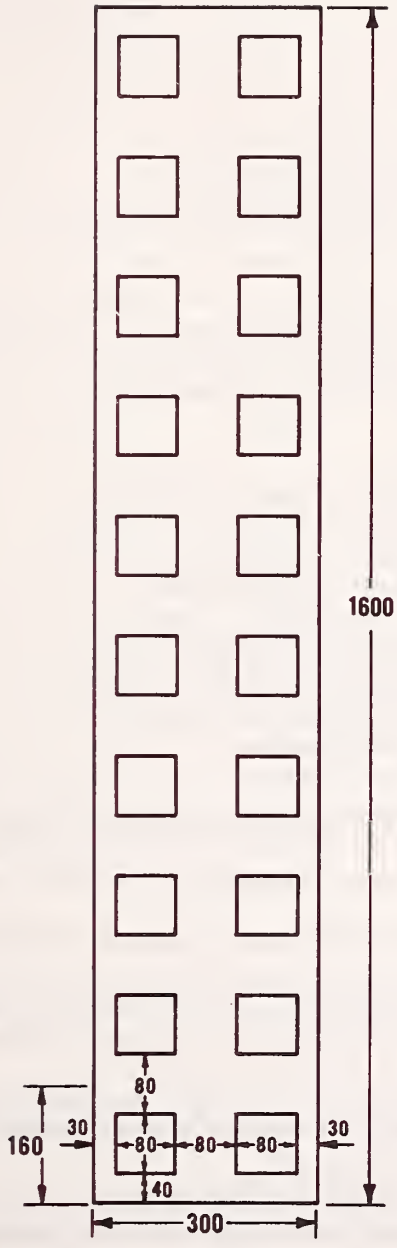

Figure 12. Layout drawing of the NBS 2 by 10 probe-pad array. All dimensions are in units of micrometers.

Table 3

Proposed Parametric Test Structures for Radiation-Hardened CCD Process

1. Linewidths and Sheet Resistances

   a. Metal cross-bridge sheet resistor
   b. n^+ cross-bridge sheet resistor
   c. n^- cross-bridge sheet resistor
   d. Polysilicon cross-bridge sheet resistors

2. Alignment

   a. Polysilicon electrical alignment test structures
   b. n^+ electrical alignment test structure
   c. p^+ electrical alignment test structure

3. Contact Resistances

   a. Metal-to-polysilicon contact resistors
   b. Metal-to-n^+ contact resistor

4. Oxide and Interface Characterization

   a. Polysilicon-gate oxide-n^- capacitors
   b. Polysilicon-gate-oxide-substrate capacitors
   c. Polysilicon-polysilicon step coverage and isolation structure
   d. Polysilicon-metal step coverage and isolation structure
   e. n^+ inversion layer detector
   f. n^- inversion layer detector

5. Bulk Generation Lifetimes and Surface Recombination Velocities

   a. Large rectangular Integrated Gated-Diode Electrometers (buried channel)
   b. Large rectangular Integrated Gated-Diode Electrometers (surface channel)
   c. Cross-shaped Integrated Gated-Diode Electrometers (buried channel)
   d. Cross-shaped Integrated Gated-Diode Electrometers (surface channel)
   e. Inverted Integrated Gated-Diode Electrometers (buried channel)
   f. Inverted Integrated Gated-Diode Electrometers (surface channel)

6. Transistor Operating Parameters

   a. Enhancement mode MOSFETs (all combinations of gates and oxides)

7. Buried Layer Profile

   a. Dual gate enhancement mode MOSFET (p-channel in buried layer)
   b. Implanted shallow source/drain enhancement mode MOSFET (p-channel in buried layer)

There are cross-bridge sheet resistors for evaluating sheet resistance and line widths of various layers, alignment resistors for evaluating the amount of misalignment between various photomask levels, and contact resistors for measuring the contact resistance at contact windows. Also included are inversion layer detectors for detecting the presence of an unwanted inversion layer under the field or gate oxides, and a step coverage and isolation structure which is in effect a small random-fault test structure and can be used to estimate oxide strength between metal and polysilicon line crossings. Several MOS and bipolar transistors are used to determine transistor operating parameters. MOS capacitors are included in the event conventional 1-MHz capacitance measurements are deemed necessary and to determine oxide thickness values. Finally, the new test structures described in the previous sections are included. The Integrated Gated-Diode Electrometer can be used to measure leakage current and to determine carrier lifetimes. The MOSFET dc Profiler can be used to measure dopant density as a function of depth.

All the test structures are designed to be compatible with the radiation-hardened CCD processes. However, minor alterations by the vendors will be necessary to assure that the structures comply with their specific process design rules and with bonding requirements for applying bias voltages during irradiation. Also, particular structures will require modifications for application to each of the layers addressed.

Additional parametric structures may be recommended at a later time. It is also expected that modifications to the present designs may be required as the program progresses and the test structure and CCD performance is evaluated before and after radiation exposure. Random fault test structures for inclusion in the final test pattern will be specified during the continuation of this program.

4.3 Descriptions of Proposed Parametric Test Structures

Designs for the proposed parametric test structures are shown in figures 13 through 23. The structures are described in the following paragraphs.

4.3.1 Integrated Gated-Diode Electrometer

New designs for the Integrated Gated-Diode Electrometer incorporate major improvements over previous designs for this device. Each of the designs is versatile in several ways:

a) They are compatible with the NBS 2 by N probe-pad array, although they can also be "bonded out" for packaging and radiation testing.

b) They are compatible with fabrication of the diode gate from any polysilicon or metal layer in a process. A series of similar devices, each examining one of the gate oxide layers, would have the same specifications, thus easing intercomparison.

c) Simplified rectangular shapes are used throughout.

d) They are modular in the sense that the amplifier interconnections are uniform in each design.

e) The amplifier, a source follower with a saturated MOSFET load, may also be used with an external load.

In addition, several of the designs have the capability of also being measured in the conventional manner, using an external picoammeter, with the same probe card. This dual-mode capability allows the possibility (for unbonded devices) of verification or detailed study where it is necessary.

The source-follower electrometer amplifier for use with the gated diode designs is shown in figure 13. It is designed with very tight design rules and may require modification by the vendors. The key feature, which must not be compromised any more than absolutely necessary, is that the total capacitance between the input MOSFET gate and the rest of the structure, including the wafer (ground), is held to a minimum.

A complete Integrated Gated-Diode Electrometer is obtained by combining a gated diode structure with the source-follower. The positioning of the two parts is determined by the required positioning of the probe pads in the 2 by N array.

The following gated diode designs are recommended for the radiation-hardened CCD program:

Large Rectangular Gated Diode (fig. 14)

This structure is expected to be the primary measurement vehicle of the group. It has near-optimal geometrical qualities, compared to an ideal, round, completely gated diode, but avoids complicating features such as metal crossovers and retains all of the versatility mentioned above. In addition, it has a small perimeter-to-area ratio compared to the other devices with smaller areas. (The perimeter-to-area ratio of a square is only 13 percent greater than that of a circle of the same area. Thus, the rectangular shape sacrifices very little in excess perimeter to achieve simplified pattern generation properties.)

Cross-Shaped Gated Diode (fig. 15)

As discussed earlier, measurements on cross-shaped gated diodes revealed an additional and unexpected leakage component due to soft breakdown at the perimeter of the gate. This phenomenon is generally found in gated structures of all types but is often not a problem. In the CCDs, such leakage may contribute significantly to the dark current. The cross-shaped gated diode emphasizes perimeter leakage and it therefore is included. It represents a new and unique tool especially appropriate for radiation testing of the CCDs.

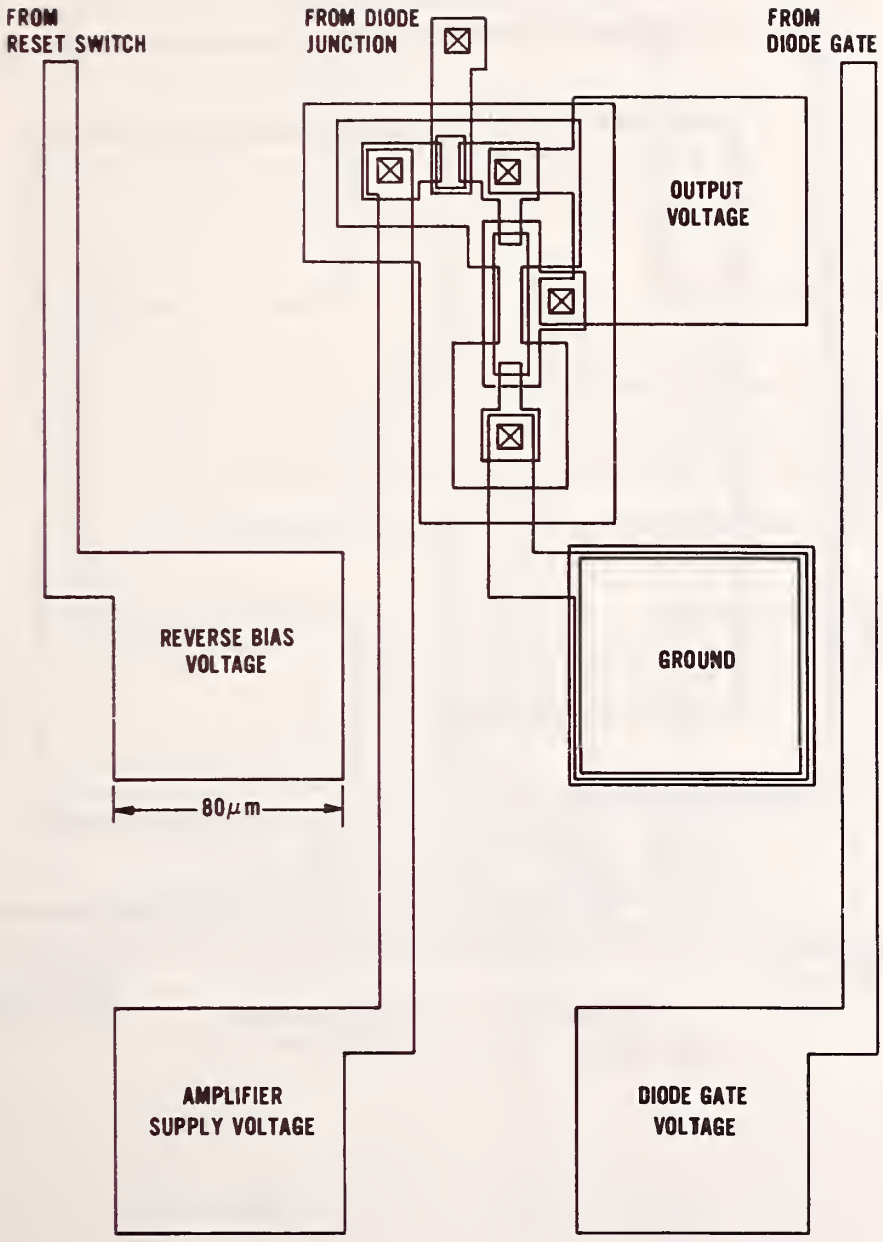

Figure 13. Outline drawing of the source-follower electrometer amplifier with a saturated MOSFET load.

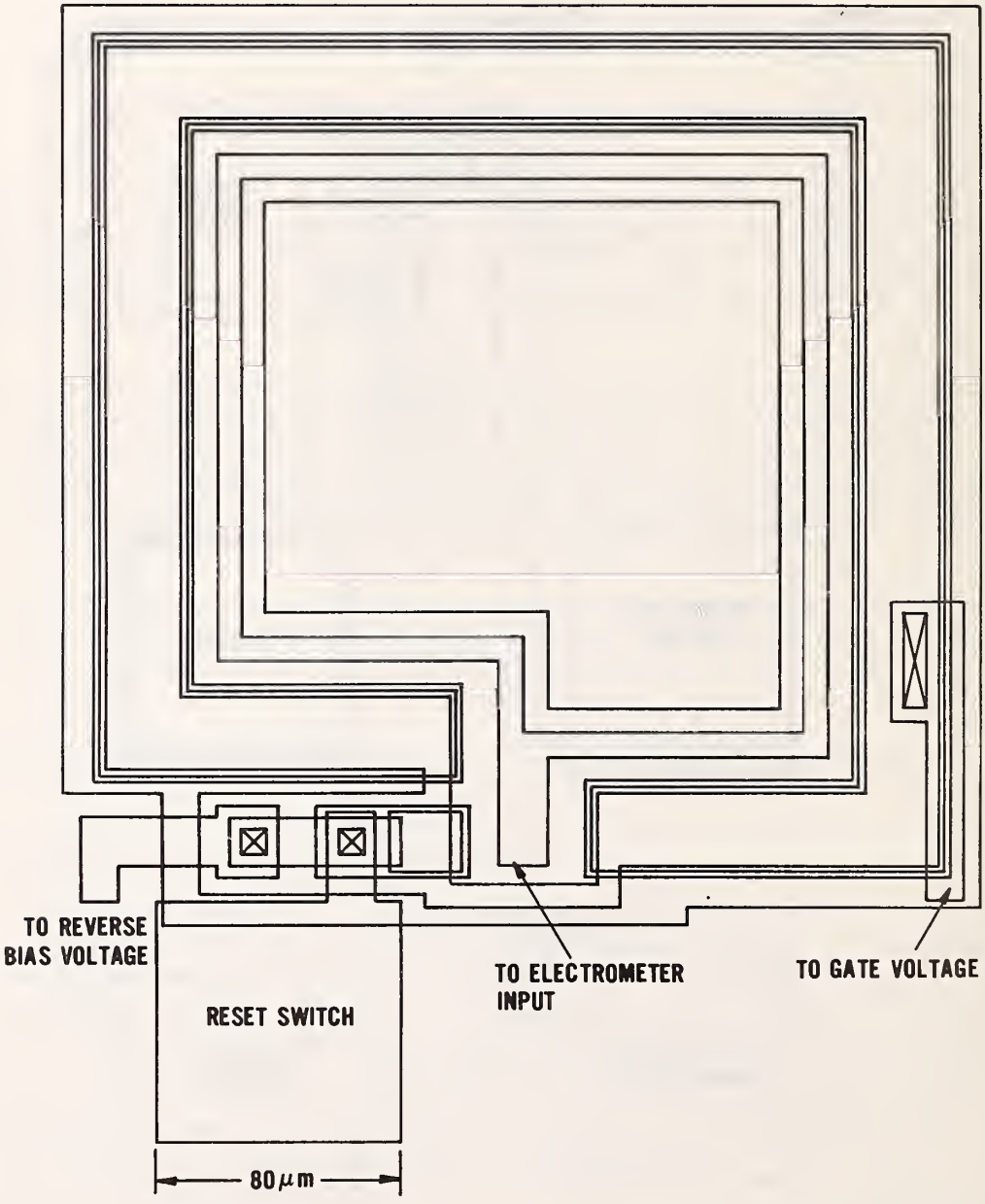

Figure 14. Outline drawing of the rectangular gated diode.

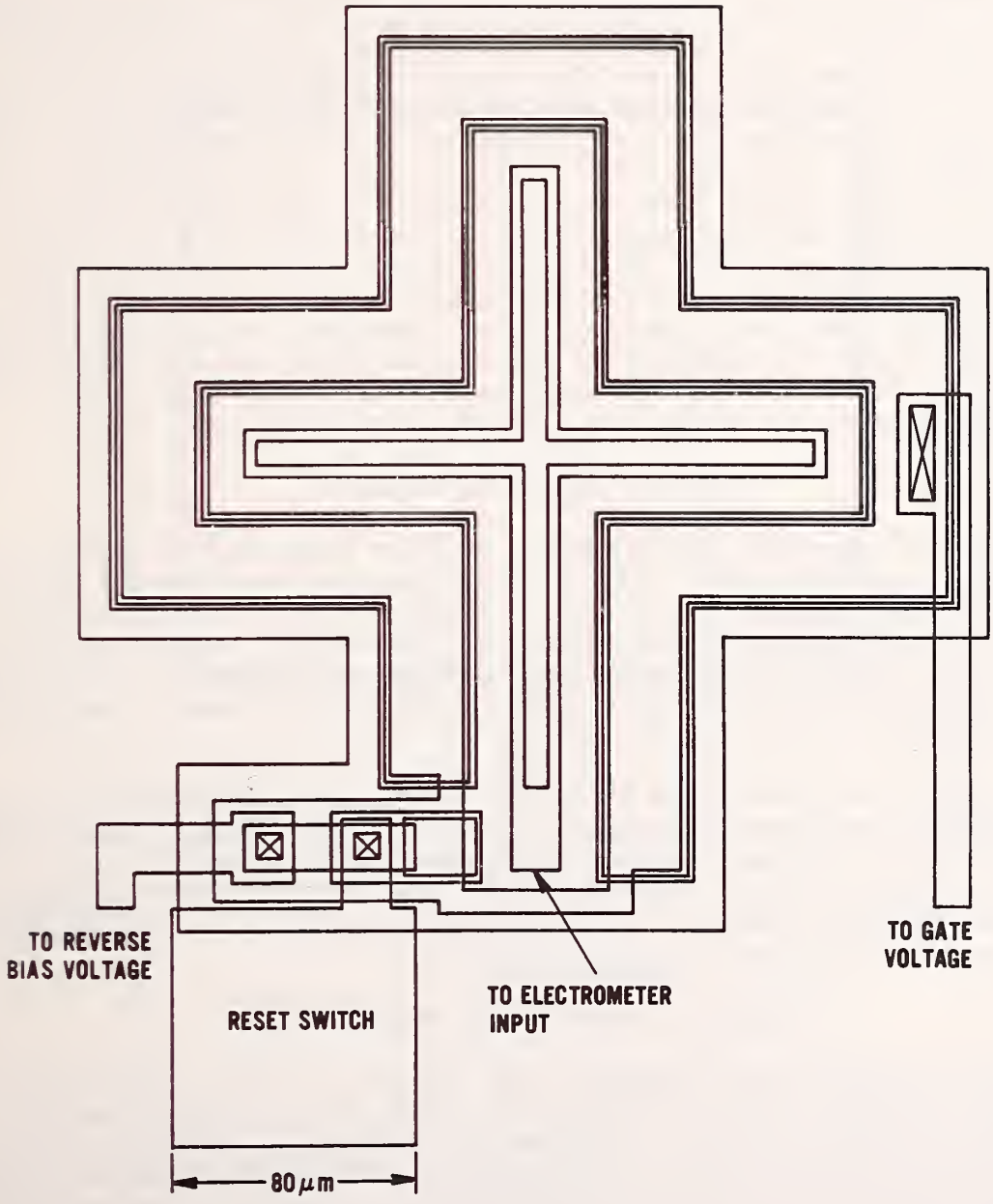

Figure 15. Outline drawing of the cross-shaped gated diode.

Inverted Rectangular Diode (fig. 16)

"Inverted" diodes are ones where the junction encloses an interior gate. The strategy here is to completely surround the gate with the metallurgical junction so that the field-induced junction does not intersect the surface or come into contact with a channel stop diffusion. In experiments on stand-alone diodes, soft breakdown leakage currents were found to interfere with accurate determination of the leakage currents in inversion. The interference will likely be greater for irradiated structures because surface state densities will be higher than we have encountered in experiments to date. The additional complexity of guarded structures is avoided at the expense, in this case, of higher levels of leakage at the outer perimeter of the metallurgical junction. Compared to guarded structures, the tradeoff may sometimes be an advantageous one depending upon the magnitude of the surface state density. Both options (guarding and inverting) may ultimately be necessary in the absence of knowledge about the amount and type of leakage expected.

4.3.2 MOSFET dc Profiler

As mentioned earlier, the MOSFET dc Profiler configuration suitable for probing a shallow layer utilizes a dual gate and source/drain tubs to achieve the necessary isolation for enhancement mode operation (fig. 10). A design for this structure is shown in figure 17. The split gate is biased high enough to invert the edges of the tub diffusion. The center profiling gate and the body contact to the tubs are used to perform the profiling.

An alternative approach is to retreat to the conventional profiler configuration and overcome the geometry difficulties by using implantation to obtain an extremely shallow source and drain. A design for such a device is shown in figure 18. Practical considerations for this device, including the avoidance of punch-through and contact to the implanted source and drain, have not been addressed.

4.3.3 Cross-Bridge Sheet Resistor

The Cross-Bridge Sheet Resistor (fig. 19) can be used to measure the sheet resistance and the linewidth for each of the various layers of interest in the process. Procedures for using this structure and calculating sheet resistance and linewidth are given in references [9] and [10]. This structure may be fabricated of any layer (including metal) to which electrical contact may be made simply by using the same design for the resistor region and adding a tub for isolation when necessary.

4.3.4 Contact Resistor

The Contact Resistor (fig. 20) can be used to measure the resistance, at a contact window, between any two layers which electrically contact each other. This structure is used to provide information on the quality of the electrical contact. Although no detailed study of this structure has

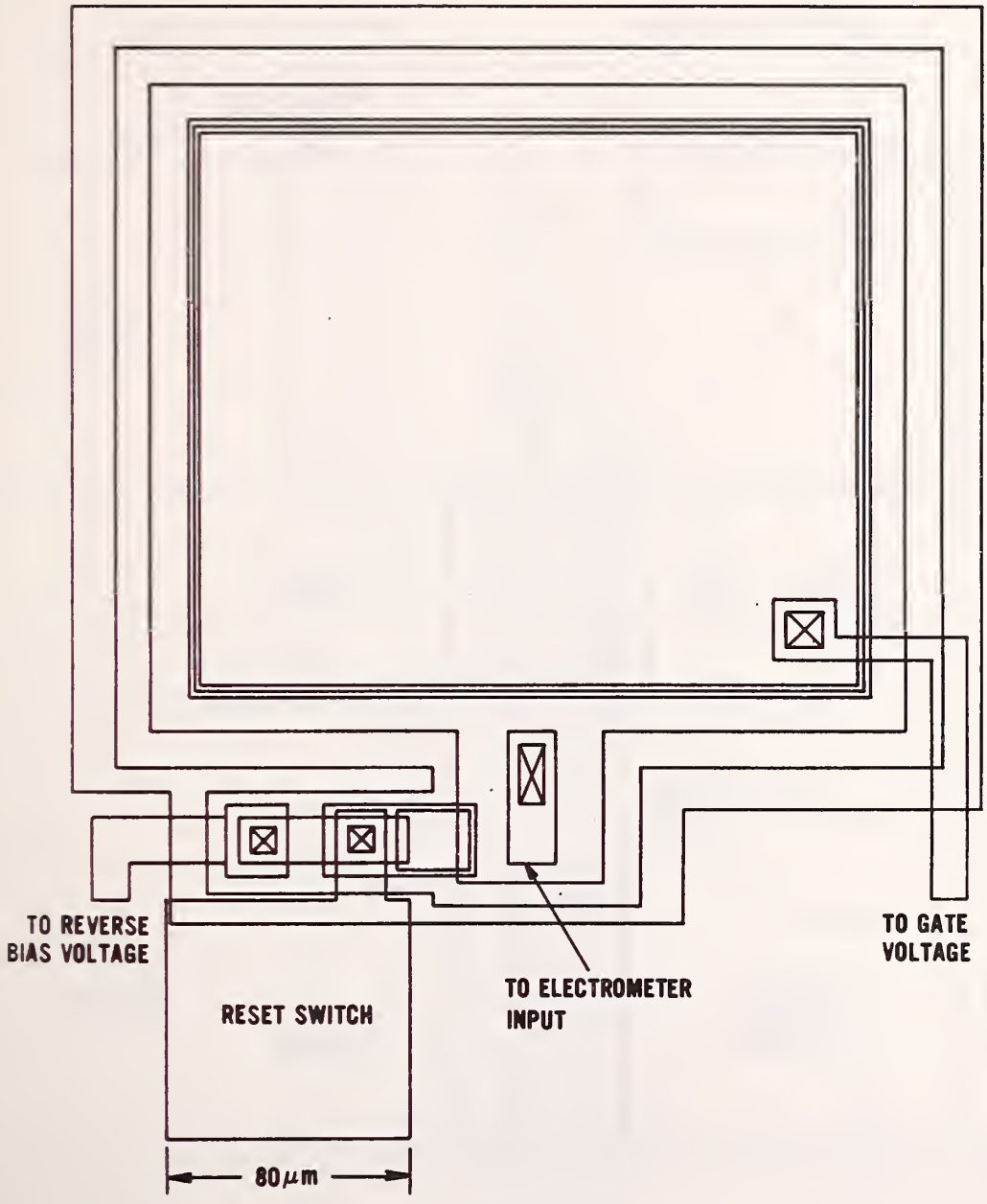

Figure 16. Outline drawing of the inverted rectangular gated diode.

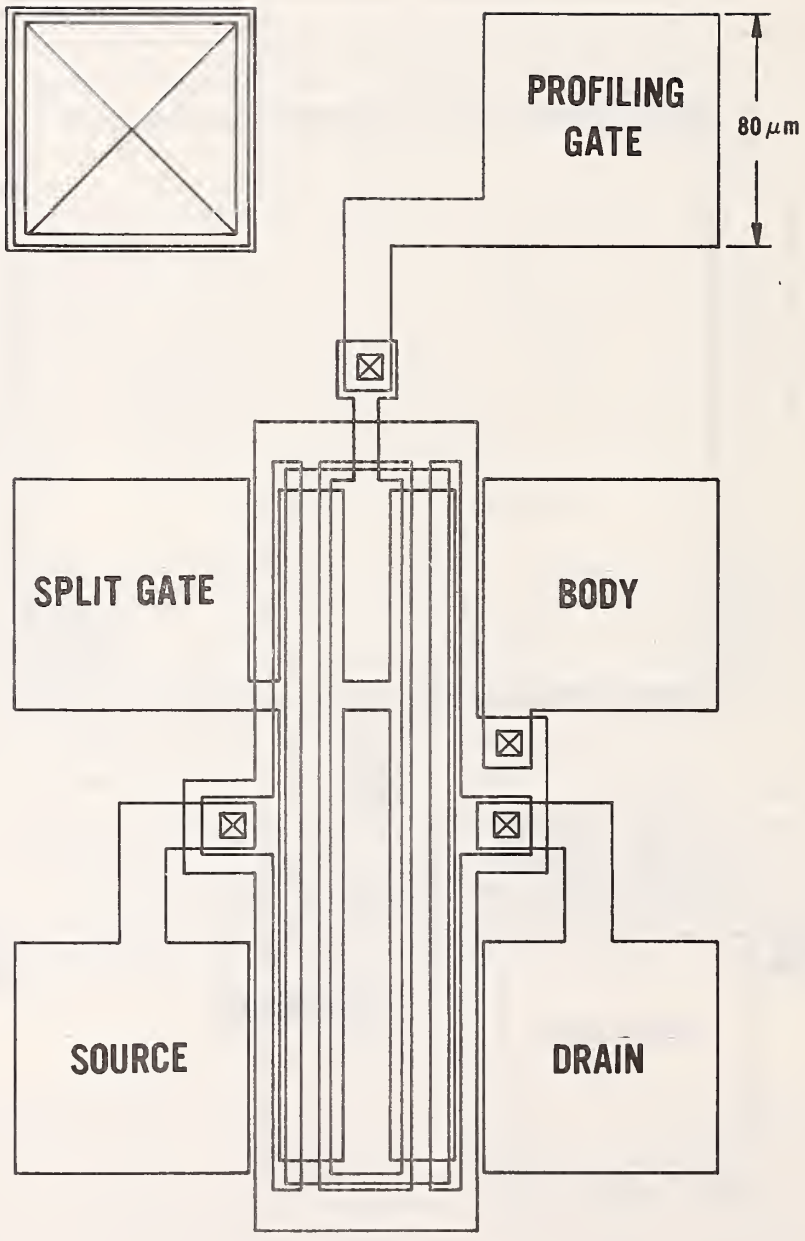

Figure 17. Outline drawing of the dual-gate MOSFET dc Profiler.

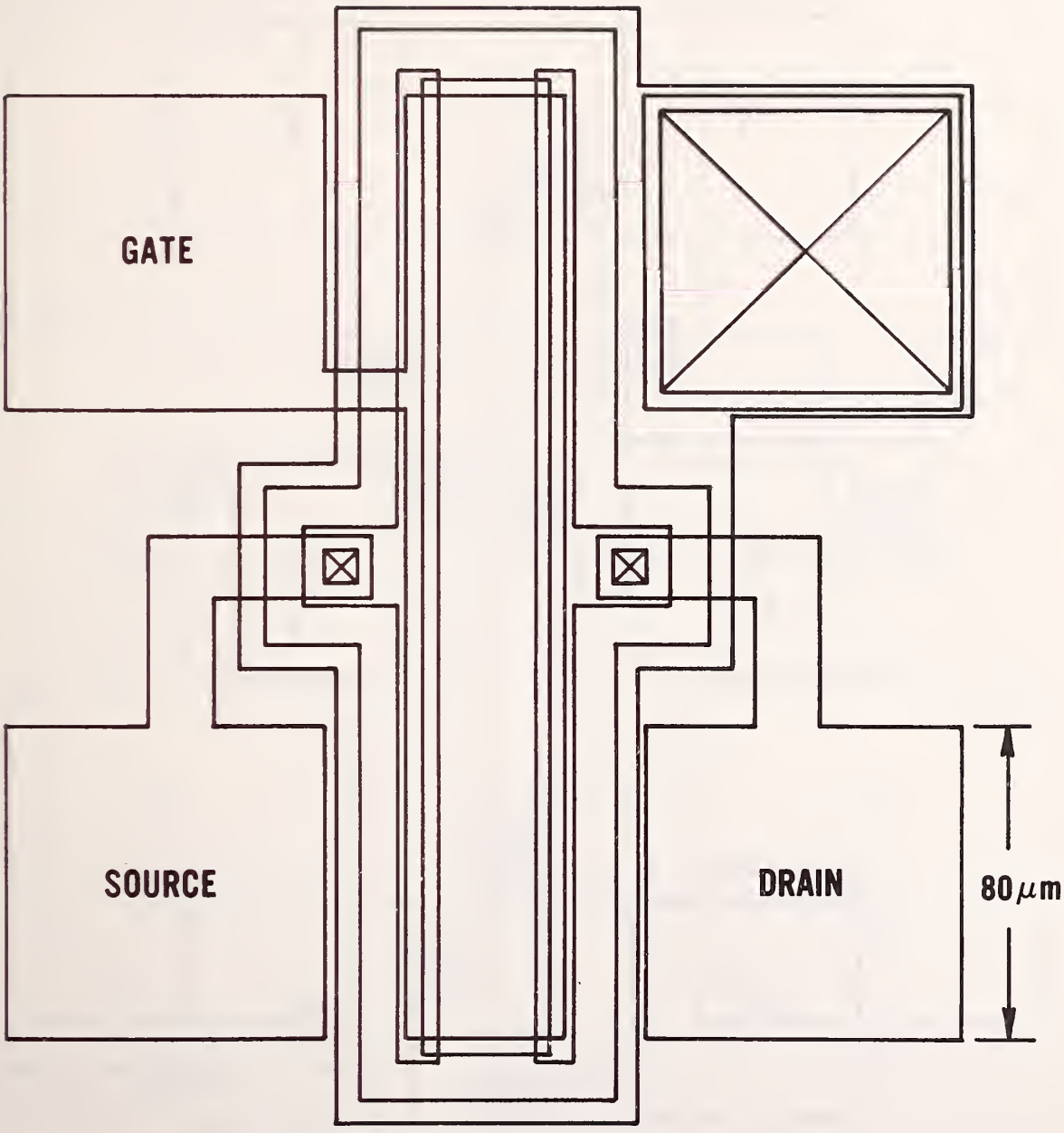

Figure 18. Outline drawing of the MOSFET dc Profiler using implanted source and drain.

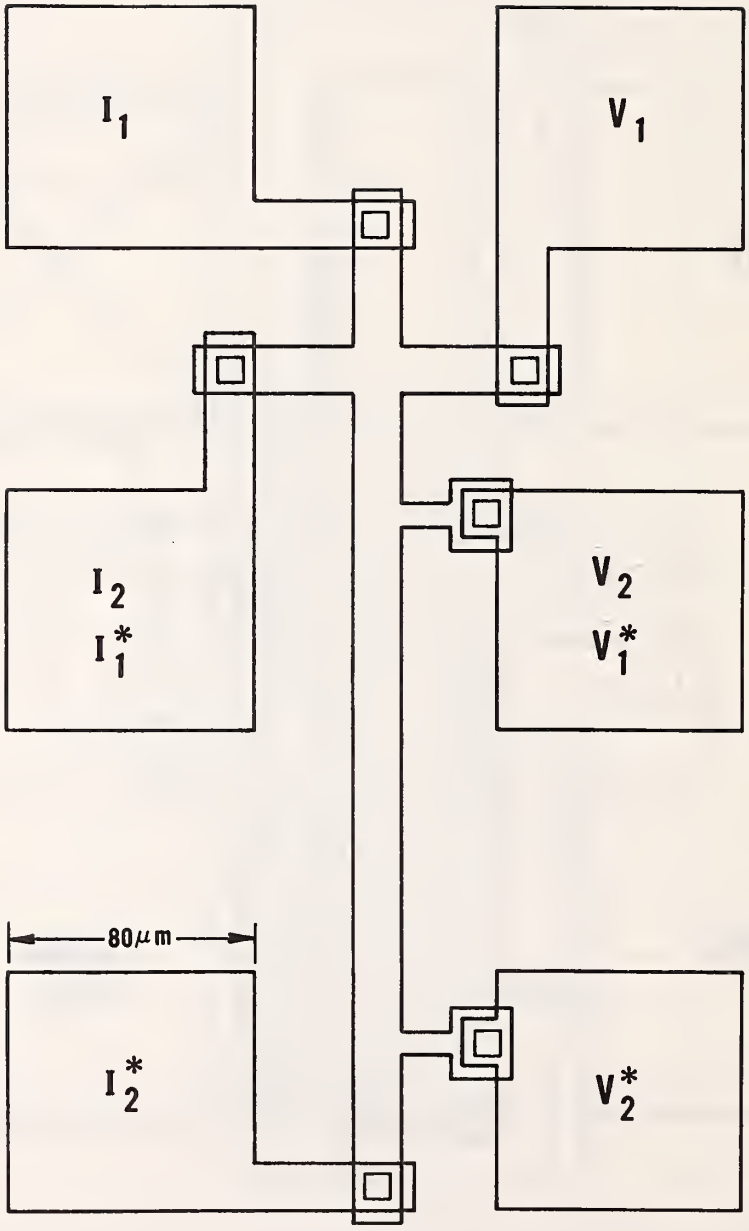

Figure 19. Outline drawing of the Cross-Bridge Sheet Resistor.

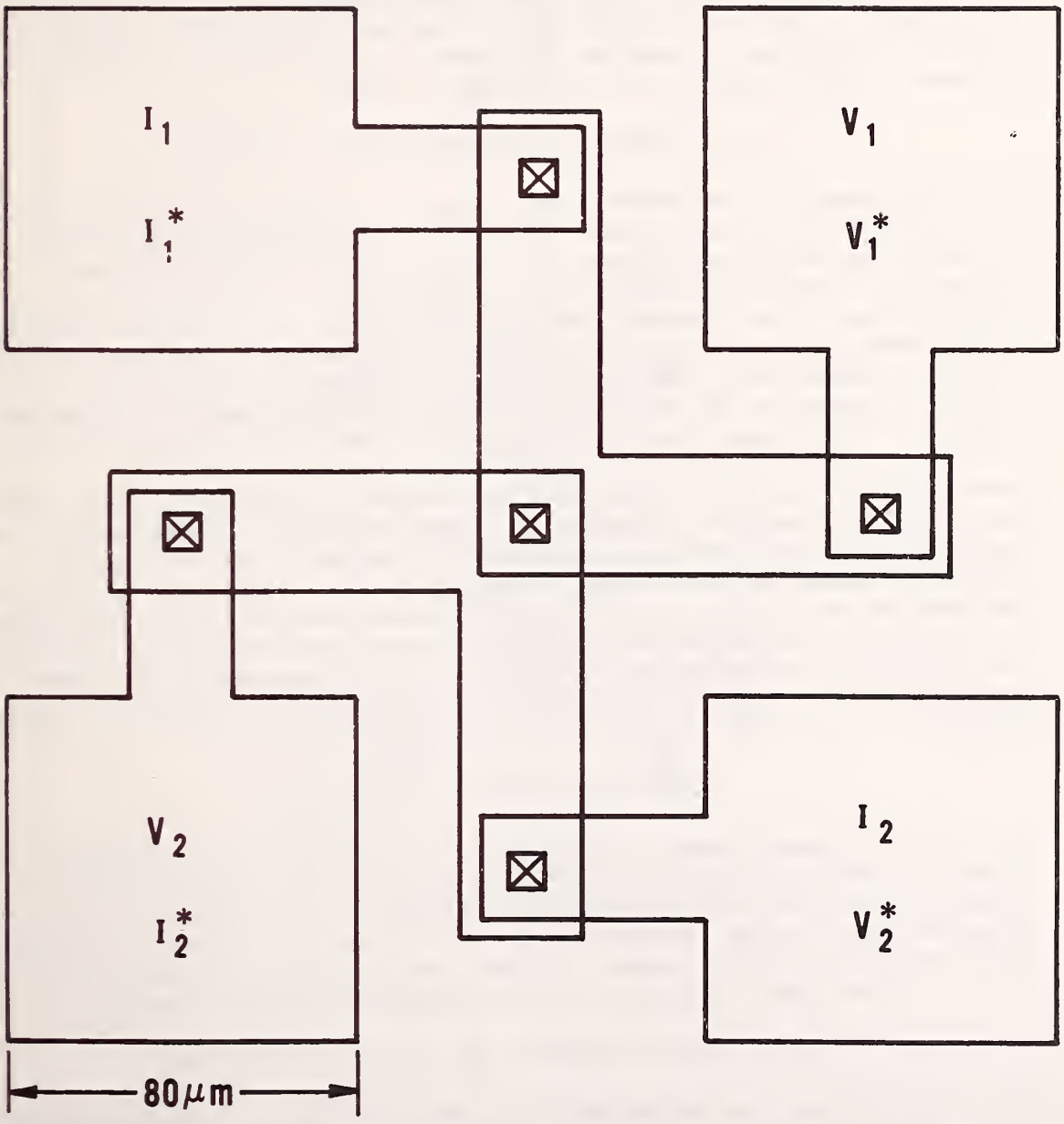

Figure 20. Outline drawing of the Contact Resistor.

been performed, it is useful for detecting gross contact faults which may lead to erroneous results from other test structures or from the CCD circuit itself. The structure is symmetrical and allows for a Kelvin measurement regardless of whether the chosen current path is linear or undergoes a right-angle turn at the contact window.

4.3.5 Electrical Alignment Test Structure

The potentiometric resistors which compose the Electrical Alignment Test Structure (fig. 21) are of two types [11]. The difference is in the detailed way the metal contacts the lower levels. If the contact window is covered by the metal, the structure is of the first type and the position of the contact window is critical. If the contact window is larger than the metal stripe which makes the contact, then the structure is of the second type and the position of the metal is critical. In both types, the position of the contact window or metal layer is determined relative to the lower level, which can be a doped layer or polysilicon.

Both types of electrical alignment structures are measured in the same way. The structure is analogous to a pair of linear potentiometers, one horizontal and one vertical, where the mid-point of the resistor is sensed by measuring the voltage imbalance between the center contact and the ends of the potentiometer when a constant current is passed through the resistor. The first configuration, which uses the contact window as the reference, is preferred. (NBS Special Publication 400-51, issued in April 1979, describes the electrical alignment test structure in greater detail.)

4.3.6 Surface Channel Detector

The Surface Channel Detector (fig. 22) is composed of interdigitated doped regions of opposite conductivity type to the substrate which therefore form *pn* junctions with the substrate. If a potential is applied between the two contact pads, the presence of a significant current implies either surface leakage or poor isolation of the dopant region, either of which may interfere with measurements on other devices.

4.3.7 Step Coverage and Isolation Structure

The Step Coverage and Isolation Structure (fig. 23) is a small version of a class of structures relating to random faults and statistical data acquisition devices which will be developed in a subsequent effort. Although the entire question of random faults has not been addressed in this year's program, this structure is included as a precursor to its class and because it may be helpful for detecting gross problems at metal-over-polysilicon and polysilicon-over-polysilicon steps. In addition, the structure may be used to obtain an estimate of the oxide strength at metal-polysilicon steps.

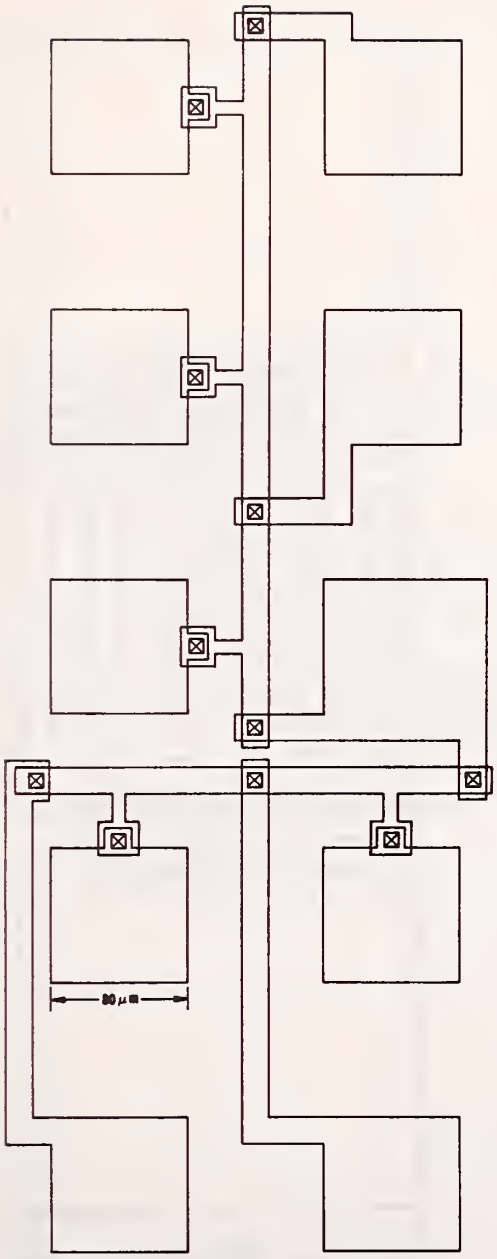

Figure 21. Outline drawing of the Electrical Alignment Test Structure.

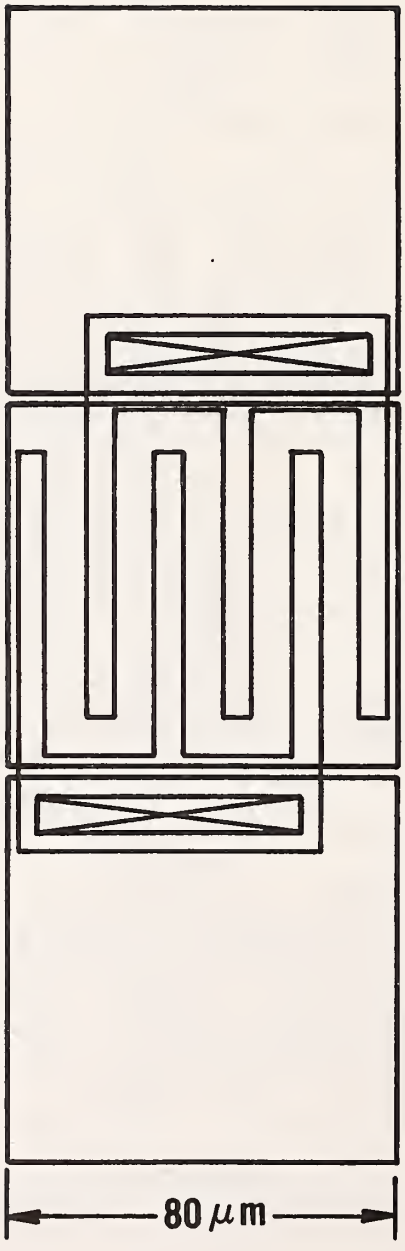

Figure 22. Outline drawing of the Inversion Layer Detector.

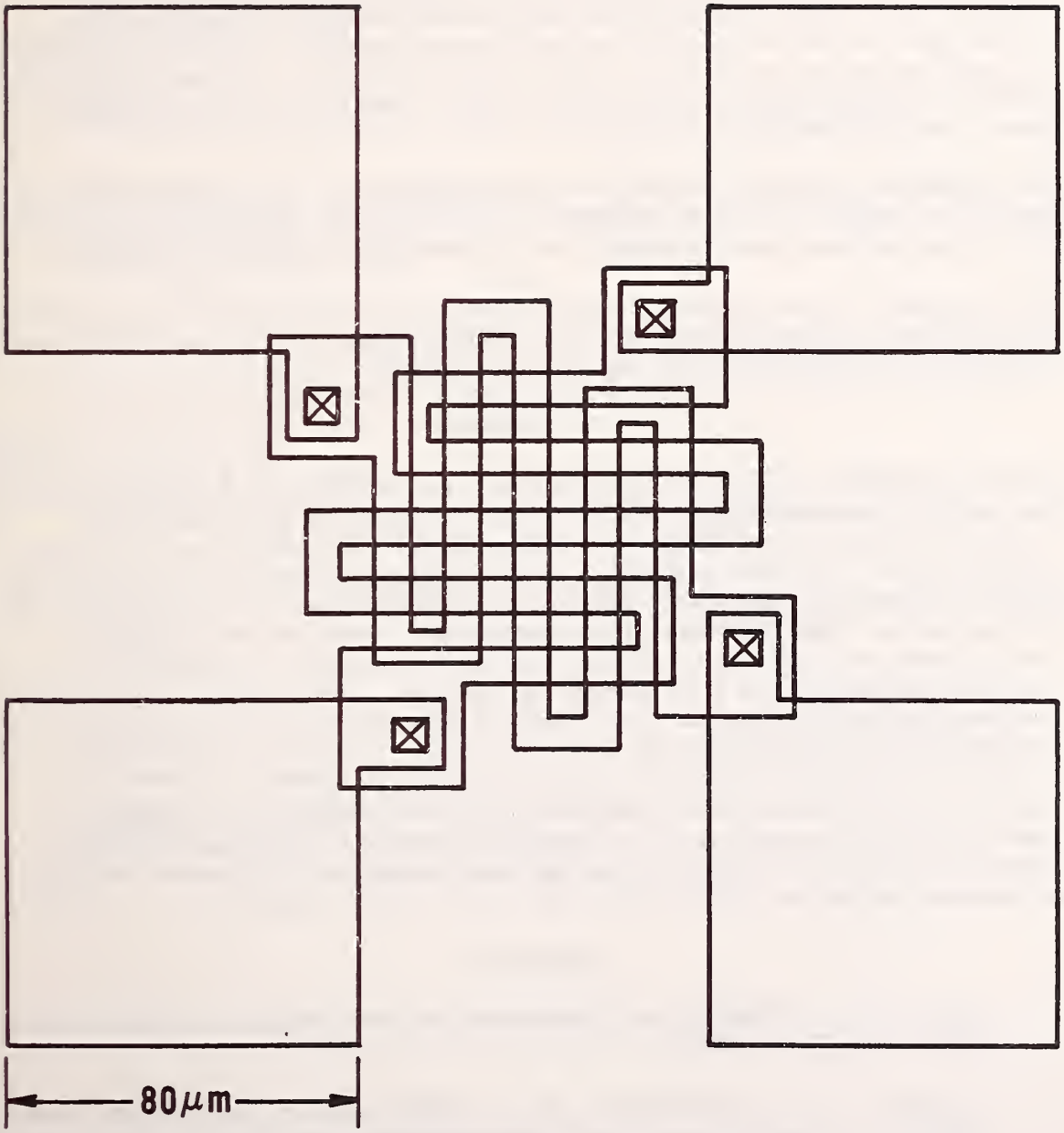

Figure 23. Outline drawing of the Step Coverage and Isolation Test Structure.

4.3.8 Other Test Structures

Also included among the parametric test structures are capacitors and transistors. The capacitors are for characterizing the various gate oxides and for use in supporting other measurements (such as the MOSFET dc Profiler which requires the gate oxide thickness). In addition, the capacitors are available for conventional capacitance-voltage measurements should these be necessary.

The transistors should include all combinations of gate material and gate and field oxides. Typical MOSFET transistor characteristics, such as threshold voltage, are desirable for process and materials evaluation.

The designs for the capacitors and transistors are expected to be those usually employed by the CCD vendors, and allowance will have to be made for bonding out for bias during irradiation.

5. Summary

A set of production-oriented parametric test structures has been proposed for use in the evaluation of the radiation-hardened processes for radiation-hardened CCD imagers. The proposed test structures specified in this report include advanced test structures which were developed during this program, improved versions of existing NBS test structures, and various other commonly used test structures. Some of the designs for test structures were modified for compatibility with the radiation-hardened processes and with radiation testing. Procedures are described for testing the test structures using high-speed computer-controlled data acquisition techniques.

Two of the test structures developed for this program, the Integrated Gated-Diode Electrometer and the MOSFET Profiler, represent new and unique test vehicles which allow the determination of relevant physical parameters which are difficult to obtain by other methods.

References

1. Grove, A. S., *Physics and Technology of Semiconductor Devices*, John Wiley (New York, 1967).

2. Thurber, W. R., and Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-4, NBS Special Publication 400-32 (April 1978).

3. Killiany, J. M., Radiation Effects on Silicon Charge-Coupled Devices, *IEEE Trans. Components, Hybrids, and Manu. Tech.* CHMT-1, 353 (1978).

4. Lonky, M. L., and Turley, A. P., Statistical Analysis of P+/N Junction Leakage Characteristics for Silicon Gate Processed Devices, *Electrochem. Soc. Ext. Abs.*, Abstract #138 (October 1975).

5. McCarthy, D., Buehler, M. G., Acevedo, J., Stamps, B., and Lonky, M. L., An Advanced Integrated Test Structure for High Speed Measurement of Generation Lifetime, *Electrochem. Soc. Ext. Abs.*, Abstract #183 (October 1978).

6. Buehler, M. G., Dopant Profiles Determined from Enhancement-Mode MOSFET dc Measurements, *Appl. Phys. Lett.* 31, 848 (1977).

7. Buehler, M. G., Limitations and Applications of the dc MOSFET Dopant Profile Method, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 241-252 (ECS, Princeton, 1978).

8. Buehler, M. G., Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-Pad Array Approach, presented at the Microelectronics Measurement Technology Seminar, San Jose, California, February, 1979 (to be published).

9. Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* 125, 650 (1978).

10. Buehler, M. G., and Thurber, W. R., An Experimental Study of Various Cross Sheet Resistor Test Structures, *J. Electrochem. Soc.* 125, 645 (1978).

11. Russell, T. J., Leedy, T. F., and Mattis, R. L., A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing, *Technical Digest*, International Electron Devices Meeting, Washington, D. C., December 5-7, 1977, pp. 7A-7F.

NBS-114A (REV. 9-78)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 79-1744	3. Recipient's Accession No.

4 TITLE AND SUBTITLE

The Development of Test Structures for Characterization of the Fabrication and Performance of Radiation-Hardened CCD Imagers

5. Publication Date

May 1979

6. Performing Organization Code

7. AUTHOR(S)

G. F. Carver and M. G. Buehler

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, DC 20234

10. Project/Task/Work Unit No.

11. Contract/Grant No.

DL-H-139485

12. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS *(Street, City, State, ZIP)*

The Charles Stark Draper Laboratory, Inc.
555 Technology Square
Cambridge, MA 02139

13. Type of Report & Period Covered

Final - 3/1/78 to 11/30/78

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

[ ] Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

A set of production-oriented parametric test structures has been proposed for use in the evaluation of the radiation-hardened processes for radiation-hardened CCD imagers. The proposed test structures specified in this report include advanced test structures which were developed during this program, improved versions of existing NBS test structures, and various other commonly used test structures. Some of the designs for test structures were modified for compatibility with the radiation-hardened processes and with radiation testing. Procedures are described for testing the test structures using high-speed computer-controlled data acquisition techniques.

Two of the test structures developed for this program represent new and unique test vehicles which allow the determination of relevant physical parameters which are difficult to obtain by other methods.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

CCD; electrical test structure; gated diode; generation lifetime; integrated gated-diode electrometer; integrated test structure; leakage current; MOSFET dc profiler; surface recombination.

18. AVAILABILITY [X] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[ ] Order From Sup. of Doc., U.S. Government Printing Office, Washington, DC 20402, SD Stock No. SN003-003-

[X] Order From National Technical Information Service (NTIS), Springfield, VA. 22161

19. SECURITY CLASS (THIS REPORT)

UNCLASSIFIED

20. SECURITY CLASS (THIS PAGE)

UNCLASSIFIED

21. NO. OF PRINTED PAGES

53

22. Price

$5.25

USCOMM-DC