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# Semiconductor Technology Program Progress Briefs

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SEMICONDUCTOR TECHNOLOGY PROGRAM

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ABSTRACT — This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: reverse-bias second breakdown, an integrated gated-diode electrometer, random fault measurements, pattern generator positional accuracy, intrachip linewidth variation, transient upset in TTL circuits, photoresist sensitometry, optical linewidth measurements, spreading resistance profiling, model spreading resistance data, silicon resistivity SRMs, and sheet resistance measurements. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

KEY WORDS: Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

## Preface

This report covers results of work during the forty-third quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Distributed Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Army Electronics R&D Command; 8. The Air Force Avionics Laboratory; 9. The Naval Material Command; 10. The Naval Weapons Support Center; and 11. The Solar Energy Research Institute.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

## Reverse-Bias Second Breakdown

A qualitative model of transistor turnoff switching behavior has been developed. Typically, the voltage storage time associated with turnoff is defined as the interval between the initiation of turnoff (base current reversal) and the time at which the collector voltage reaches 10% of its peak (usually clamped) value. However, there is a significant interval between the time that the device voltage begins to rise above its saturation voltage (leaves saturation and enters quasi-saturation) and the time it reaches 10% of its peak value. This is because the collector region of a typical modern power transistor is long and lightly doped. Significant power is dissipated during this interval because the voltage is rising and the current is constant at its peak value. Depending upon the operating conditions, 10 to 30% of the total energy dissipated during one turnoff cycle can be dissipated before the voltage reaches 10% of its peak value. To account for this region of high energy dissipation, another time interval must be defined. The voltage storage time then becomes the time interval from the initiation of turnoff until the time at which the device leaves saturation. The other time interval, as yet unnamed, which accounts for quasi-saturation, extends from the time the transistor leaves saturation until the time at which the collector voltage reaches 10% of its peak value. Current crowding occurs only in this latter time interval. Consequently, the voltage at which second breakdown occurs is most sensitive to the magnitude of the reverse base current during this time interval and is relatively insensitive to the magnitude during the voltage storage time as newly defined above. Preliminary experiments confirm that the reverse base current magnitude is not important as far as the second breakdown voltage is concerned until the device reaches its quasi-saturation region. [Sponsor: 2]

(D. L. Blackburn, x3621)

## Integrated Gated-Diode Electrometer

Continuing studies of the integrated gated-diode electrometer were carried out. Experimental measurements of the interactions between the designed elements of the circuit and the parasitic circuit elements are being compared with computer circuit simulations.* Preliminary conclusions reinforce confidence both in the analytical model for the equivalent circuit for this integrated test structure and in the methods developed to measure the structure. Insights have been obtained which provide alternative methods to overcome limitations of the device. For example, it was verified experimentally that a large fixed capacitor, connected in parallel with the diode junction, dominates both the junction capacitance and parallel parasitic capacitances so that only the added fixed capacitance need be considered when calculating the leakage current. Measurements of leakage current with and without the capacitor give the same result, although the presence of the additional large capacitance substantially decreases the output voltage decay rate. Under certain circumstances, the tradeoff may be desirable if it results in a more accurate measurement by reducing the effects of parasitic capacitance.

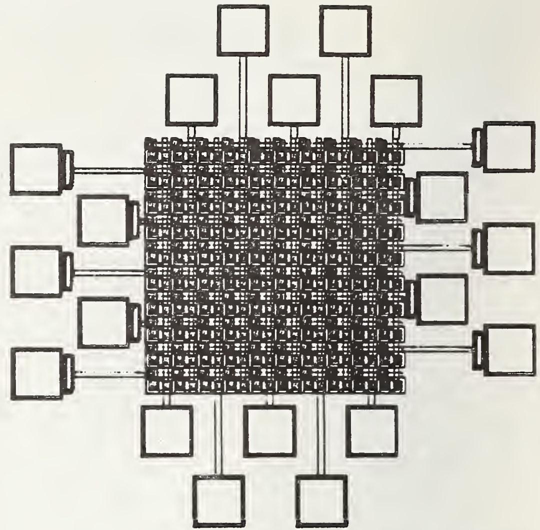
As an extension of the utility of the integrated test structure, pulsed capacitance measurements of the charge build-

*Design and fabrication of the test devices used in the experiments and the computer simulations were carried out by the Westinghouse Advanced Technology Laboratories, Baltimore, MD.

up in the gate inversion layer are being investigated. In these measurements, the diode gate is used as an MOS capacitor, and the diode junction and the electrometer are employed as a charge-sensing amplifier. Unlike conventional capacitor transient measurements where capacitance is measured as a function of time following a voltage pulse which biases the capacitor into deep depletion, in this procedure the charge buildup in the gate inversion layer is measured as a function of time. Evaluation of the experimental results awaits completion of an analytical description of the time rate-of-increase of the inversion layer charge density, but it is anticipated that this technique will complement the gated-diode reverse-bias voltage decay measurement by providing a second method for measurement of bulk lifetime. An extension of this technique would use the integrated test structure to measure recovery time or storage time in a dynamic memory cell. In this application, the diode gate functions as the transfer electrode, and the diode junction and electrometer operate as a charge integrator, a configuration analogous to the charge-sensing output amplifier frequently used in CCDs. [Sponsors: 1,2,6] (G. P. Carver, x3541)

## Random Fault Measurements

Initial test results have demonstrated that the location of a fault can be identified from electrical measurements on memory-type MOSFET array test structures. In some cases, fault type has also been identified electrically from the data taken to date. Four such structures appear on test pattern NBS-16. This pattern is being used to develop process assessment methods to evaluate the electrical performance, radiation tolerance, and yield of radiation-hardened, silicon-gate CMOS/SOS LSI circuits. Each random-fault test structure consists of a 10 by 10 array of *n*- or *p*-channel MOSFETs, each with its gate connected to its drain. The sources are connected in



***Check plot of a typical p-channel MOSFET array found on test pattern NBS-16. The probe pads around the periphery of the array are 80 μm by 80 μm.***

columns and the gates and drains are connected in rows, as illustrated in the accompanying check plot of a typical *p*-channel MOSFET array. Each device is electrically isolated from its neighbors (except for the common row and column connections). Threshold voltage, breakdown voltage, and source-to-drain leakage current can be individually measured for each MOSFET on the array by addressing the appropriate row and column probe pads. Further analysis is continuing in order to establish improved criteria for identifying fault types from electrical data. [Sponsor: 8]

(L. W. Linholm, x3541)

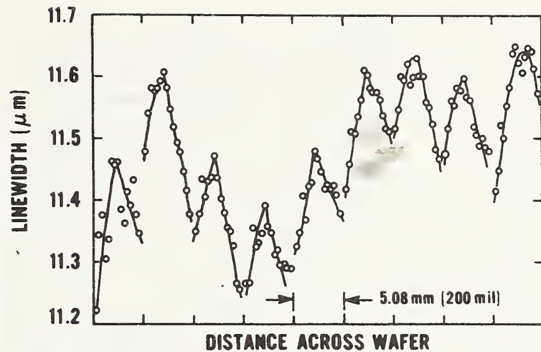
## Pattern Generator Positional Accuracy

The metal-to-doped region potentiometric electrical alignment test structures on test pattern NBS-15 were used to evaluate the positional accuracy of a typical computer-controlled pattern generator. A composite 10X reticle was made up by flashing the rectangles from the mask levels for both the metal areas (mask level 3) and the doped regions (mask level 1) on the same plate. This reti-

cle was stepped and repeated to construct a 1X working photomask. Two wafers were fabricated by contact printing the pattern on an aluminum film evaporated on an oxidized silicon substrate and defining the pattern by wet chemical etching. The misalignment was measured at 266 locations on each wafer. The mean value of the measured misalignment (35 nm) is indicative of the positional accuracy of the pattern generator. This indicates that rectangles could be positioned within 350 nm on the 10X reticle, well within the stated accuracy of the pattern generator employed. Variability in the alignment may be introduced by the processing of the 10X reticle, the 1X photomask, and the wafers. The average of the sample standard deviations was 49 nm, which suggests that variability from processing exceeds the after-reduction positioning error of the pattern generator. [Sponsor: 1]
(T. J. Russell, x3541)

## Intrachip Linewidth Variation

Additional measurements of periodic and random variations in linewidth over an integrated circuit wafer were made using test pattern NBS-21. This single-level pattern consists of an 8 by 15 array of identical cross-bridge sheet resistors with a drawn linewidth of 0.600 mils (15.24 μm). The array fits within a square 200 mils (5.08 mm) on a side and is repeated across the mask on 200-mil centers each way. The pattern is fabricated by delineating (with the use of contact printing and wet chemical etching techniques) the cross-bridge resistors in an 800-nm thick aluminum film evaporated on an oxidized silicon wafer. Each wafer contains 53 arrays. All the arrays on a given wafer exhibited a similar pattern of linewidth variation which was on the order of 0.2 μm for the smallest to the largest value, as illustrated by the example of data from one row in the arrays across the diameter of a wafer shown in the accompanying figure. Similar periodic variations have been measured on other wafers from various lots, all fabricated with the same photomask. These periodic variations can be attributed to the system used to fabricate the photomask. In addition, variations over the wafer were observed when the same structure in each array was measured. These variations, which are also evident in the example shown in the figure, can be attributed to the photolithography associated with the contact printing or to variations in etching the pattern or to both. The range in measured linewidth across the entire wafer was typically about 0.5 μm. [Sponsors: 1,2] L. W. Linholm, x3541)




*Linewidth variations in one row of the nine arrays across the diameter of a wafer as measured by the cross-bridge structures of test pattern NBS-21.*

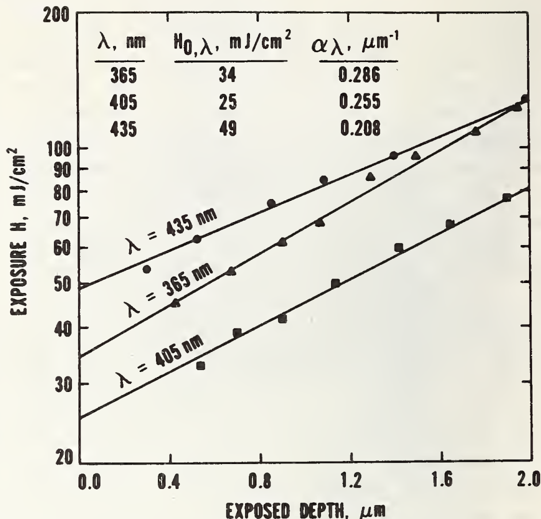
## Transient Upset in TTL Circuits

During an on-going study of transient upset in digital integrated circuits, being conducted in collaboration with the Naval Research Laboratory, a temperature dependence of the upset threshold was observed in standard transistor-transistor logic (TTL) circuits. Preliminary results indicate that the threshold increases with temperature over the range from 20 to 150°C. Other workers addressing this problem have disagreed in predictions of the direction of the temperature dependence. Based on the limited amount of data currently available, it has been hypothesized that upset is due to photocurrent generated in the depletion layer of the

collector-substrate junction. The decrease in sensitivity to upset with increasing temperature in a standard gold-doped TTL gate would result from the reduction in thickness of the depletion layer as the resistivity of the gold-doped material decreases. The capacitance of the depletion layer in such a gate was measured and was found to increase with increasing temperature, which supports this hypothesis. Further support for the hypothesis is given by the fact that in Schottky-clamped versions of the same gate (74S series), the upset sensitivity and the junction capacitance do not depend significantly on temperature. The Schottky-clamped devices are not gold-doped. [Sponsor: 5]
(T. F. Leedy, x3621)

## Photoresist Sensitometry

A more rapid and precise technique than direct measurement of photoresist linewidth variations as a function of exposure has been found for measuring exposure characteristics of photoresist. The linewidth measurement technique suffered both from the inability to locate the line edges accurately and from large variability in the resulting data. The current technique is based on the property that the depth of photoresist dissolved during a controlled amount of development after exposure to a known amount of monochromatic radiation corresponds to a specific fraction of photolysis. The depth of the exposed pattern is measured with a surface profilometer; plots of log exposure against developed depth of a positive resist exposed to radiation of wavelength 365, 405, or 436 nm (the three strong lines of high pressure, short arc mercury lamps typically used in microelectronic patterning) show a linear relationship. Examples of these plots are given in the accompanying figure. The linear behavior is predicted from theoretical modeling of resist exposure performed and reported previously. The development of this technique represents an initial step in the complete characterization of resist exposure. Each relation of monochromatic exposure against depth constitutes an element in the additive effect of these exposures when a resist is simultaneously exposed to the complete radiation spectrum of the mercury lamp. One unexpected result was obtained: the 405-nm radiation appears to be more effective than the 365-nm radiation despite the greater absorbance of the resist at 365 nm. In general, it had been assumed that radiation of the wavelength for which the resist exhibits the greatest absorbance has the greatest effect on the resist exposure. The 436-nm radiation, which is least sensitive, also has the lowest absorbance, and so follows the expected trend. Also, an aging effect, a decrease in resist sensitivity with time, was observed; this behavior suggests that this method of resist exposure characterization may provide a tool for assessing resist shelf life and aging effects. [Sponsor: 1]
(D. B. Novotny, x3621)




*Semilog plot of photoresist exposure, H, as a function of exposed depth, d, for a positive resist exposed to monochromatic radiation of wavelength λ. The data follow the relationship*

$$\log H = \log H_{0,\lambda} + \alpha_\lambda d \ .$$

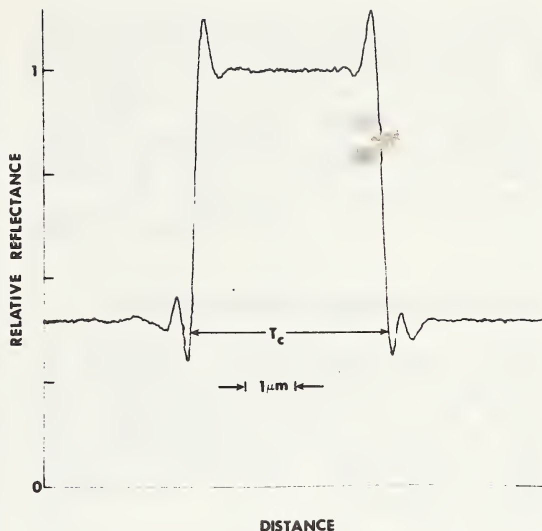
*The quantity H is proportional to time of exposure to a constant flux of radiation.*

## Optical Linewidth Measurements

The prototype system for optical linewidth measurements on wafers in reflected light was completed. Linewidths down to 0.5 μm can be measured with a sensitivity of 0.01 μm. For measurements of features with steep edges in thin layers, the capability of the reflected light system is comparable to that of the scanning photometric microscope developed earlier for measurements on photomasks in transmitted light. However, the two systems differ significantly. Both systems operate with Kohler illumination and modified bright field illumination (the illuminating numerical aperture must be one-fourth or less of that of the imaging objective for low contrast materials), but the reflected light system uses a 0.5-W krypton laser source and a more sensitive photomultiplier-detector system. In addition, the alignment requirements for the optics of the reflected light system, which illuminate a much smaller field of view, are more stringent than those for the optics of the transmitted light system. All of these conditions result from the need for illumination with very narrow spectral bandwidth which is dictated by the strong wavelength dependence of both the reflectance and optical phase difference associated with thin films. The reflected-light system produces image profiles like that shown in the accompanying figure.* From such an image profile, the linewidth is determined using the coherent optical threshold $T_C$ with appropriate corrections for the reflectances of the materials and the optical path difference which occurs at the edge on reflection. At the present time, both the reflected light and transmitted light systems are limited to films less than 400 nm thick. For thicker layers the edge detection equations are no longer valid and determination of best focus is ambiguous. Research is underway to develop accurate edge detection and focusing procedures for thick layers. [Sponsors: 1,2]

(D. Nyyssonen, x3621)

*To obtain this feature, the NBS linewidth calibration pattern (NBS 77) was contact printed from an anti-reflection chromium photomask and plasma etched. The wafer pattern contains lines as narrow as 0.55 μm. (Y. M. Liu, x3541)



*Line image profile of a 3.9-μm line etched in a 150-nm thick layer of silicon dioxide on a silicon wafer.*

## Spreading Resistance Profiling

A continuum formulation of spreading resistance correction factors was obtained by deriving a differential equation for the kernel of the correction factor integral in the limit as the layer thickness approaches zero. This differential equation is nonlinear and inhomogeneous, but, because it is of the Riccati type, it can be transformed into a linear, second-order equation which can be solved analytically in several cases. The continuum form of the correction factor was compared with the correction factor generated from the multilayer version of the Laplace equation description of spreading resistance for the case of a specimen with exponentially varying resistivity. The difference between the results obtained from the two forms depends on the exponential constant, the total thickness of the structure, and (most importantly) the number of layers used in the discrete form.

Typically, for the case of 11 layers, the discrete form yields a factor about one-third that yielded by the continuum form, but for the case of 201 layers the difference is only about 6%. These differences represent a fundamental limitation to the accuracy of the multilayer correction factor. [Sponsor: 1]
(J. H. Albers, x3625)

## Model Spreading Resistance Data

Studies were made of model spreading resistance data* for deep diffusions (up to 90 μm). For diffusions deeper than about 5 μm, the simple relationship between spreading resistance, $R_{sp}(x)$, and incremental sheet resistance, $R_s(x)$:

$$R_{sp}(x) = \frac{1}{\pi} R_s(x) \ln \frac{s}{a} ,$$

where s is the probe spacing and a is the effective contact radius, is no longer valid. It is found that, for all diffused layers investigated, the spreading resistance is approximately linear in ln s with a slope which is approximately proportional to the sheet resistance. This result would indicate that, for diffusions, probe spacing experiments could be safely interpreted in terms of a sheet resistance, even though the interpretation of the intercept as being related to the probe radius holds only for uniform layers and shallow diffusions. [Sponsor: 1]
(J. H. Albers, x3625)

## Silicon Resistivity SRMs

Twenty sets of SRM 1522, Silicon Power Device Level Resistivity Standard, have been fabricated and individually measured and certified. This new standard reference material is comprised of three 51-mm diameter slices of neutron transmutation doped (*n*-type) silicon with nominal resistivities (at room temperature) of 25, 75, and 180 Ω•cm. Each slice is nominally 25 mils (0.64 mm) thick. A two-operator two-instrument experiment was performed on five specimens from each crystal to estimate the precision of the certification measurements. Results of the experiment give estimates of the 95% confidence interval about the certified values as follows: ±0.2, ±0.4, and ±0.6% for the 25-, 75-, and 180-Ω•cm specimens, respectively. [Sponsor: 2] (J. R. Ehrstein, x3625)

## Sheet Resistance Measurements

Results of an interlaboratory experiment on the measurement of the sheet resistance of thin silicon layers by the four-probe method were analyzed. The experiment was coordinated by NBS for ASTM Committee F-1 on Electronics. It was conducted to evaluate the precision to be expected when ASTM Test Method F 374, Sheet Resistance of Silicon Layers, is used for the measurement of layers less than 3 μm thick. The procedure requires the use of a probe assembly with four blunt probe tips, terminating either in a hemisphere with a radius between 100 and 250 μm or in a circular truncation of a cone with a circle diameter between 100 and 250 μm. A probe force between 0.30 and 0.80 N (31 and 82 gf) is required for either configuration of probe tips. Six types of implanted layers and two types of epitaxial layers were used as test specimens in the experiment. Layer thicknesses were between 0.2 and 1.5 μm, and layer sheet resistance values were between 200 and 6000 Ω/□. The analysis, which accounted for laboratory-to-laboratory differences, run-to-run differences within a given laboratory, and differences in the six measurements on each specimen in any run, indicated that overall precision generally degraded with increasing specimen sheet resistance. The precision can be expressed in terms of the reproducibility interval for the average of six measurements on a specimen, the reproducibility interval being the 95% confidence interval for the difference in averages of specimen sheet resistance

*An annotated computer program to calculate model spreading resistance data is available on request. The program is written in double-precision UNIVAC FORTRAN V.

measured by two different laboratories. A conservative estimate for this reproducibility interval, which covers all specimens tested, is ±10% of the average sheet resistance value. [Sponsor: 2]
(J. R. Ehrstein, x3625, and J. Orban*)

## New Topics . . .

Applications of Neutron Transmutation Doped Silicon — A survey is being undertaken to determine the technical impediments to more effective utilization of NTD silicon for thyristor production. During this period, discussions with several industrial users of NTD silicon were completed to determine present areas of concern in NTD usage and to assess the potential for application of NTD silicon in other high power devices. In addition, groups involved in silicon materials research were also contacted. Additional information from individuals and organizations interested in this topic is welcomed. [Sponsor: 3] (D. R. Myers, x3625)

Gallium Arsenide Characterization — Evaluation of improved practical methods for characterizing device quality gallium arsenide substrates and epitaxial layers was initiated. Initial activity is directed toward extension to gallium arsenide of measurement techniques for silicon characterization. These include capacitance-voltage profiling, resistivity and Hall measurements on van der Pauw specimens, deep level transient spectroscopy (DLTS), and spreading resistance measurements. In addition, photo-DLTS and optical absorption measurements are being explored for applicability to characterization of semi-insulating gallium arsenide. [Sponsor: 7] (A. C. Seabaugh and R. Y. Koyama, x3625)

## Work in Progress . . .

An improved pattern for linewidth calibration artifacts has been designed. The improvements are based on results from the 10-laboratory evaluation of procedures for optical measurement of linewidths in the 0.5- to 10-µm range on chromium photomasks with transmitted light. Additional elements are included in the artifact to enable the user to check for lead-screw errors in filar and image-shearing microscope eyepieces. Several minor design changes were made to reduce confusion in locating and identifying each measurement element and to facilitate distinguishing the multiple lines in line-spacing measurements with image-shearing eyepieces. Procurement of anti-reflective chromium and iron-oxide artifacts with the improved pattern was initiated. [Sponsors: 1,2] (J. M. Jerke, x3621)

Wafer maps of the forward voltage of power rectifiers at low injection levels were previously found to be correlated with the reverse leakage current; regions of high forward drop corresponded to regions of low reverse leakage current. However, at values of forward current exceeding the high injection threshold, the correlation with reverse leakage is found to disappear abruptly. This transition is related to the dependence of the forward drop on the carrier lifetime. At low injection, the minority carrier lifetime dominates, whereas at high injection the forward drop depends on the high level lifetime. [Sponsor: 3] (R. Y. Koyama, x3625)

*NBS-NRC Postdoctoral Research Associate, NBS Statistical Engineering Division.

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*Reports of Contract Research.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include studies of: reverse-bias second breakdown, an integrated gated-diode electrometer, random fault measurements, pattern generator positional accuracy, intrachip linewidth variation, transient upset in TTL circuits, photoresist sensitometry, optical linewidth measurements, spreading resistance profiling, model spreading resistance data, silicon resistivity SRMs, and sheet resistance measurements. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*
Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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