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Semiconductor Technology Program Progress Briefs

W. Murray Bullis, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
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SEMICONDUCTOR TECHNOLOGY PROGRAM

TABLE OF CONTENTS

ABSTRACT — This report provides information on the current status of NBS work in measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: analysis of X-levels in indium-doped silicon; evaluation of an electrical alignment test structure; correlations of gold density with leakage current in silicon; initial application of resonance ionization spectroscopy; calibration of second-generation line-width measurement artifacts; dopant profiling by dc measurements on MOSFETs; observation of an isotope shift in the sulfur deep level in silicon; development of a nondestructive test for second breakdown; analysis of scanning acoustic microscopy; and the third pacemaker workshop. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of current publications, publications in preparation, and scheduled talks are also included.

KEY WORDS — Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

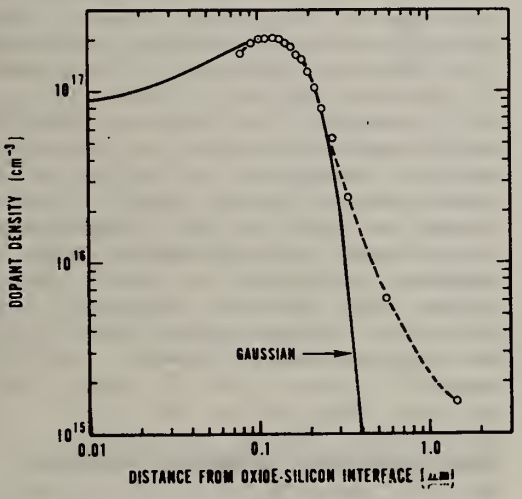
Preface

This report covers results of work during the thirty-eighth quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified by a superscript numeral at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; and 6. The Goddard Space Flight Center.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information and a list of past publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D. C. 20234, telephone: (301) 921-3786.

Dopant Profiles from dc Measurements

Dopant profiles can be determined from measurement of the capacitance of an MOS capacitor, junction diode, or Schottky diode as a function of voltage. These measurements require high frequency signals; they cannot be performed on high-speed test equipment. A method was developed to determine profiles from dc measurements; it was described in the 15 December 1977 issue of *Applied Physics Letters*. The method, which employs an enhancement-mode MOSFET, has been applied to measurement of boron and phosphorus implants in silicon as well as uniformly doped silicon. Impurity redistribution due to thermal oxidation can be distinctly observed. Profiles obtained by this method can be distorted by high channel conductance which causes an apparent shift of the profile toward smaller depths and higher dopant density values. This distortion can be eliminated by extrapolating the data to the case of zero channel conductance. When this is done, dopant densities measured by this method on specimens uniformly doped to densities about 10^{16} cm^{-3} agreed within two percent with values measured by the capacitance-voltage method.[1] (M. G. Buehler, x3541)



Dopant profile of a phosphorus-implanted region in 5-Ω•cm *n*-type silicon from dc measurements on an enhancement-mode MOSFET.

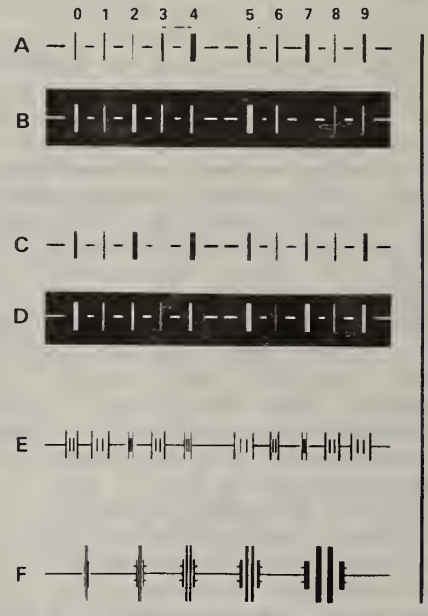
Nondestructive Second Breakdown Test

The nondestructive test method for detecting thermal instabilities of bipolar transistors, previously applied to the refinement of the forward-bias safe operating area (SOA), has been extended to the determination of second breakdown susceptibility. The test method is based upon measuring the time derivative of emitter-base voltage (dV_{EB}/dt) which shows a well-defined peak at the onset of instability. This peak is used to trigger a removal of power from the device under test before a hot spot can occur. For low-current operating conditions, second breakdown follows immediately after the thermal instability. At higher currents stable hot spots occur. In this case, it is found that a second peak in dV_{EB}/dt occurs before actual second breakdown. This reversal can be used to trigger removal of power from the device before second breakdown occurs, but after thermal instability. This contrasts with the more common method which allows a device to first experience second breakdown before removal of power. Although this method does not destroy the device, the peak junction temperature before shut-off may exceed 300°C. Therefore, the method is not recommended for device rating, testing, or inspection of SOA limits. With it, however, one can generate the entire loci of both thermal instability and second breakdown on a single device. Because previously used tests were destructive, determination of the actual second breakdown locus on a single device has been heretofore impossible. The new method can be employed with a sim-

ple modification of the standard circuit for measuring thermal resistance with V_{EB} as the temperature sensitive parameter. Many second breakdown test circuits can also be modified to use the new sensing technique.[2] (D. L. Blackburn, x3621)

Line-Width Measurement Calibrations

Calibration of selected lines on ten photomask-like black-chrome-on-glass artifacts was initiated in preparation for a full-scale interlaboratory evaluation of the newly developed procedures for line-width measurements in transmitted illumination. The pattern on these second-generation artifacts contains six rows of ten isolated or multiple lines in the 1- to 10-μm range. Provision is made for measurement of both line spacing and line width. The rationale for the design of this artifact is described in the January 1978 issue of *Solid State Technology*. In addition, a training seminar was conducted at which representatives of 32 organizations — integrated circuit, instrument, and photomask houses — gained experience in the line-width measurement procedures through lectures, group discussions, and laboratory exercises. Because of the success of this seminar and to meet the demand for additional training of this type, the second seminar in this series has been scheduled to be held in June 1978.[1,2] (J. M. Jerke, x2185)



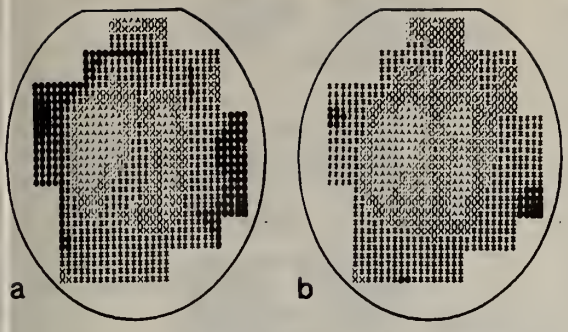
Pattern of second-generation photomask-like artifact for line-width calibration.

Resonance Ionization Spectroscopy

Initial results were obtained as a prelude to the study of the applicability of resonance ionization spectroscopy to the detection of very low ($\gtrsim 10^{12}$ cm^{-3}) impurity densities in solids. In this application, resonance ionization spectroscopy will be combined with laser-induced vaporization. Research on this technique is being conducted in order to develop it as an analytical tool to be applied to the detection of trace impurities in solid semiconductor materials such as silicon and gallium arsenide. Quantitative results are in principle possible through calibrated samples containing known impurity densities. As a first step in this research, sodium resonance ionization was demonstrated by a two-photon absorption experiment. Sodium vapor was irradiated with two simultaneous light pulses of wavelength $\lambda_1 = 589.592$ nm and $\lambda_2 = 568.263$ nm to induce $3^2S_{1/2} \rightarrow 3^2P_{1/2}$ and $3^2P_{1/2} \rightarrow 4^2D$ transitions in atomic sodium included in a proportional counter. Ionization of sodium in 4^2D state takes place through further interaction with λ_1 or λ_2 light pulses. The released photoelectron triggers a Townsend avalanche in the counter. Tunable dye lasers pulsed at 40-s intervals with an energy of about 1 joule per pulse were used to provide the light pulses.[2] (S. Mayo, x3625)

Gold, Leakage Current Correlation

The variable temperature wafer prober developed at NBS was used to make wafer maps of the distribution of gold donor and



Wafer maps of gold acceptor density (a) and leakage current (b).

acceptor density by means of thermally stimulated capacitance measurements on n^+p and p^+n diodes, respectively. These distributions were shown to correlate well with wafer maps of leakage current measured at room temperature on the same diodes. In the example, the gold acceptor density varies from 1.9 to 7.6 × 10^{13} cm^{-3} and the leakage current, from 0.26 to 1.05 nA. The maps show five equal ranges; the darkest symbol denotes the highest range.[2,3] (R. Y. Koyama, x3625)

Isotope Shift of Sulfur in Silicon

The existence of an isotope shift in the deep level of sulfur in silicon was discovered by measuring the energy levels produced by the isotopes ^{32}S and ^{34}S using the isothermal transient capacitance technique. Samples were prepared by implantation of the appropriate isotope into the p^+ region of junctions prepared by boron diffusion into n-type substrates. The implantation was shallow and served only as an isotopically pure dopant source for the diffusion of the sulfur impurities to the junction regions. As a result, implantation-related damage does not contribute to the response curves. The energy levels of the isotope ^{32}S were found to be in good agreement with the energy levels of sulfur (95% ^{32}S) introduced by thermal diffusion; however, the deep level of the isotope ^{34}S was found to be 3% nearer to the conduction band. The difference (0.014 eV) between the deep level of ^{32}S and that of ^{34}S is significantly greater than the uncertainty in the determination of either level (0.002 eV). The existence of an isotope shift for the sulfur deep level is a strong indication that the electronic energy levels of the sulfur deep level are coupled to the thermal vibrations of the silicon lattice.[1,2,3] (D. R. Myers,* x3625, and W. E. Phillips, x3625)

*NBS-NRC Postdoctoral Fellow.

X-Levels in Indium-Doped Silicon

For some samples of indium-doped silicon, a model which includes an extraneous acceptor level, the so-called X-level, which lies nearer the valence-band edge than the indium level, has consistently given better agreement with experimental Hall effect data than alternative models which do not involve X-levels. In the analysis, one generally calculates the carrier density as a function of temperature from the assumed model and compares this with the inverse product of the Hall coefficient and the electronic charge. Since the latter does not equal the carrier density exactly, one cannot *a priori* infer that the interpretation which yields the best agreement is the correct one. As a first step to resolve this issue, the existence of X-levels in a crystal (in which their presence was inferred from the analysis of Hall data) was demonstrated by monitoring the behavior of the Hall coefficient and the apparent spectral response of X-levels beyond the indium cut-off wavelength as oxygen donors were added to the crystal by a series of 450°C anneals. The observed behavior of both parameters with oxygen donor addition was in almost perfect agreement with that predicted by the X-level interpretation and completely at variance with that predicted by the only plausible alternative not involving X-levels. By showing that X-levels must be invoked to explain the behavior, the Hall analysis was shown to be correct. It can therefore be inferred that the assumptions made in the analysis are appropriate for interpreting Hall effect data on indium-

doped silicon and that Hall effect data can be used to determine whether X-levels are present or absent.[1]

(R. D. Larrabee, x3625)

Hall Effect Analysis Program

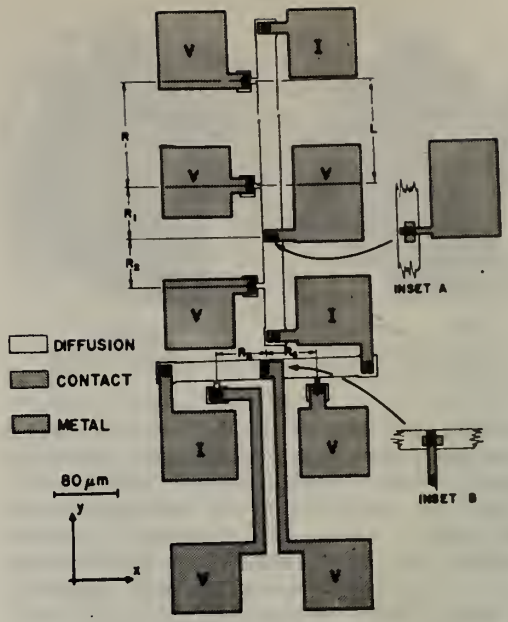
A listing of a FORTRAN computer program developed for evaluating the temperature dependence of resistivity, carrier density, and mobility of silicon is now available on request. The program has been documented by thorough annotation with comment statements and examples. This program was most recently utilized in the study of X-levels in indium-doped silicon.[1,2]

(R. D. Larrabee, x3625)

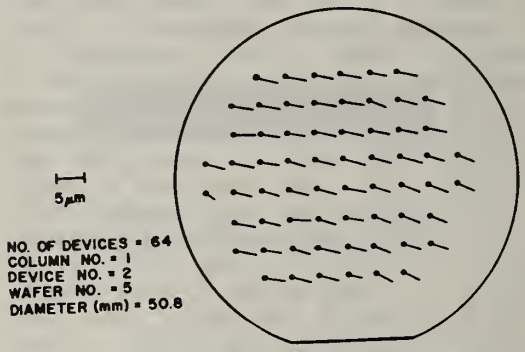
Electrical Alignment Test Structure

Results of the evaluation of a potentiometric electrical alignment test structure, fabricated with 6-μm-minimum-line-width design rules, were reported at the 1977 International Electron Devices Meeting. The structure can be incorporated in appropriate masks to enable direct electrical determination of the registration between diffusion and contact window mask levels and between contact window and metallization mask levels. The results showed that the test structure can resolve misregistration of the order of 0.1 μm. This resolution is similar to that which can be obtained with advanced visual alignment test structures. Since the electrical data can be acquired and analyzed in about one-hundredth of the time required to collect data from a visual structure, it is possible to make complete wafer maps of the misalignment. These maps can be analyzed to extract translational, rotational, and process-induced misalignment. The electrical alignment test structure can be combined with the cross-bridge sheet resistor to provide, in a compact, 12-pad structure, means for determining sheet resistance, line width, and alignment.[1]

(T. J. Russell, x3541)



Test structure for electrical measurement of misalignment of diffusion and contact window photomasks, or, if modified as shown in insets A and B, of contact window and metallization masks. Volt-current ratios R, R_1, R_2, R_3, and R_4 are measured; the spacing L is taken from the diffusion mask dimension.



Wafer map of misalignment between diffusion and contact window masks; a 5-μm lateral displacement was intentionally introduced.

Scanning Acoustic Microscopy

Surface and subsurface defects in semiconductor device structures can be viewed

with high-resolution scanning acoustic microscopy. The understanding of acoustic reflections from smooth single crystal surfaces covered with thin dielectric or metallic layers, as found in such structures, was advanced at both Stanford and Hughes. A rigid reflector model provided a qualitative explanation of the phase reversals observed as the lens-to-specimen distance is varied. However, this model does not account for the dependence of the response on the elastic properties of the materials. With an elastic reflector model it is possible to estimate the thickness of such layers. The first of three publications on the analysis of acoustic images appeared in the 15 December 1977 issue of *Applied Physics Letters*.[1] (R. I. Scace,* x3625)

Third Pacemaker Workshop

The third in a continuing series of workshops on reliability technology for cardiac pacemakers held at NBS-Gaithersburg on October 19-20, 1977, attracted 157 representatives of pacemaker manufacturers; battery manufacturers; and suppliers of materials, components, and services to the pacemaker community. The workshop provided a stimulating atmosphere to discuss the following topics: procurement and assurance of high reliability electronic components and systems; battery evaluation, characterization, and quality control; moisture measurement problems; and materials and assembly processes. A report on the workshop is being prepared. Reports of the first two workshops were published as NBS Special Publications 400-28 and 400-42.[2] (H. A. Schafft, x3625)

Future Events . . .

Stability of Thin Film Solar Cells and Materials — This workshop, being conducted by NBS in cooperation with the Division of Solar Technology, Department of Energy, is intended to provide a broad-based forum for the discussion of reliability problems which might arise in connection with the manufacture and deployment of solar power conversion systems based on thin film photovoltaic cells. The workshop is scheduled to be held at NBS-Gaithersburg on May 1-3, 1978. (D. E. Sawyer, x3621)

Carrier Lifetime and Related Device Parameters — ASTM Committee F-1 on Electronics is planning this symposium to be held in San Diego on February 15 and 16, 1979, in conjunction with its regular winter meeting. Emphasis will be on the areas of lifetime-related requirements and problems in various device technologies, interactions between lifetime and microdefects, and methods and equipment for measuring lifetime. Proceedings of the symposium, to be chaired by R. D. Westbrook of Oak Ridge, will be published by ASTM. (W. M. Bullis, x3786)

New Projects . . .

Spreading Resistance Calibration Procedures — Work on development of procedures for preparing specimen surfaces for spreading resistance calibrations and measurements is being extended to the case of high-resistivity n-type silicon typical of that used to fabricate thyristors. Surfaces of such specimens have generally been found to be unstable and very sensitive to preparation procedures and to the specific nature of the probe-semiconductor contact. Procedures capable of yielding reliable calibration of n-type surfaces while not adding problems when measuring p-type regions also found in thyristor structures are being sought.[3] (J. R. Ehrstein, x3625)

SEM Depth-Dose Study — The increasing use of electron beam instruments for processing and testing semiconductor devices makes it very desirable to have accurate data for the electron penetration and the absorbed radiation dose in various layers of the device. The scanning electron microscope (SEM) is being used to make measurements of electron penetration and absorption in a wide variety of materials of

*NBS Contact.

interest to the semiconductor industry. This depth-dose study is projected as an updating and extension of the results of Everhart and Hoff.[2] (W. J. Keery, x3625, and P. Roitman,* x3625)

Electrical Testing of Complex ICs — The difficulties of testing complex integrated circuits (ICs) are many and well-known. A review of testing and reliability problems that affect the manufacturers and consumers of digital integrated circuits was undertaken to determine whether a project in this area could be fruitfully undertaken. Initial emphasis is being placed on the testing of large scale integrated (LSI) memory devices as they exhibit many of the failure modes found in other complex devices.[2]
(T. F. Leedy, x3621)

Characterization of Reverse-Bias Second Breakdown — Work was initiated to study the characterization of power transistors under reverse-bias operation. A circuit has been designed and constructed which removes power from the device under test within about 40 ns after the occurrence of reverse-bias second breakdown. The circuit can apply over 1000 V and up to 40 A to the device under test. It has been designed so that the forward on-time and base drive as well as reverse base drive (constant current or constant voltage source) are variable over a wide range.[2]
(D. W. Berning, x3621)

Solar Cell Measurement Techniques — This new program combines development of innovative solar cell measurement techniques with activities designed to support the broader objectives of the photovoltaic plan of the Department of Energy. In the initial phases, an analysis of a proposed technique for determining solar cell "emitter" sheet resistance by nondamaging laser scanning has been carried to the point of achieving closed-form expressions relating the quantities of interest. In addition, the laser scanner is being modified so that one may study the point-by-point spatial behavior of concentrator cells, and techniques are being investigated to allow cells to be biased at arbitrary, but uniform and controlled, light levels while being scanned.[4]
(D. E. Sawyer, x3621)

*NBS-NRC Postdoctoral Fellow.

Work in Progress . . .

Mobility measurements on degenerate boron-doped silicon specimens, being made as part of the reevaluation of the resistivity-dopant density relations in silicon now nearing completion, indicate that the hole mobility does not saturate at a value as large as that previously assumed.[1] (W. R. Thurber, x3625)

An improved version of the local slope algorithm for analysis of spreading resistance profiles has been written, but discrepancies between implanted profiles obtained using this algorithm and profiles calculated from LSS theory remain.[1]
(J. H. Albers, x3625)

Tests continued of the particle impact noise detection (PIND) method for screening microcircuit packages for the presence of loose particles using specially seeded packages. The results provide further evidence that the tendency for a small particle to lock up in TO-18 devices is enhanced by higher acceleration levels at lower frequencies, but little or no correlation of lock-up behavior with frequency or acceleration level was seen on TO-5 and flatpack devices.[6] (P. S. Lederer, x3821)

Work resumed on development of the rapid gas cycling technique for the measurement of gross leaks. This method minimizes the rapid depletion of the gas from the package interior that takes place with large leaks (the factor which limits the range of currently used tracer gas leak tests) by reducing the delay time between pressurization and detection. It also provides controlled environmental conditions so that a quantitative relationship between true and measured leak values can be obtained.[1] (S. Ruthberg, x3621)

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Buehler, M. G., Limitations and Applications of the D-C MOSFET Profile Method.

Koyama, R. Y., Wafer Mapping of Electrically Active Devices.

Koyama, R. Y., Techniques for Characterizing Defects in Starting Silicon Wafers Using TSM.

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15. SUPPLEMENTARY NOTES

ARPA Order 2397, Program Code 8Y10; DNA IACRO 78-807; Dept. of Energy, Interagency Agreement EX-77-A01-6010, Task Orders A021-EES and A054-SE; NASA, Request No. S-39193B.

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This report provides information on the current status of NBS work in measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: analysis of X-levels in indium-doped silicon; evaluation of an electrical alignment test structure; correlations of gold density with leakage current in silicon; initial application of resonance ionization spectroscopy; calibration of second-generation line-width measurement artifacts; dopant profiling by dc measurements on MOSFETs; observation of an isotope shift in the sulfur deep level in silicon; development of a nondestructive test for second breakdown; analysis of scanning acoustic microscopy; and the third pacemaker workshop. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of current publications, publications in preparation, and scheduled talks are also included.

17. KEY WORDS (six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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