NBSIR 78-1444-3

Semiconductor Technology Program Progress Briefs

W. Murray Bullis, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, D.C. 20234

October 1978

Prepared for
The Defense Advanced Research Projects Agency
The National Bureau of Standards
The Division of Electric Energy Systems, Department of Energy
The Division of Solar Technology, Department of Energy
The Defense Nuclear Agency
The Charles Stark Draper Laboratory
The Army Electronics Research and Development Command
The Air Force Avionics Laboratory

ABSTRACT - This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: determination of resistivity-dopant density relationships in silicon; measurement of ion-implanted dopant profiles by spreading resistance; optical measurement of line widths on chrome photomasks, iron-oxide photomasks, and silicon wafers; additional data on sulfur impurity levels in silicon; conduct of a workshop on stability of thin film solar cells; analysis of leakage currents in gated diode test structures; calculations of the radiation dose incurred by oxide layers during x-ray and e-beam lithographic steps; correlation of selected electrical parameters on commercial rectifier diode wafers; and availability of a test pattern for determining alignment between mask levels. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

SEMICONDUCTOR TECHNOLOGY PROGRAM

TABLE OF CONTENTS

KEY WORDS: Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

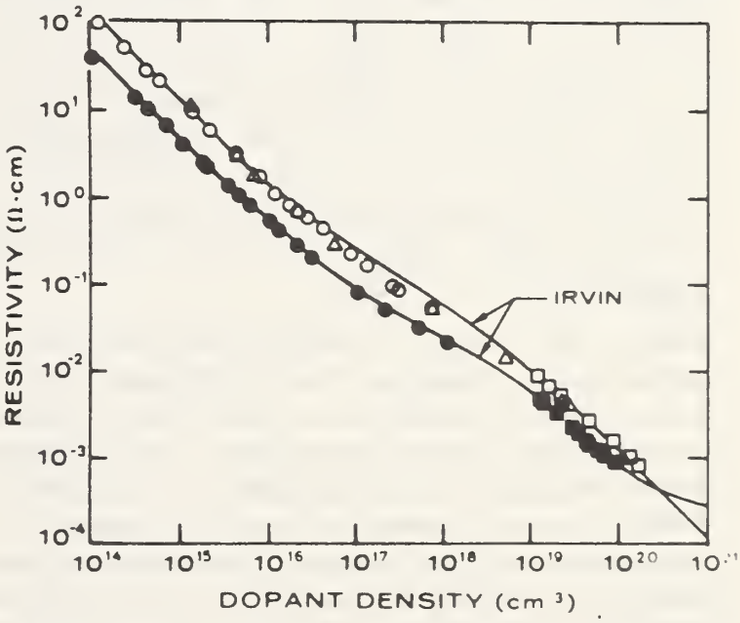
This report covers results of work during the fortieth quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Army Electronics R&D Command; and 8. The Air Force Avionics Laboratory.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of past publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Resistivity-Dopant Density Relationships

The study of the resistivity-dopant density relationships in silicon is nearing completion and preliminary results have been reported at the ECS Topical Conference on Characterization Techniques for Semiconductor Materials and Devices. These relationships are widely used in the semiconductor industry in connection with materials acceptance, process control, and device design. During the past decade, the most frequently used conversion curves for both *n*- and *p*-type silicon have been those formulated by Caughey and Thomas based on the data of Irvin. More recently, new data which differ significantly from those of Irvin in certain ranges have been reported in the literature. Because of these discrepancies, the relationships were redetermined for both phosphorus- and boron-doped silicon with dopant densities from 10^{13} to 10^{20} cm^{-3}. Careful attention was paid to selection of test wafers with uniform resistivity and to the design and fabrication of the test structures which were used for the measurements. In the dopant density range below about 10^{18} cm^{-3}, the net dopant density was determined from capacitance-voltage measurements on gated junction diodes, and the resistivity was measured with planar, square-array, four-probe test structures. In the dopant density range above about 10^{19} cm^{-3}, the resistivity and net carrier density were determined from Hall mobility measurements on van der Pauw specimens cut ultrasonically from the bulk silicon slices. Neither procedure is fully satisfactory for use on specimens with dopant density between 10^{18} and 10^{19} cm^{-3}.

In developing the results, it was found to be essential to take into account the fact that not all dopant atoms are ionized in the intermediate range of dopant density ($\sim 10^{17}$ to $\sim 10^{19}$ cm^{-3}). Accurate determinations of the ionized fraction are hampered by uncertainties in Hall scattering factor, r (which preclude accurate determination of the carrier density in the intermediate dopant density range). The new results for the resistivity-dopant density relationship for phosphorus- and boron-doped silicon depart significantly from the Irvin curves, particularly for boron-doped material with resistivity below 1 Ω•cm. The maximum discrepancy for boron-doped silicon occurs near 0.1 Ω•cm where the Irvin curve predicts a dopant density almost double that measured in this work. For phosphorus-doped material, the present results differ from the Irvin curve by 5 to 10 percent over the



Resistivity as a function of dopant density for silicon at 300 K. Data for boron- and phosphorus-doped specimens are shown as open and solid symbols, respectively. Circles are data obtained from junction capacitance-voltage measurements of the net dopant density; squares are data obtained from Hall mobility measurements of net carrier density; triangles are data obtained from nuclear-track measurements of the total boron density.

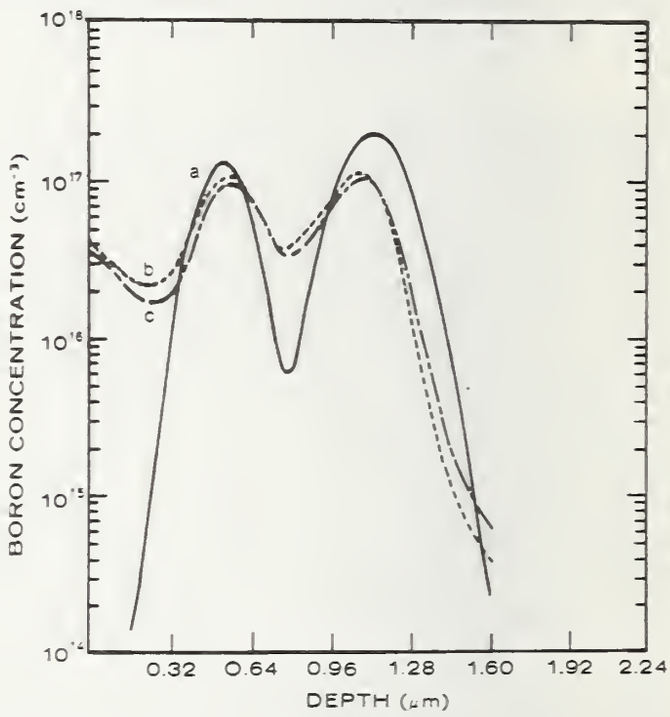
entire resistivity range, always in the direction of lower resistivity for a given dopant density.

In addition to the uncertainty related to the dopant fraction ionized, an uncertainty remains in the results for boron-doped silicon at high dopant densities. It was assumed that r could be taken as 1.0 in the calculation of carrier density in heavily doped material because the conduction is metallic for densities greater than the degeneracy density, which at room temperature is 2×10^{19} cm^{-3}. Although this assumption appears to be satisfactory for *n*-type silicon, the nonparabolic valence band structure of silicon may result in a value of r that is not unity in the degenerate range for *p*-type silicon. Attempts to resolve this question experimentally have so far proved inadequate because the several methods which have been employed in efforts to obtain an independent measure of the dopant density in this range have not had sufficient accuracy. If the Hall scattering factor for degenerate *p*-type silicon has a value of about 0.8 (as suggested by calculations of Li, University of Florida), the present data would agree quite closely with that of both Irvin and Wagner in this range.

Additional work is being carried out in efforts to resolve the remaining uncertainties. In addition, empirical expressions are being developed to provide engineering curves suitable for use in modeling and computation. In order to preserve the distinction between carrier density and dopant density, expressions are being developed to fit curves of the product of dopant density and resistivity (and its inverse) as a function of resistivity as well as curves of mobility as a function of carrier density. [Sponsor: 1] (W. R. Thurber, x3625)

Dopant Profiles by Spreading Resistance

The local slope method for correcting spreading resistance data to obtain dopant profiles has been refined so that the spreading resistance profiles of ion implantations are in good semiquantitative agreement with the actual dopant distributions. Although the spreading resistance technique is a potentially powerful method for measuring the dopant distribution by reason of its large dynamic range and small sampling volume, its use has been limited by the necessity for large corrections to the measured data, especially if the dopant density is rapidly varying (orders of magnitude over a few micrometers). Corrections have been particularly troublesome for ion implantations which generally have an increasing dopant density near the surface and a decreasing dopant density deeper into the material. The local slope method is based on an assumed form for connecting two asymptotic models for the conduction process involved in the spreading resistance measurement. It has the added virtue that, because of its simplicity, the correction factor can be calculated on a desk-top calculator, affording a real-time analysis of the measurement. In addition, the simplicity



Profiles of boron double implant (200 and 500 keV, doses of 3×10^{12} cm^{-2} and 6×10^{12} cm^{-2}): (a) Gaussian prediction, (b) multilayer spreading resistance profile, and (c) local slope spreading resistance profile.

of the method also makes it feasible to incorporate additional refinements to allow for data smoothing and iterative determination of effective probe radius (which is a function of local resistivity). With these refinements, it was possible to correct spreading resistance data taken on a silicon wafer doubly implanted with boron to provide a two-peak distribution to obtain peak densities and peak locations which are in reasonable agreement both with values predicted from a Gaussian model for the implantation process and with values predicted from the multilayer technique which is based on the solution of Laplace's equation for a system of parallel layers of differing resistivity. Additional refinements of the local slope method are being investigated to determine if further improvement can be obtained. [Sponsor: 1] (J. H. Albers, x3625, and J. R. Ehrstein, x3625)

Optical Line-Width Measurements – I

The second in a series of seminars on Micromeasurements on Integrated-Circuit Photomasks was held at NBS-Gaithersburg June 6 through 8. The seminar, which was provided in order to assist in the transfer to the industry of the results of research on measurement of line widths on chrome photomasks in transmitted light, was held in response to requests from individuals unable to attend the first seminar in this series, held last November. An additional 24 individuals representing 18 different integrated circuit and line width-measurement equipment manufacturers attended the seminar. A publication comprising the edited versions of the lecture notes used in the seminars is being prepared. A third seminar, which is tentatively scheduled for the late fall of 1979, is expected to cover line-width measurements on silicon wafers and see-through masks as well as line-width measurements on chrome masks.

Data have been received from several of the participants in the ten-laboratory evaluation of the procedures for measuring line widths on chrome photomasks. It is planned to develop the line-width calibration artifact for issuance as a standard reference material if the results of the interlaboratory evaluation experiment are satisfactory. [Sponsors: 1,2] (J. M. Jerke, x2185)

Optical Line-Width Measurements – II

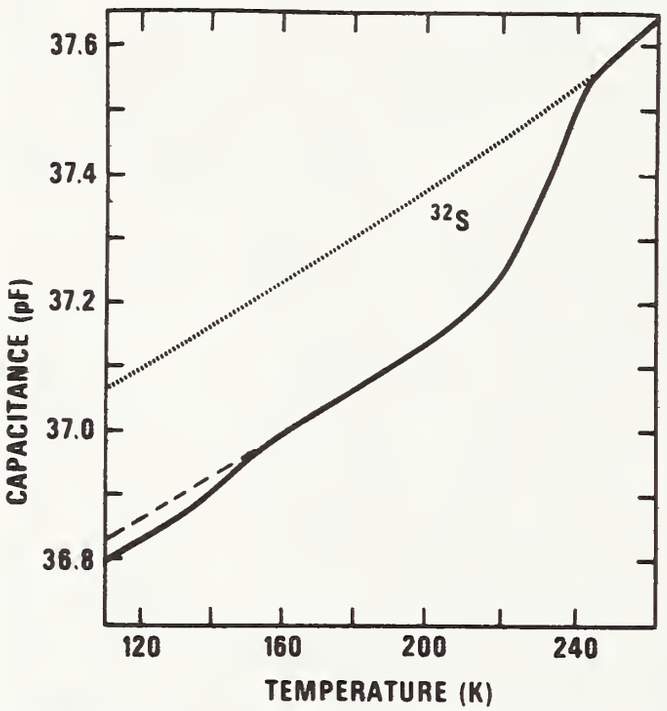
Significant differences of up to 1 μm can be encountered for optical measurements of lines less than 10 μm wide on both see-through photomasks and wafers. Previous NBS work on the development of line-width calibration methods has shown the need for including a correction for the phase difference at the line edge as seen by the optical microscope for both transmitted light measurements on see-through photomasks and reflected light measurements on wafers. Early attempts to determine this phase difference from external interferometer systems produced poor agreement between theoretical and experimental line-image profiles and cast a large uncertainty on the resulting line-width measurement. Current theoretical work shows that this phase difference can be determined directly from the line-image profile in either transmitted or reflected light. NBS line-width calibration systems which record the photometric line-image profiles can incorporate this phase correction for the accurate measurement of line widths on see-through photomasks and wafers. This technique, which is described in detail in the proceedings of the recent conference on Developments in Semiconductor Microlithography III, will be used to calibrate the test artifacts for use in a forthcoming interlaboratory evaluation of procedures for line-width measurements on iron-oxide photomasks. [Sponsor: 1] (D. Nyyssonen, x2185)

Sulfur Levels in Silicon

Study of the electrically active sulfur introduced into silicon by ion implan-

tation predeposition followed by thermal drive-in indicates that the density associated with the shallower level (0.235 eV below the conduction band edge) is not always the same as that associated with the deeper level (∿0.52 eV below the conduction band edge). The densities of active centers were determined from the magnitudes of the dynathermal capacitance transients. For the case of ^{32}S implanted to a dose of 2×10^{14} cm^{-2}, both centers were present with equal density, 1.5×10^{13} cm^{-3}. This result is similar to that observed in previous published studies of sulfur diffused into silicon.

However, for the case of ^{32}S implanted to a dose of 1×10^{13} cm^{-2}, the transients for the shallow and deep centers were no longer of the same magnitude as illustrated in the accompanying figure. The deeper sulfur defect appears at almost the same density as for the higher fluence predepositions; however, the density of the shallower defect is reduced by approximately a factor of seven. Implantation of ^{34}S to a dose of 1×10^{13} cm^{-2} also led to unequal transients for the shallow and deep centers. As reported previously, the energy of the deep center for the ^{34}S implant was shifted 0.014 eV toward the conduction band edge from the energy of the deep center for the ^{32}S implant; however, no such isotope shift could be observed for the case of the shallower center.



Dynathermal capacitance response of silicon p-n junction diode doped with ^{32}S to a dose of 1×10^{13} cm^{-2}. The capacitance shifts which occur in the neighborhood of 145 and 235 K are proportional to the densities of the shallow and deep sulfur centers, respectively.

The isotope shift of the deep center is evidence of strong coupling between the impurity electronic wavefunctions and the vibrations of the surrounding lattice. This electron-lattice coupling had not been considered in any of the published theoretical treatments of sulfur in silicon. The density differences observed in the more lightly implanted specimens bring into question another aspect of the theoretical treatments of the sulfur center. Those studies that relied on the effective mass theory predict that substitutional sulfur would have two energy levels within the silicon bandgap, while models of the same center based on the Slater self-consistent field method had suggested that one of the sulfur energy levels would be resonant with the silicon valence band. The fact that equal densities had been seen for the shallow and deep defect levels had been taken as implying that both these levels arose from the same center, thereby supporting the pseudopotential treatment. However, the present results suggest that the density of the center responsible for the shallow level increases with increasing sulfur implant dose while the density of the center responsible for the deeper level remains nearly constant, thus weakening the support for the pseudopotential model. [Sponsors: 2,3] (D. R. Myers,* x3625, R. Y. Koyama, x3625, and W. E. Phillips, x3625)

Gated Diode Test Structures

In earlier experiments, it was determined that the gated diode structure on

*NBS-NRC Postdoctoral Research Associate.

test pattern NBS-12 exhibits excess leakage currents which cause uncertainty in the determination of the surface and bulk leakage currents. Using a variety of diodes with differing geometrical configurations, it was determined that the excess leakage current in the gate-surface-accumulated regime is directly proportional to the length of the inner perimeter of the gate. This finding, together with the previously determined result that the excess leakage current in accumulation is proportional to the electric field intensity between the diode and the gate, confirms that the periphery of the diode (along the inner perimeter of the gate) is the source of the excess leakage. The current is due to soft breakdown effects at the periphery of the diode which occur when the depletion region is tending to be forced into the edge of the p^+ base diffusion. The complementary effect occurs in inversion, when the gate is forcing the inversion region against the channel stop diffusion. In either case, the situation may be thought of as the approach toward a p^+-n^+ diode.

The excess currents cause uncertainty in the estimate of the values of the bulk generation leakage currents. In severe situations, the baseline of the leakage current ***vs.*** gate voltage curves is distorted enough to prevent determination of the bulk generation currents. The circumstances which tend to minimize the baseline distortion are that (1) the diode-to-gate voltage difference is small, and (2) the perimeter-to-area ratio of the diode is small. In this context, "small" is relative; it depends on the particular wafer properties. The present results can be used to determine geometrical constraints on the designs of gated diodes which will suppress or emphasize one or more of the leakage current sources. The tradeoffs would be decided by the needs of a particular situation.

Leakage currents due to the soft breakdown effects are expected to be especially significant when the device parameters enhance soft breakdown under the edge of a control gate and when the performance of the device is especially sensitive to leakage. An example would be dark current in a charge-coupled device.

In an advanced test structure, also being developed, the gated diode is connected to an on-chip electrometer amplifier. The amplifier permits measurement of extremely small leakage currents using conventional high-speed automated test equipment. The fundamental concept of this advanced test structure is that the amplifier measures the reverse bias voltage decay of the gated diode as the leakage currents neutralize the charge stored by the diode junction capacitance. The diode junction is connected directly to the gate of the amplifier FET. If the capacitance of the FET gate is small compared to the diode capacitance, no correction need be made for displacement currents in the FET gate, ***viz.***, the open circuit voltage decay of the diode is the amplifier input signal. The output voltage signal is given by the amplifier transfer characteristics, which may be determined for each advanced test structure during testing. [Sponsor: 6]

(G. P. Carver, x3541)

Solar Cell Workshop

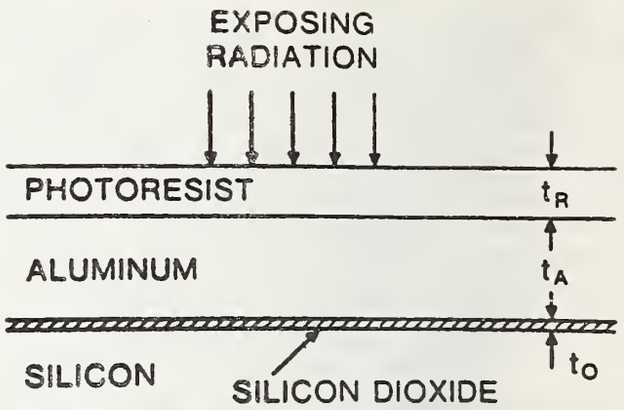
A workshop on the Stability of (Thin Film) Solar Cells and Materials was conducted at NBS-Gaithersburg on May 1 through 3 as part of the Department of Energy's National Photovoltaic Program. The workshop addressed many of the problems and obstacles to achieving stability and long life of terrestrial solar cell devices using forefront technology. The following three groups of exploratory solar cell materials and concepts were considered: (1) [CdZn]S/Cu_2S, CdS/Cu-ternaries, CdS/InP, and amorphous Si, (2) polycrystalline, MIS, and conducting-oxide Si, and (3) polycrystalline and AMOS GaAs.

Researchers in the field reviewed modes and mechanisms for failure and degradation of these systems and the status of present reliability testing. Speakers from related device technologies discussed measurement and test approaches that they have used. Two talks of particular interest described a technique for detecting changes in the physics of failure with increasing severity of a stress test to establish the maximum possible acceleration factor for a given failure and a technique for uncoupling different failure mechanisms from an analysis of failure rate data.

Among the conclusions by the 102 scientists and engineers who attended the workshop are that more research needs to be conducted in this forefront technology. One general need called out was study of the chemical, mechanical, and physical compatibility of the various materials used in these solar cell devices and their influence on device characteristics. Also expressed was the need for the development of performance and measurement standards for use at the buyer-seller interface. Finally, the need for adequate device manufacturing process controls and adequately described test procedures and data was underscored as a prerequisite for meaningful headway in the quantification of solar cell stability and long life. [Sponsor: 4] (D. E. Sawyer, x3621)

Process-Induced Radiation Damage

X-ray and direct-writing electron-beam lithographic techniques for integrated circuits are promising lithographic technologies with demonstrated linewidth resolution capability below 1 μm. These techniques have the potential problem that significant radiation damage to device structures may occur during their use. If the x-rays and electrons have sufficient energy to penetrate to critical dielectric layers such as silicon dioxide, the classical radiation damage phenomena observed in dielectric films exposed to ionizing



Schematic diagram of typical device structure. For the calculations, t_O = 100 nm, t_A = 1000 nm, and t_R = 500 nm.

radiation will result. Process sequences must be designed to take this damage into account so that its effects can be minimized by proper annealing.

Estimates of the radiation dose incurred by oxide layers while using x-ray and direct-writing electron-beam lithographic techniques were developed for the typical device structure schematically represented in the accompanying figure. The silicon substrate is covered with 100 nm of silicon dioxide which is covered with 1000 nm of aluminum metallization which is in turn covered with 500 nm of resist material to be patterned. For exposure of typical x-ray resists with aluminum K_α radiation, the dose absorbed in the oxide is estimated to be in the range of 0.08 to 40 Mrad(SiO_2). This estimate is based on a calculated dose of approximately 0.08 Mrad(SiO_2) for each joule absorbed per cubic centimeter of resist.

For typical electron-beam resists, the dose deposited in the silicon dioxide layer is estimated to be in the range of 1 to 20 Mrad(SiO_2). This estimate is based on a calculated dose of 2 Mrad(SiO_2) in the oxide layer for a 15-keV electron beam with an incident flux of 1 μC/cm^2 and a calculated dose of 3 Mrad(SiO_2) in the oxide layer for a 25-keV beam with the same incident flux.

These estimates, which have been based on the use of positive resist, suggest that the dose incurred while using x-ray

or e-beam lithographic techniques is sufficient to cause severe device degradation. The use of negative resist would reduce, but not eliminate, the problem. Thermal annealing of devices exposed to ionizing radiation is thought to remove most of the oxide damage manifesting itself as trapped positive charge and restore the preirradiation electrical parameters. Annealing temperatures are usually in the 250 to 400°C range; the time required can vary from minutes to hours. However, radiation-induced neutral electron and hole traps have been observed in silicon dioxide layers. These neutral traps do not appear to be removed by annealing at temperatures below 550°C. Since these traps are neutral until filled with carriers, they cannot be detected by capacitance-voltage measurements alone. However, a source of carriers produced by ionizing radiation in the oxide can rapidly fill these traps and cause shifts in device threshold voltages. These neutral traps can also contribute to device instability or other reliability problems by trapping injected hot carriers.

These results suggest that mechanisms of generation and annealing of radiation-induced traps should be further investigated, that optical lithographic techniques should be pushed to their resolution limits, and that more sensitive e-beam and x-ray resists which will reduce radiation exposure should be developed. [Sponsors: 1,2,5]

(K. F. Galloway, x3625, P. Roitman,* x3625, and S. Mayo, x3625)

Rectifier Diode Parameter Correlations

Several electrical parameters which should be related to the presence of deep level defects are being investigated. Wafer maps of diode reverse leakage current, forward voltage drop, and open-circuit voltage decay (OCVD) lifetime were made on commercially fabricated rectifier diode wafers. Each wafer contained approximately 150 diodes. Although not all the measured parameters depend on the same mechanisms, their variations across the wafer were similar in nature. For example, forward voltage drop at 10 μA depends primarily on recombination, whereas the reverse leakage current at a reverse bias of 15 V depends primarily on generation in the depletion region; yet, the similarity of the wafer maps, shown in the accompanying figure, suggests that they originate from a common defect. [Sponsor: 3]

(R. Y. Koyama, x3625)

*NBS-NRC Postdoctoral Research Associate.

Wafer maps of (a) forward voltage drop, V_F, (b) reverse leakage current, I_R, and (c) open circuit voltage decay lifetime, τ, measured on a commercially fabricated rectifier diode wafer. Darker symbols represent higher values; V_F ranges from 0.285 to 0.309 V; I_R, from 3.5 to 19.1 nA; and τ, from 4.9 to 9.4 μs.

Availability of Test Pattern NBS-15

Documentation for test pattern NBS-15 is being prepared. This pattern is embodied in a three-level mask set which contains a variety of potentiometric electrical alignment test structures with which maps of the misalignment between the diffusion and contact-window mask levels or between the diffusion and metallization mask levels can be rapidly made with the use of automatic test equipment.

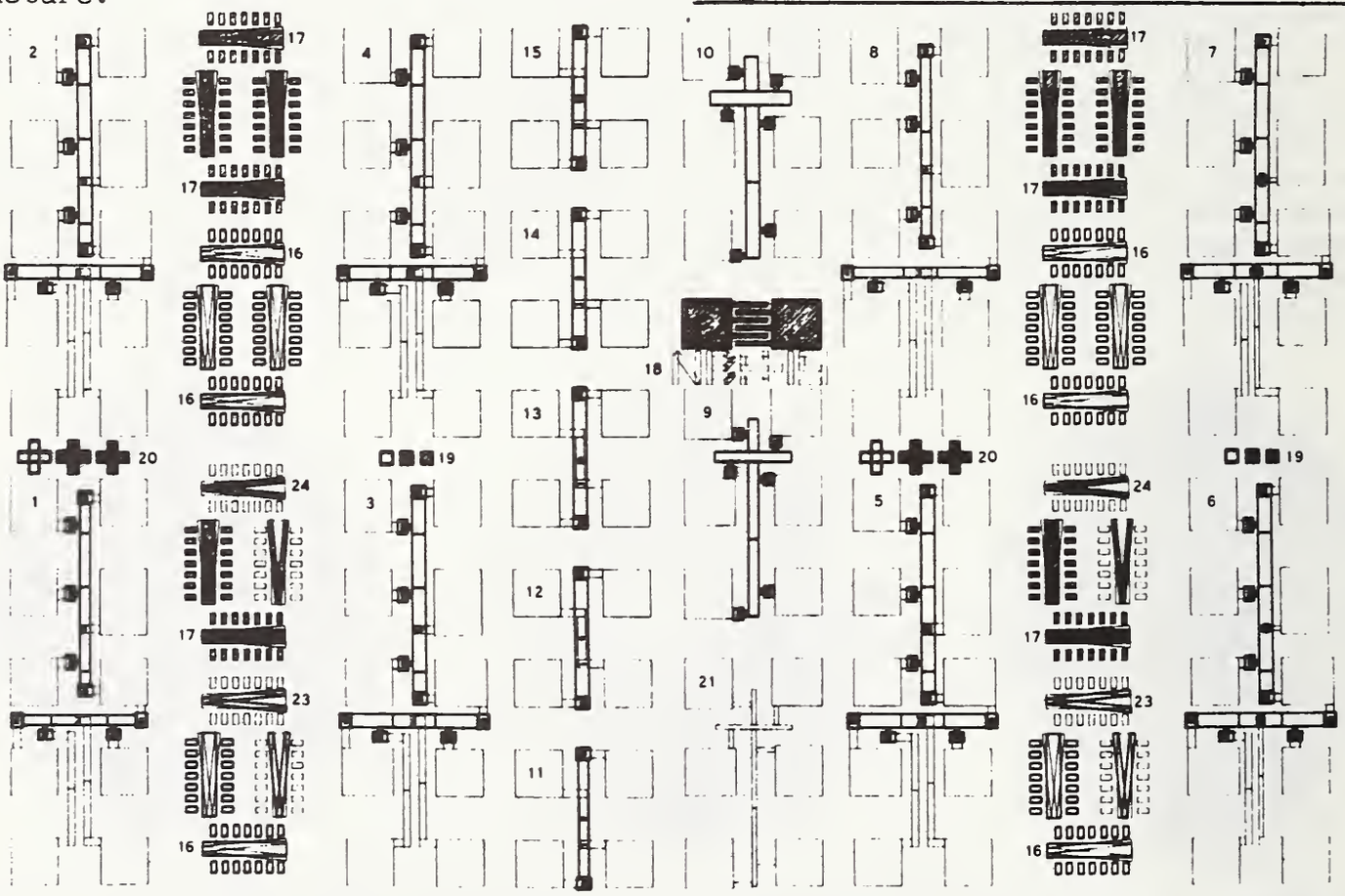
The pattern also contains optical alignment test structures, selected contact resistors and cross-bridge test structures, and several sets of alignment markers. The contact resistors are particularly important because it has been found that incomplete etching of contact windows or an aluminum-silicon alloying can cause spurious results in measurements on the electrical alignment test structure.

A report summarizes the test structures that are included in the test pattern and lists references which explain how each of the structures is measured. In addition, a magnetic tape of the test pattern can be supplied with information necessary for a computer-controlled pattern generator to fabricate the photomasks. [Sponsor: 1]

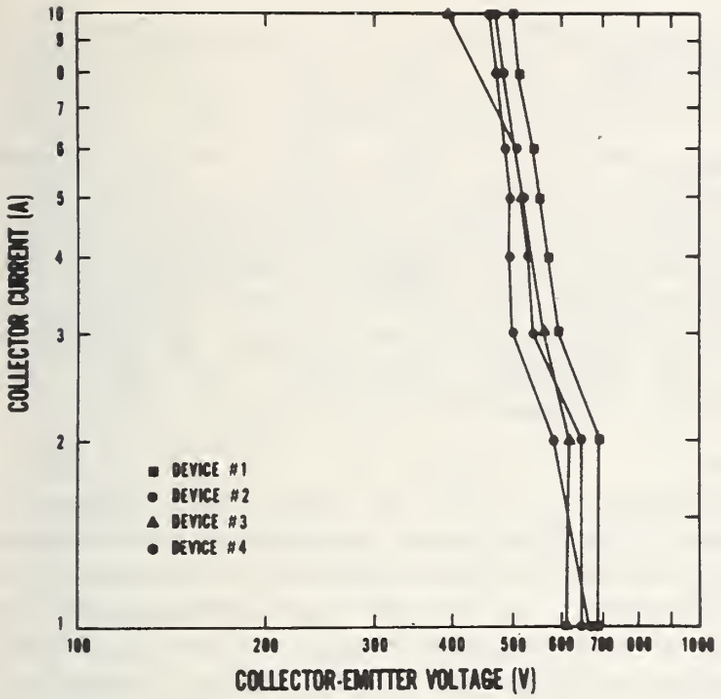
(T. J. Russell, x3541)

Reverse-Bias SOA Curves

The test circuit which was developed to permit the nondestructive measurement of reverse-bias breakdown characteristics of transistors was used to generate reverse breakdown for several different transistors. Each curve can be made with a single transistor by virtue of the ability to remove power within 40 ns after the breakdown event. A graph of the breakdown loci of several different



Check plot of a die in test pattern NBS-15. The diffusion level is shown with heavy outlines; the contact-window level, with cross hatching; and the metallization level, with light outlines. Extra lines which outline adjacent flashed rectangles have not been removed.



Measured points at which second breakdown occurred for four different transistors with the same 2N number, manufactured by the same company. For all measurements, the forward and reverse base currents were 20% of the collector current.

transistors from the same lot showed variations of 100 to 200 V for breakdown at identical collector currents, demonstrating the need for the nondestructive test for obtaining data accurate enough for research purposes. [Sponsor: 2]

(D. W. Berning, x3621)

New Topics . . .

Laser Annealing of Low-Fluence Implants – A task has been undertaken to extend the study of laser annealing of ion-implanted silicon to the case of low-fluence ($\sim 10^{12}$ cm^{-2}) implants. The results of initial measurements suggest that even for low-fluence implants, laser annealing can produce electrical activation identical to thermal annealing without measurable diffusion of the implanted species, and, more importantly, that the crystalline quality of the laser-annealed areas may be significantly improved compared to thermal annealing. Since earlier reported studies have been limited to studying regions implanted with fluences several orders of magnitude larger, the effectiveness of laser annealing on these less heavily damaged layers had been unclear. The present study is made possible by the use of capacitance-voltage profiling and electron-beam-induced-current-mode SEM examination of aluminum Schottky barrier diodes. These techniques are sensitive to orders of magnitude smaller densities of implanted impurities than the physical analysis techniques which had dictated the high-fluence implants for previous studies of laser annealing. [Sponsor: 2]

(D. R. Myers,* x3625, P. Roitman,* x3625, and S. Mayo, x3625)

Back-Channel Leakage in CMOS/SOS – The dc MOSFET profiling technique is being developed for profiling the channel region of *n*-channel MOSFETs fabricated in silicon on sapphire. A test pattern (NBS-17) has been designed to pursue investigations of back-channel leakage in CMOS/SOS devices using the dc MOSFET technique. The pattern contains over forty structures including four-terminal MOSFETs, closed geometry MOSFETs, MOSFETs with varying channel lengths, secondary ion mass spectroscopy structures, and other structures not available on existing SOS test patterns. The pattern also contains metal-gate bulk structures which can be utilized in auxiliary experiments designed to obtain a better understanding of this measurement technique. [Sponsor: 5]

(L. W. Linholm, x3541)

Cross-Bridge Sheet Resistors – A study was initiated to determine the sensitivity of the cross-bridge sheet resistor test structure to several geometric permutations. The permutations presently under consideration are the width of the active area and the presence or absence of symmetry tabs. Preliminary results suggest that the measured sheet resistance increases as the design width of the active area is reduced from 24 μm through 18 μm and 12 μm to 6 μm. [Sponsor: 1] (R. L. Mattis, x3541)

*NBS-NRC Postdoctoral Research Associate.

Hall Scattering Factors in Silicon – The development of theoretical expressions for hole and electron mobilities in silicon at the University of Florida is being extended to include the Hall scattering factors in n- and p-type silicon. By taking into account both band properties and all scattering mechanisms in the derivations, the resulting expressions would allow accurate computation of electron or hole density from Hall effect measurements on extrinsic silicon. [Sponsor: 1]

(W. R. Thurber,* x3625)

Work in Progress . . .

Further studies are being carried out on the NBS-developed test circuit for detecting the onset of thermal instability for use in specifying and confirming transistor safe-operating-area limits in the forward-bias region. It was found that the sensitivity of the test circuit to the onset of thermal instability at high currents is not sufficient to assure detection. Although the hot spots at high currents may not be as severe as those at low currents, the peak junction temperature increases as the thermal instability limit is exceeded. Other means of detecting or establishing the limit for these currents are being investigated. [Sponsor: 2]

(S. Rubin, x3621)

Initial evaluations of the apparatus for the rapid gas cycling gross leak test were carried out. The essence of this test method is a rapid sequence comprising (1) back pressurization of the test specimen(s), (2) elimination of the tracer gas from the chamber ambient around the specimen by multiple expansion steps, and (3) coupling of the chamber to the leak detector with minimum lapse time. Sequential operation of pressure-vacuum valve combinations is required with precise time intervals. Although such precise operation is best obtained with microprocessor control, the initial study was conducted using mechanical control and electrical step switching. It was observed that the first stage gas expansion ratio follows the predicted value, but second stage expansion does not. Leakage in the test chamber manifold is limiting ultimate pressure, which affects the second stage expansion. In addition, differences in the valve timing which were encountered also adversely affected the test results. [Sponsor: 1,2]

(S. Ruthberg, x3621)

Extensive testing of the effect of specimen preparation on spreading resistance measurements of high resistivity n-type specimens is nearly completed. Results to date indicate that, in terms of the repeatability of the measured value of the spreading resistance, polishing with 0.5-μm diamond in a nonaqueous medium appears to be the surface preparation which gives the most consistent results. This technique is also clearly superior to others in terms of high signal-to-noise ratio. [Sponsor: 3]

(J. R. Ehrstein, x3625)

Investigation of reflectance techniques to characterize the surface quality of sapphire substrates continued at RCA Laboratories. Silicon films, 0.4 and 0.6 μm thick, were grown on sapphire substrates with a wide range of surface polishing damage as characterized by infrared reflectance ratios ranging from less than 0.1 to nearly 1.0. The films, grown on both unannealed substrates and substrates annealed at 1500°C, were characterized by ultraviolet reflectance. Although there was considerable variability in the ultraviolet reflectance of a given film, the results indicate that the quality of films grown on annealed substrates is essentially independent of the initial state of surface damage of the substrate. [Sponsor: 1] (K. F. Galloway,* x3625)

Recent Publications . . .

Swyt, D. A., Rosberry, F. W., and Nyssonen, D., Calibration of Optical Microscopes for Photomask Linewidth

*NBS Contract.

Measurements, *Proc. Microelectronics Seminar — Interface '77*, Monterey, California, October 5-7, 1977, pp. 131-144.

Oroshnik, J., and Croll, W. K., Threshold Adhesion Failure: An Approach to Aluminum Thin-Film Adhesion Measurement Using the Stylus Method, *Adhesion Measurement of Thin Films, Thick Films, and Bulk Coatings*, ASTM STP 640, K. L. Mittal, Ed, pp. 158-183 (ASTM, Philadelphia, 1978).

*Zanzucchi, P. J., Duffy, M. T., and Alig, R. C., Optical Reflectance Method for Determining Surface Quality of Sapphire, *J. Electrochem. Soc.* 125, 299-305 (February 1978).

*Schwarz, S. A., Helms, C. R., and Spicer, W. E., High Resolution Auger Sputter Profiling Study of the Effect of Phosphorus Pileup on the Si-SiO_2 Interface Morphology, *J. Vac. Sci. Technol.* 15, 227-230 (March/April 1978).

*Strausser, Y. E., and Majumder, K. S., The Chemical Structure of the Al/SiO_2 Interface, *J. Vac. Sci. Technol.* 15, 238-239 (March/April 1978).

Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test — How to Use It, How to Abuse It, *Proc. 1978 IEEE Electronic Components Conference*, Anaheim, California, April 25, 1978, pp. 291-299.

Blackburn, D. L., and Larrabee, R. D., Automated Photovoltaic Technique for Nondestructively Measuring Resistivity Variations of High-Resistivity Silicon Wafers, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 168-179 (ECS, Princeton, 1978).

Buehler, M. G., Limitations and Applications of the D-C MOSFET Profile Method, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 241-252 (ECS, Princeton, 1978).

*Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Auger Sputter Profiling Studies of the Si-SiO_2 Interface, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 136-138 (ECS, Princeton, 1978).

Koyama, R. Y., Wafer Mapping of Electrically Active Devices, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 220-228 (ECS, Princeton, 1978).

Koyama, R. Y., Techniques for Characterizing Defects in Starting Silicon Wafers Using TSM, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 53-60 (ECS, Princeton, 1978).

Larrabee, R. D., Interpretation of Hall Measurements, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 71-76 (ECS, Princeton, 1978).

Thurber, W. R., Mattis, R. L., and Liu, Y. M., Resistivity-Dopant Density Relationship for Silicon, *Semiconductor Characterization Techniques*, Proceedings Volume 78-3, P. A. Barnes and G. A. Rozgonyi, Eds, pp. 81-92 (ECS, Princeton, 1978).

*Jamba, D. M., Secondary Particle Collection in Ion Implantation Dose Measurement, *Rev. Sci. Instrum.* 49, 634-638 (May 1978).

Galloway, K. F., and Mayo, S., On the Compatibility of X-Ray Lithography and SOS Device Fabrication, *IEEE Trans. Electron Dev.* ED-25, 549-550 (May 1978).

Oettinger, F. F., Ed, Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1 to December 31, 1977, NBSIR 78-1474 (May 1978).

Novotny, D. B., and Ciarlo, D. R., Automated Photomask Inspection, *Solid State Technology* 21 (5), 51-59, 76 (May 1978) and 21 (6), 59-67 (June 1978).

Blackburn, D. L., Photovoltaic Technique for Measuring Resistivity Variations of High Resistivity Silicon Slices, *NBS J. Res.* 83, 265-271 (May-June 1978).

Koyama, R. Y., Detection of Deep Levels in High Power Semiconductor Materials and Devices, *NBS J. Res.* 83, 273-281 (May-June 1978).

Myers, D. R., and Phillips, W. E., Existence of an Isotope Shift for the

*Reports of Contract Research.

Sulfur Deep Level in Silicon, *Appl. Phys. Lett.* 32, 756-758 (June 1978).

Bullis, W. M., Government Programs on Advanced Technology and Manufacturing Techniques: Comments on U.S.A., Japan, and Europe, NBSIR 78-1482 (June 1978).

*Kuczer, P., Hook, H. O., and Goodman, A. M., A Versatile High-Voltage Bias Supply for Extended Range MIS C(V) and G(V) Measurements, *RCA Review* 39, 309-339 (June 1978).

Bullis, W. M., and Mayo-Wells, J. F., Eds, Semiconductor Measurement Technology, Progress Report, July 1 to September 30, 1976, NBS Spec. Publ. 400-36 (July 1978).

Sawyer, D. E., Kessler, H. K., and Schafft, H. A., Measurement Techniques for Solar Cells, Quarterly Report: September 15 to December 31, 1977, NBSIR 78-1488 (July 1978).

Koyama, R. Y., Phillips, W. E., Myers, D. R., Liu, Y. M., and Dietrich, H. B., The Energy Levels and the Defect Signature of Sulfur-Implanted Silicon by ITCAP and TSC Measurements, *Solid-State Electronics* 21, 953-955 (July 1978).

Publications in Press . . .

*Atalar, A., An Angular Spectrum Approach to Contrast in Reflection Acoustic Microscope, *J. Appl. Phys.*

Buehler, M. G., Microelectronic Test Patterns for Use in Procuring LSICs, *Proc. Industry/Joint Services Automatic Test Conf. and Workshop*, San Diego, California, April 4-6, 1978.

Galloway, K. F., VLSI Processing, Radiation, and Hardening, *IEEE Trans. Nucl. Sci.*

*Grunthaner, F. J., and Maserjian, J., Chemical Structure of the Transition Region of the SiO_2/Si Interface, *Proc. Internat. Topical Conf. on Physics of SiO_2 and Its Interfaces*, Yorktown Heights, New York, March 22-24, 1978.

Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test — How to Use It, How to Abuse It, *IEEE Trans. Components, Hybrids, and Manufacturing Technology.*

*Helms, C. R., Johnson, N. M., Schwarz, S. A., and Spicer, W. E., Auger Sputter Profiling Studies of the Si-SiO_2 Interface, *Proc. Internat. Topical Conf. on Physics of SiO_2 and Its Interfaces*, Yorktown Heights, New York, March 22-24, 1978.

*Johannessen, J. S., Spicer, W. E., Gibbons, J. F., Plummer, J. D., and Taylor, N. J., Observation of Phosphorus Pile-Up at the SiO_2-Si Interface, *J. Appl. Phys.*

Larrabee, R. D., "X" Levels in Indium-Doped Silicon, *Proc. IRIS Specialty Group Meeting*, Annapolis, Maryland, June 13-15, 1978.

*Li, S. S., The Dopant Density and Temperature Dependence of Hole Mobility and Resistivity in Boron-Doped Silicon, *Solid-State Electronics.*

Russell, T. J., Reimann, C. T., Maxwell, D. A., and Buehler, M. G., A Microelectronic Test Pattern for Measuring the Uniformity of an Integrated Circuit Fabrication Technology, *Proc. Govt. Microcircuit Applications Conf.*, Monterey, California, November 14-16, 1978.

Sawyer, D. E., Kessler, H. K., and Schafft, H. A., Measurement Techniques for Solar Cells, Quarterly Report: January 1 to March 31, 1978, NBSIR 78-1513.

Sawyer, D. E., A Technique for Using An Optical Scanner to Reveal Solar Cell Defects, *Proc. 13th IEEE Photovoltaic Specialists Conference*, Washington, D. C., June 5-8, 1978.

*Schwarz, S. A., and Helms, C. R., A Geometrical Model of Sputtering, *Appl. Phys. Letters.*

*Strausser, Y. E., Scheibner, E. J., and Johannessen, J. S., Observations of Al_2O_3 and Free Si in the Interface Between Al Films and SiO_2, *Thin Solid Films.*

*Weglein, R. D., and Wilson, R. G., An Acoustic Gray Scale for Scanning Acoustic Microscopy and Diagnostic Ultrasound, *Ultrasound Imaging.*

*Wilson, R. G., and Weglein, R. D., Acoustic Material Signatures Using the

*Reports of Contract Research.

(Continued on Back Cover)

NBS-114A (REV. 11-77)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 78-1444-3	2. Gov't Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

Semiconductor Technology Program — Progress Briefs

5. Publication Date October 1978

6. Performing Organization Code

7. AUTHOR(S) W. M. Bullis

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234
and various contractor facilities (as noted)

10. Project/Task/Work Unit No.

11. Contract/Grant No. See item 15

12. Sponsoring Organization Name and Complete Address (Street, City, State, ZIP)

NBS, Washington, DC 20234; ARPA, Arlington, VA 22209; DNA, Washington, DC 20305; Dept. of Energy, Washington, DC 20545; C. S. Draper Laboratory, Cambridge, MA 02139; AFAL, Wright-Patterson AFB, OH 45433; Army Electronics R&D Command, Ft. Belvoir, VA 22260.

13. Type of Report & Period Covered Interim April - June 1978

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

ARPA Order 2397; Program Code 8Y10; DNA IACRO 78-807; Dept. of Energy, Interagency Agreement EX-77-A01-6010, Task Orders A021-EES and A054-SE; C. S. Draper Laboratory, P. O. DL-H-139485 (Navy contract N 00030-78-C-0100); AFAL, MIPR FY117578N2026; Army Electronics, MERADCOM, P. O. 28052.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work in measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: determination of resistivity-dopant density relationships in silicon; measurement of ion-implanted dopant profiles by spreading resistance; optical measurement of line widths on chrome photomasks, iron-oxide photomasks, and silicon wafers; additional data on sulfur impurity levels in silicon; conduct of a workshop on stability of thin film solar cells; analysis of leakage currents in gated diode test structures; calculations of the radiation dose incurred by oxide layers during x-ray and e-beam lithographic steps; correlation of selected electrical parameters on commercial rectifier diode wafers; and availability of a test pattern for determining alignment between mask levels. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

18. AVAILABILITY

[X] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[ ] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Stock No. SN003-003

[X] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151

19. SECURITY CLASS (THIS REPORT)	21. NO. OF PAGES
UNCLASSIFIED	16
20. SECURITY CLASS (THIS PAGE)	**22. Price**
UNCLASSIFIED	$4.00

USCOMM-DC 66038-P78

(Continued from Page 14)

Reflection Acoustic Microscope, *Proc. 1st Internat. Symp. Ultrasonics Matls.* *Characterization*, Washington, D. June 8-10, 1978.

U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, *Secretary*

Dr. Sidney Harman, *Under Secretary*

Jordan J. Baruch, *Assistant Secretary for Science and Technology*

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*