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Semiconductor Technology Program Progress Briefs

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ABSTRACT - This report provides information on the current status of NBS work in measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: profiling of the Si-SiO_2 interface by Auger electron and x-ray photoelectron spectroscopies; use of the laser scanner to detect hairline cracks in solar cells; use of gated diodes in evaluation of CCD imager wafers; availability of silicon resistivity standard reference materials; observation of unintentional channeling effects in low-fluence random equivalent ion implantations; initiation of a comparative study of deep level measurements; implementation of the NBS-designed circuit for determining safe-operating-area limits of forward-biased transistors; observation of acoustic material signatures; availability of test pattern NBS-4; conduct of a workshop on moisture measurements; and comparison of carrier lifetimes as measured by the surface photovoltage and photoconductive decay methods. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

SEMICONDUCTOR TECHNOLOGY PROGRAM

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KEY WORDS - Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the thirty-ninth quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Division of Solar Technology, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Army Electronics R&D Command; and 8. The Air Force Avionics Laboratory.

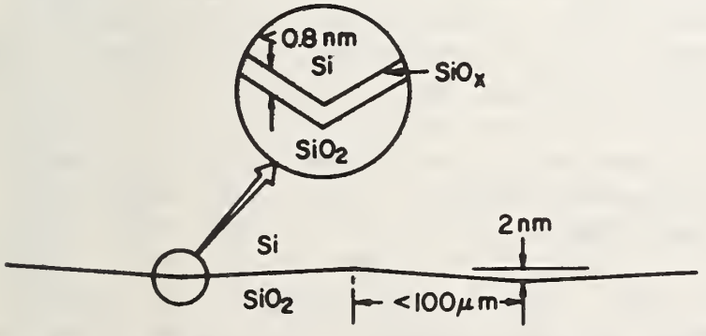
This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information and a list of past publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Profiling the Si-SiO_2 Interface

Contract efforts are currently underway to develop and refine the application of X-ray Photoelectron Spectroscopy (XPS) and Auger Electron Spectroscopy (AES) for the examination and control of electron device structures. Papers describing the application of these measurement tools to determine the chemical structure of the interface between silicon and thermally grown silicon dioxide were recently presented at the International Topical Conference on the Physics of SiO_2 and Its Interfaces (Yorktown Heights, NY, 22-24 March 1978).

In the XPS work (performed at JPL), depth profiling was accomplished using a newly developed wet-chemical etching technique which minimizes the perturbation of the remaining oxide due to oxide-solvent reaction. The data from this work indicate that the stoichiometry of SiO_2 as determined by XPS is essentially uniform except for a transitional zone within $\sim$0.5 nm of the interface. The data also give evidence for intermediate oxidation states near the interface.

In the AES work (performed at Stanford University), depth profiling was accomplished using a 1-keV argon beam to remove material by sputtering. The data are deconvolved to account for ion beam knock-on and electron escape depth effects in order to improve the depth resolution. The results indicate that there is a transition region between essentially pure SiO_2 and essentially pure Si no greater than 0.8 nm wide which undulates with a period of less than 100 μm and a peak-to-peak amplitude of about 2 nm. This picture of the interface, illustrated in the accompanying figure, is consistent both with the one emerging from the XPS work and with the results of published transmission electron microscope studies. [Sponsor: 1] (K. F. Galloway,* x3625)



Model of the Si-SiO_2 interface as derived from sputter Auger studies.

Detection of Cracks in Solar Cells

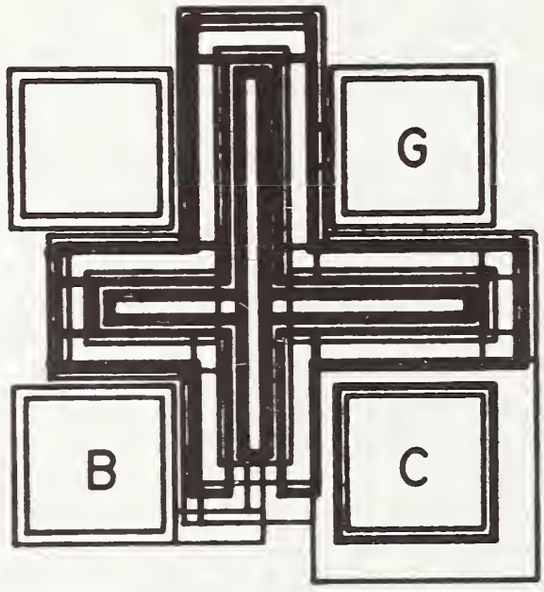
The presence of hairline cracks in a photovoltaic solar cell can significantly degrade both the power output and the reliability of the cell. A technique based on the laser scanner has been developed to detect these tiny cracks, which frequently cannot be observed visually. In this technique the cell is forward biased during laser scanning either electrically with a current source or optically by shining light on the cell, or by a combination of both methods. The crack is revealed by a change in the slope of the photoresponse signal as the laser beam crosses the crack. In some cases, the magnitude of the photoresponse is different on the two sides of the crack so that there is also an abrupt change in magnitude of the signal as the beam crosses the crack. The photoresponse is displayed on a TV screen to permit visual observation of the cracked region. This technique can also be used to observe and identify regions of the grid metallization of a solar cell which are not in good contact with the cell emitter region (that portion of the cell between the p-n junction and the illuminated surface). Analysis of a distributed resistance representation of the solar cell predicts that the photoresponse to a scanning light beam should rise to a common maximum at the edges of the emitter metallization provided that (1) the metallization edge in question is

*NBS Contact.

electrically continuous to the cell leadwire and (2) a good ohmic contact exists between the metallization and the emitter. However, in regions of ineffectual contacting the analysis predicts that the signal should not rise. Observations on cells with known metallization faults confirmed the predictions of the analysis. These results were reported to the 13th IEEE Photovoltaic Specialists Conference in June. [Sponsor: 4](D. E. Sawyer, x3621)

Gated Diodes and CCD Dark Current

Preliminary measurements on a gated diode test structure suggest that this test structure will be useful in revealing unexpected and undesirable effects which impact directly on the performance of CCD imagers. With the addition of an on-chip MOSFET amplifier, which serves as an electrometer, the combined test structure becomes compatible with high-speed dc data acquisition techniques, and the diode dimensions can be reduced to sizes typical of integrated circuit elements. Initial measurements were made on the gated diode test structures on test pattern NBS-12, shown in the figure. These diodes were found to exhibit excess leakage currents at high gate potentials. Due to a geometrical configuration which maximizes the perimeter of the diode and its gate, surface generation occurring at the edges of the depletion layer, where it intersects the $Si-SiO_2$ interface, is enhanced. Zener emission and impact ionization may also contribute at edges or corners. Such excess leakage currents were initially unwelcome. However, it appears that their presence has serendipidously uncovered a likely mechanism for unexpected surface leakage in some CCD designs in which such leakage is likely to be manifested as an undesirable component of dark current in the output gates. Experiments are underway to further understand the nature of this surface leakage and how it depends on the design of the gated diode structure, including such parameters as the length of the gate perimeter, the overlap of the gate and the junction and channel stop diffusions, and the properties of the gate oxide. [Sponsor: 6] (G. P. Carver, x3541)



Computer-generated composite drawing of gated diode on bi-MOS test pattern NBS-12. Contact pads: G, gate; B, p^+ base diffusion (source); C, n-collector region (body).

Silicon Resistivity SRMs

Twenty additional sets of the silicon resistivity standard designated as SRM 1520: Boron-Doped Silicon Slices for Resistivity Measurement have been certified and are now ready for release. This standard reference material consists of two boron-doped silicon single-crystal slices, one with a nominal resistivity of 0.1 Ω•cm, the other with a nominal resistivity of 10 Ω•cm. The slices have a [111] crystallographic orientation and are approximately 42 mm in diameter and 1 mm thick. They are intended for use with four-probe resistivity testers. In addition, twenty more sets of such standards, identical to the above, except that the thickness has been reduced to less than 0.76 mm for use with contactless resistivity gauges in addition to the standard four-probe testers, have also been certified. These sets will be available under the designation, SRM 1521: Boron-Doped Silicon Slices for Resistivity Measurement. The SRM sets may be ordered from the Office of Standard Reference Materials, National Bureau of Standards, Washington,

DC 20234. The cost of each set is $176. [Sponsor: 2] (J. R. Ehrstein, x3625)

Unintentional Ion Channeling Effects

Unintentional channeling during ion implantation can lead to the formation of undesirable deeply penetrating tails in the depth distributions of implanted dopants, especially during low fluence implantations. The magnitude of these dopant tails depends on the angle the ion beam makes with the substrate crystal axes. A joint effort was undertaken with Hughes Research Laboratories to analyze the variation of dopant profiles with the angle of beam incidence. Dopant profiles were determined by differential capacitance-voltage measurements at 1-MHz. The results clearly indicate that the beam must be oriented at an angle with the nearest low-index crystal direction which is at least twice the classical critical angle for channeling in order to minimize unintentional channeling. The critical angles, which were calculated by a simple but accurate procedure, were found to vary from 2 to 7 deg from common industrial implants. Therefore, minimizing the extent of unintentional channeling during implantation requires tilt angles of 4 to 14 deg. These angles can easily exceed the 7- to 10-deg tilt angles commonly used in implantation. These results are being written up as an NBS special publication. [Sponsors: 1,2] (D. R. Myers,* x3625)

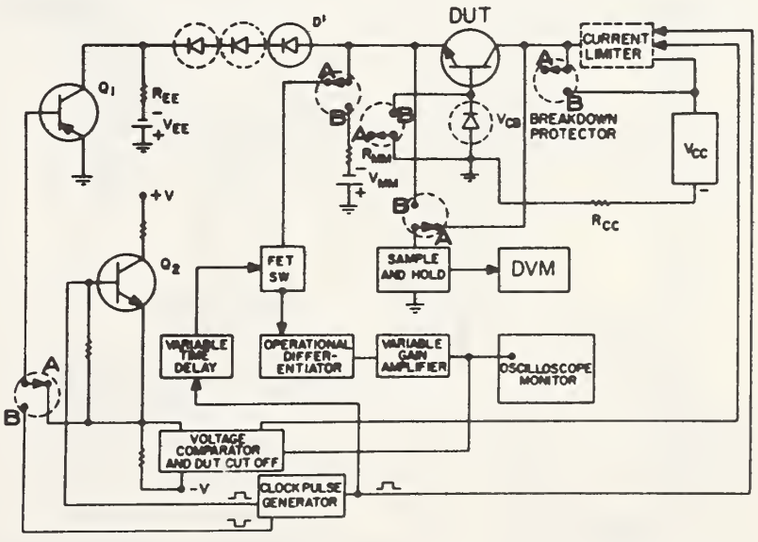
Deep Level Measurements

A comparative study is being initiated so that interested laboratories can assess their ability to accurately measure deep level impurities. In this study, a pair of gold-doped silicon gated diodes is available for measurement of defect energy levels and associated densities and emission rates by each interested laboratory. When sufficient results have been obtained, the measured values and the methods used by the participating laboratories will be compiled. However, the names of the participating laboratories will not be associated with their data in this compilation. It is hoped that this type of interlaboratory comparison will raise the general level of competence in the field of deep level measurements to a point that they will become more effectively and widely used by the semiconductor industry. Laboratories interested in participating in this comparative study should contact the Electron Devices Division, A353 Technology, NBS, Washington, DC 20234. [Sponsors: 1,2,3]

(D. R. Myers,* x3625, W. E. Phillips, x3625, and R. Y. Koyama, x3625)

Transferability of SOA Test Circuit

Safe-operating-area limits of forward-biased bipolar transistors which exclude operation in the hot-spot, or current-constricted, mode can be determined with the circuit shown schematically in the figure. The method involves the measurement of the time derivative of the emitter-base voltage, which shows a well-defined peak at the onset of hot-spot formation. The method and associated circuit were described at the 1977 IEEE Power Electronics Specialists Conference and the 1977 Annual Meeting of the IEEE Industrial



Block diagram of circuit used to generate SOA limit based upon the limit of thermal instability (switches in position A). With switches in position B circuit can be used to measure thermal resistance by the standard method.

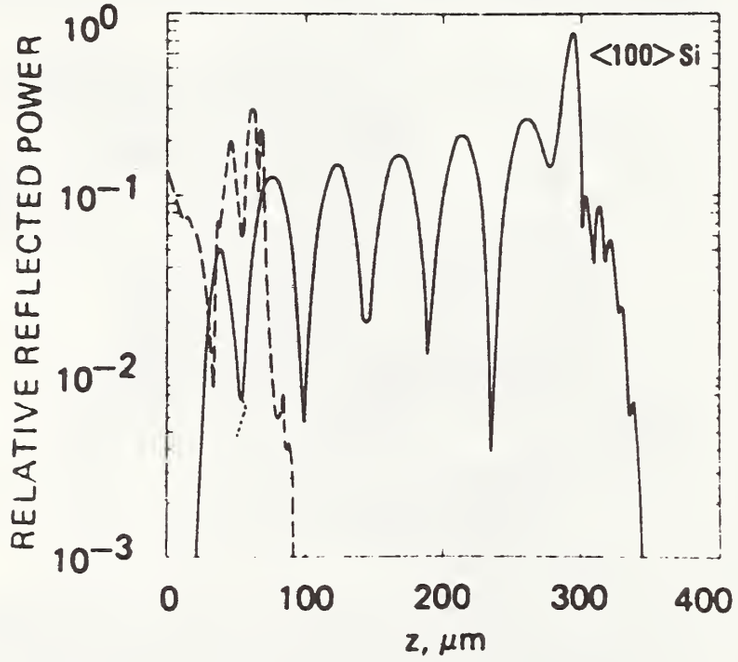
*NBS-NRC Postdoctoral Research Associate.

Applications Society. To aid in implementation of this method, NBS can provide detailed diagrams of the circuit. In addition, several different devices in TO-3 packages are available for circulation to groups who have built the NBS-developed test circuit so that they may evaluate their circuits. If enough organizations take advantage of this opportunity, the data will be summarized to establish an estimate of the interlaboratory reproducibility of the method. Groups desiring information on the method or to obtain the test devices should contact the Electron Devices Division, A353 Technology, NBS, Washington, DC 20234. [Sponsor: 2] (D. L. Blackburn, x3621)

Acoustic Material Signatures

Scanning acoustic micrographs of integrated circuits not only show a large range of contrast between adjacent details in the field of view, but the contrast can be varied or even reversed if the distance from the lens to the specimen is changed. To understand why this occurs, the acoustic reflectance of a variety of materials as a function of lens-to-specimen spacing has been measured at Hughes Research Laboratories. Each material so far examined has a unique reflectance characteristic, frequently with a number of strong minima whose depth and spacing differ for each. These minima are believed to arise because surface waves are excited in the material, and at specific lens-to-specimen distances destructive interference occurs between the normal acoustic return from the specimen and energy re-radiated from the surface wave. Since the velocity of propagation of surface waves is characteristic of the material, and also depends on the direction of propagation in the material, the reflected energy versus lens spacing response is material dependent. In specimens such as integrated circuits where several materials may be present, the contrast changes can be understood as a superposition of responses of the different materials. [Sponsor: 1]

(R. I. Scace,* x3625)



Acoustic material signature (relative reflected power as a function of lens-to-specimen spacing, z) for <100> surface of silicon.

Availability of Test Pattern NBS-4

Documentation for microelectronic test pattern NBS-4 is now available as NBS Special Publication 400-32 in the Semiconductor Measurement Technology series. The NBS-4 pattern contains 38 test structures such as planar four-probe resistors, sheet resistors, MOS capacitors, *p-n* junctions, bipolar and MOS transistors, Hall effect device, and etch control and resolution structures. The overall pattern is a square 200 mil (5.08 mm) on a side and is divided into four quadrants which are separated by scribe lines. This pattern was designed principally for use in measuring resistivity and dopant density of *n*- and *p*-type silicon slices with resistivity from 10^{14} to 10^{20} Ω·cm at room temperature. It has been used both at NBS and at the University of Florida in studies to relate resistivity, carrier density, and dopant density in silicon. The structures contained on the pattern are, like those on earlier test patterns NBS-2 and NBS-3, also of value for measuring parameters in setting up and controlling processing of semiconductor

*NBS Contact.

devices. The earlier mask sets have been released to over 50 government, industrial, or academic laboratories. Requests for releasing the mask set for test pattern NBS-4 from a commercial mask-making company may be addressed to M. G. Buehler. The cost of a mask set is about $200. [Sponsors: 1,2] (M. G. Buehler, x3541 and W. R. Thurber, x3625)

Moisture Measurement Workshop

The fifth in a series of ARPA/NBS workshops concerned with measurement problems in integrated circuit processing and assembly was held at NBS-Gaithersburg on March 22 and 23. The workshop examined present problems with the measurement of moisture in hermetic semiconductor devices, a dangerous and pervasive contaminant. The urgency of these problems is compounded by the recent adoption of moisture measurement test methods in MIL-STD-883. The workshop featured 20 formal talks and several group and panel discussions. The 150 attendees represented a broad spectrum of the semiconductor and related communities concerned with moisture measurement. The measurement approaches addressed in detail were those using mass spectrometers and moisture sensors (aluminum oxide and surface conductivity types). The workshop concluded: 1) for all of the methods used to make measurements in device packages, one can only talk about precision - not accuracy; 2) none of the measurement techniques now available is ready for use by inexperienced personnel; and 3) the precision or repeatability of moisture measurement will not really be satisfactory until much more is done to characterize mass spectrometers and moisture sensors in terms of *all* the variables, conditions, and applications that can affect the measurement. During the workshop, about 60 workshop attendees signed a formal request to NBS for assistance in moisture measurements, especially with respect to traceable standards. In addition, there were numerous expressions of interest in subsequent workshops on moisture measurement. [Sponsor: 1] (H. A. Schafft, x3625)

SPV-PCD Lifetime Comparison

An investigation showed that bulk crystal damage near the semiconductor surface can lead to the often observed discrepancy between the bulk carrier lifetimes measured by the surface photovoltage (SPV) and photoconductive decay (PCD) methods. Both PCD and SPV measurements were made on high resistivity ($\sim$100 $\Omega \cdot$cm), high lifetime (0.1-1.0 ms) silicon slices. The lifetimes as measured by the PCD method on lapped and chem-mechanically polished specimens were consistently one to two orders of magnitude longer than those measured by the SPV method. Also, the SPV plot (intensity, I, versus reciprocal absorption coefficient, α^{-1}) was not linear as required by theory but was concave downward for α^{-1} greater than about 100 μm. All of the assumptions of the SPV theory concerning specimen thickness with respect to α^{-1} and diffusion length were met. A theoretical analysis showed that the I versus α^{-1} data could be qualitatively explained by a two-lifetime model: a short lifetime near the surface and a long lifetime deeper within the bulk. It was found that after removal of the short-lifetime surface region by etching in a solution of 10 parts hydrofluoric acid, 6 parts of nitric acid, and 4 parts hydrochloric acid the SPV data showed the expected linear relationship, and the value of lifetime measured by the SPV method approached that measured by the PCD method. [Sponsor: 2]

(D. L. Blackburn, x3621)

New Projects . . .

Photoresist Adhesion - A study of photoresist-substrate adhesion mechanisms has been initiated. Experiments are being conducted to determine the effect of a silica surface on the chemistry of the photoactive component of negative resist. In addition, model polymers are being synthesized. These will be used to determine the relationship between polymer adsorption and film adherence. [Sponsor: 2] (J. A. Hinkley,* x3621)

*NBS-NRC Postdoctoral Research Associate.

Hydrogen Contamination in Thermal Oxides — Work has been initiated on analyzing the mechanisms through which hydrogen and hydroxyl impurities become incorporated into thin, thermally grown silicon dioxide films prepared in "dry" oxidation atmospheres enclosed in resistance-heated fused silica or silicon furnace tubes. Calculations of the hydrogen content in silicon dioxide films suitable for producing radiation-hardened MOS devices will be made in comparison with the available experimental results. Previous work indicates that environmental conditions such as the substrate, the purity of the oxidation atmosphere, and the furnace tube quality directly affect film composition and properties. The amount of water contamination in a typically nominally "dry" oxidation atmosphere, using electronic grade oxygen with no special preoxidation treatment, enclosed in a fused silicon tube at 1000°C is about 20 ppm. Consequently, the hydrogen and hydroxyl impurities in thin silicon dioxide films can probably be explained in terms of the water introduced into the oxidation atmosphere with the "dry" oxygen. This and other possible mechanisms will be examined quantitatively. [Sponsor: 5]

(S. Mayo, x3625)

Standard Reference Materials — A third standard reference material for four-probe resistivity measurements is being produced in order to provide the high-power semiconductor device industry with silicon slices of calibrated resistivity. The set will consist of three slices of neutron transmutation doped silicon with nominal room temperature resistivities of 25, 75, and 180 Ω·cm. The slices are 51 mm in diameter and 0.64 mm thick.

In addition, a study has been undertaken to determine the effect of storage on the stability of the calibration value of thermally grown oxide on silicon to serve as standard reference materials for measurement of oxide film thickness. Silicon slices were thermally oxidized to form a silicon dioxide layer about 50 nm thick. Groups of four slices each are being stored under one of seven test conditions. The thickness of each oxide film is being measured ellipsometrically on a periodic basis to establish the short-term (∿2 weeks) and long-term (∿6 months) stability of the thickness. A similar set of tests is also to be run on 100-nm thick oxides. [Sponsor: 2] (J. R. Ehrstein, x3625)

Hall Measurements in Two-Layer Structures — In many cases it is desired to characterize by means of Hall effect and resistivity measurements two-layer structures in which there is a p-n junction at the interface. In general, the junction must be considered to have a finite, nonzero impedance which couples the two layers together and thus interferes with conventional Hall measurements. To meet the need for nondestructively characterizing such structures, a modification of the conventional Hall technique is being studied. In this modification which requires ohmic contacts to both layers, Hall measurements are made simultaneously on both layers, and the interface impedance is measured and taken into account. The equations necessary for analyzing the results of the measurements have been developed, and experimental tests of the method are being initiated. [Sponsor: 7]

(R. D. Larrabee, x3625)

CMOS/SOS Test Pattern — Work has begun on designing a test pattern (NBS-16) to develop process assessment methods which can be used by an independent source to evaluate the electrical performance, radiation tolerance, and yield potential of LSI circuits fabricated with a radiation-hardened, silicon-gate CMOS/SOS process. The project is being carried out in collaboration with the Jet Propulsion Laboratories and RCA. NBS and JPL are designing the test pattern. After fabrication of the pattern by RCA under an AFAL contract, NBS and JPL will measure and evaluate the pattern. [Sponsor: 8]

(L. W. Linholm, x3541)

Work in Progress . . .

Hall effect and resistivity measurements on silicon specimens with phosphorus dopant densities in the range 10^{19} to 10^{20} cm^{-3}, being made as part of the reevalua-

tion of the resistivity-dopant density relations in silicon now nearing completion, suggest that for a given dopant density the resistivity is 5 to 10 percent lower than that given by the Irvin curve. [Sponsor: 1] (W. R. Thurber,x3625)

The feasibility of using plasma etching to form mesa diode structures for deep-level measurements on partially or fully fabricated thyristor wafers was demonstrated. With an available etch rate of about 40 μm/h, mesa structures were routinely fabricated with a moat-etch as deep as 80 to 90 μm, which is compatible with junction depths in commercial thyristor structures. Studies have been initiated to determine the optimum technique for making contact to the high resistivity *n*-type region and for optimizing the size of the mesa diodes to compensate for lateral etching during mesa formation. [Sponsor: 3] (R. Y. Koyama, x3625, and J. Krawczyk, x3541)

Calibration of ten artifacts to be used in the interlaboratory evaluation of the line-width measurement procedure was completed. Following revision of the test instructions to incorporate calibration procedures for direct-reading TV-type microscope measuring instruments, the artifacts were distributed to the ten participants. [Sponsors: 1,2](J. M. Jerke, x2185)

Various limitations of the dc MOSFET method for measuring dopant profiles were analyzed. It was found that the principal limitations were those associated with the fact that, as in high-frequency capacitance-voltage methods, the dopant density is measured within the depletion layer so that profiles can be measured only where the material can be depleted of holes and electrons. Thus, the region from about three Debye lengths from the oxide-silicon interface to a depth limited by avalanche breakdown in the silicon can be profiled by these methods. [Sponsors: 1,5] (M. G. Buehler, x3541)

The ultraviolet reflectance technique, developed at RCA Laboratories to evaluate silicon films epitaxially grown on sapphire, has also been shown to be sensitive to surface damage on polished silicon wafers cut from single-crystal boules. [Sponsor: 1] (K. F. Galloway,* x3625)

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report provides information on the current status of NBS work in measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: profiling of the Si-SiO_2 interface by Auger electron and x-ray photoelectron spectroscopies; use of the laser scanner to detect hairline cracks in solar cells; use of gated diodes in evaluation of CCD imager wafers; availability of silicon resistivity standard reference materials; observation of unintentional channeling effects in low-fluence random equivalent ion implantations; initiation of a comparative study of deep level measurements; implementation of the NBS-designed circuit for determining safe-operating-area limits of forward-biased transistors; observation of acoustic material signatures; availability of test pattern NBS-4; conduct of a workshop on moisture measurements; and comparison of carrier lifetimes as measured by the surface photovoltage and photoconductive decay methods. In addition, brief descriptions of new and selected on-going projects are given. The report is not meant to be exhaustive; contacts for obtaining further information are listed. Compilations of recent publications and publications in press are also included.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

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