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Government sponsored research and development on semiconductor devices intended for application in radiation environments often relies on test structures arranged into test patterns for device design information and process characterization. Problems unique to a radiation environment are often analyzed using test structures such as MOS capacitors and break-out transistors. The work reviewed in this report clearly demonstrates the importance of test structures in isolating and identifying problem areas. However, the measurement methodology associated with test structures is seldom reported which makes it difficult to compare the results of different workers. Also, the work reported to date using test structures and test patterns for assessing radiation effects has involved the relatively slow-speed laboratory testing of statistically insignificant numbers of test structures. Test patterns could be used by buyers of radiation hardened devices for (1) vendor selection and qualification, (2) process validation for hardness screening and hardness assurance, and (3) identification of circuit parameters critical to hardness assurance. However, before this can effectively be done, it is necessary that standardized modular test structures be designed to permit measurement of parameters of known importance to device hardness, that test structures be measurable with high-speed integrated circuit testers so that significant numbers can be measured, and that the data reduction and analysis routines be well established.

1. Introduction

Test patterns are widely used in the semiconductor industry for characterization and control of the process used in the manufacture of semiconductor devices. These patterns take many different forms and are used and tested in a variety of ways. In general, these patterns are made up of test structures designed to evaluate a specific process step or sequence of process steps, to obtain circuit performance information, and to assess potential circuit reliability problems. Designers and manufacturers of radiation hardened devices typically use test structures and test patterns for all of these purposes. In addition, specific test structures are often utilized to evaluate and isolate problems unique to radiation hardening and to degradation or failure in a radiation environment. However, additional work is necessary to effectively take the information available from test structures and test patterns from the research and development phase to the production phase of hardened devices.

The purpose of this report is to elucidate the developments necessary to make test patterns effective for (1) vendor selection and qualification, (2) process validation for hardness screening and hardness assurance, and (3) identification of circuit parameters critical to hardness assurance. After briefly reviewing some of the general attributes of test structures and test patterns, this report reviews some of the reported applications of test structures and test patterns in assessing radiation effects and in developing hardened device fabrication processes. Also, the possible future applications of test patterns in the manufacture of radiation hardened semiconductor devices are discussed.

2. General Attributes of Test Structures and Test Patterns

At least four arrangements of test structures on a wafer are commonly encountered. One arrangement consists of an expanded metallization test chip where the microcircuit metallization has been altered to allow access to circuit elements such as transistors and resistors. These chips are often used in circuit design and yield analysis. A second arrangement is a process analysis test chip with specially designed test structures for process control, yield, and reliability analysis. A third arrangement consists of test structures such as test transistors placed on the periphery of every microcircuit chip and used primarily for process control. The fourth arrangement is where the entire wafer is composed of test patterns; this is called a process validation wafer.

The kinds of test structures may vary from clear areas for etch control to patterned areas utilized in various ways. Alignment and resolution patterns are used in photoresist operations and for etch control. Process control structures fall into two categories: those that can be probed before wafers are metallized and those probed after metallization. Those probed before metallization are used to provide rapid feedback to the process. For example, the gain of a transistor

can be brought into specification by additional heat cycles prior to metallization. Those structures probed after metallization are used to monitor the process by giving overall trends and allowing for longer range corrective action. Such structures are typically sheet resistors, contact resistors, metal continuity resistors, test diodes, and test transistors. These process control structures are used to evaluate the process parameters, yield loss mechanisms, and reliability of microcircuits. In contrast to process control structures, circuit and device oriented test structures are useful to the design engineer since they give him information relative to the overall design. They consist of the various resistors, capacitors, diodes, and transistors found in the microcircuit.

There have been several publications describing test patterns and test structures and detailing their application to a variety of problems.[1-9] A special workshop[10] on test patterns for integrated circuits was conducted under ARPA/NBS sponsorship in 1974.

3. Uses of Test Structures and Test Patterns in the Assessment of Radiation Effects

Test structures and test patterns are frequently used for the evaluation of process variations aimed at device hardening and for isolating specific phenomena in radiation effects testing. These test structures vary from diffused resistors to simple inverter circuits. The testing required ranges from complicated high-frequency ac testing on specially packaged structures to high-speed dc wafer probe measurements. Three aspects of the examples in the following paragraphs are especially important to consider for future test vehicle applications: (1) the speed with which test structure measurements can be made; (2) the test structure testability; and (3) the success with which test structure parameters are related to radiation effects.

3.1 Metal-Oxide-Semiconductor Technologies

Probably the most familiar and most widely used special test structure for studying radiation related problems is the metal-oxide-semiconductor (MOS) capacitor. The sensitivity of critical silicon dioxide layers and of the silicon-silicon dioxide interface region to ionizing radiation damage is a problem in the development of both radiation hardened MOS integrated circuits and radiation hardened linear bipolar integrated circuits. Two phenomena are important for understanding this ionizing radiation damage: the accumulation of trapped charge in the silicon dioxide and the creation of additional interface states at the silicon-silicon dioxide interface. MOS capacitors are used to measure trapped charge and interface-state densities in oxides before irradiation and to assess the effects of radiation on these quantities. MOS capacitors have also been widely used as an evaluation tool in the development of processes for fabricating radiation hardened MOS circuits. It should be pointed out that the measurements on this test structure take several minutes per device and that they are not amenable to testing

in a high speed wafer probe mode. Also, the results represent an average over an area of the wafer which is much larger than the gate area of an MOS transistor.

The applications of MOS capacitors as test structures have been so extensive that a comprehensive review is impractical here; however, the several examples mentioned briefly in the following paragraphs indicate the importance of this test structure. The reports cited also contain references to other reports giving details on MOS capacitor measurements.

In an investigation of chromium-doped oxides, MOS capacitors were part of a test chip used by Kjar[11] for radiation hardness studies. Aubuchon, Harari, and Chang[12] utilized MOS capacitors to study the effects of HCl gettering, chromium doping, aluminum ion implantation, and polysilicon gate electrodes on gate oxide hardness. MOS capacitors were the principal test structures used by Sah[13] in a program to study the properties of process-induced interface states and their relation to radiation-induced interface states. Srour *et al.*,[14] in studying the basic mechanisms involved in the charge transport and charge buildup in silicon dioxide, utilized MOS capacitors as their test vehicle.

MOS capacitors were utilized in an effort to optimize the processing of aluminum-gate radiation-hardened CMOS integrated circuits described by Derbenwick and Gregory.[15,16] The effects of low-temperature processing (pre-oxidation silicon conditions, cleans, and rinses; and post-oxidation photoresist steps) and high-temperature processing (oxidation, annealing, and sintering) on oxide radiation resistance were evaluated using measurements on MOS capacitors. The capacitors were characterized before and after irradiation using high-frequency (1 MHz) and quasi-static capacitance-voltage measurements. These measurements contributed to the development of a reproducible and controllable baseline process for the fabrication of hardened CMOS integrated circuits using dry thermal oxides which was then demonstrated by fabricating CMOS 4007 inverters.

One of many problems in the development of radiation-hardened MOS devices on sapphire substrates is understanding the effects of radiation on the silicon-sapphire interface. Goodman[17] has extended the use of MOS capacitor test structures to capacitance-voltage measurements on metal-sapphire-silicon structures. These back-gate measurements serve as a process control monitor in determining the effect of various fabrication steps on the state of the silicon-sapphire interface and establish in the most direct way the influence of ionizing radiation on the interface charge of silicon-sapphire interfaces.[18]

In work conducted by Kjar and Kuhlman[19] directed at optimizing the radiation hardness and reliability of CMOS/SOS circuits, test structures for measurement of device and processing parameters were incorporated into a test pattern. This pattern is interesting in that large oxide areas suitable for impurity measurements using ion microprobe mass analysis were included. Also, MOS capacitors were included for measurement of electrical and radiation damage parameters. The resulting

pattern was intended for evaluation of state-of-the-art SOS device fabrication and to facilitate investigation of problems such as island edge anomalies associated with *n*-channel devices.

In a program intended to determine the applicability of MNOS devices to systems requiring radiation hardening,[20] test structures were used to evaluate five basic types of MNOS process sequences. The test structures contained memory and nonmemory capacitors and transistors of various designs. All constituent parts required for the fabrication of fully decoded memory arrays on either bulk silicon or silicon on sapphire were tested through total dose and dose rate environments. The test structures allowed the identification of fabrication sequences for devices which would satisfactorily withstand a total dose of approximately 10^6 rads(Si) and dose rates of approximately 10^{11} rads(Si)/s.

In order to evaluate techniques for protecting CMOS circuits against EMP threats, Stewart and Hampel[21] developed an extensive EMP test chip. The test chip included structures useful to studying five specifically identified failure mechanisms: melting of metallization, interconnects, buried heat failure, stepped oxide failures, inadequate clamping effectiveness, and junction failure. Several experimental protection devices, control devices, and logic gates protected with a diode clamping circuit were included on the test chip. The application of this EMP test chip contributed to the understanding of the mechanism by which electrical transients damage CMOS integrated circuits and to the design of more effective devices for protecting integrated circuits against voltage transients.

3.2 Bipolar Technologies

The gate controlled bipolar transistor or diode is a test structure frequently used for studying surface effects.[22,23] It is used to obtain information on surface recombination velocity, fast surface state density, and the charge carrier capture cross-sections of the fast surface states. The measurements on these devices are laboratory bench-level tests requiring minutes to complete. Sivo, Hughes, and King[24] used a gate controlled bipolar transistor and an MOS capacitor on the same silicon chip to study the ionizing radiation dose dependence of the capture cross-sections and interface states. Sivo[25] used gate controlled measurement techniques to study the relative roles of the radiation-induced interface states and trapped oxide charge on the surface degradation of *npn* planar transistors.

Specially designed test patterns and MOS capacitors fabricated on pilot wafers have been used in programs directed at improving the radiation hardness of bipolar linear circuits. In work described by Lee,[26] modifications of a standard test patterns used in the fabrication of an uncompensated precision operational amplifier using super-beta transistors were described. The standard test pattern consisted of test structures by which the sheet resistances of the various diffusions and the betas, breakdowns, etc., of the transistors could be measured. This pattern was modified with the addition of a *pnp* substrate transistor,

an MOS capacitor, and a gated diode to gain information on process control and process variation related to the hardening effort. Radiation effects on the test structures have been studied by Sivo.[27] The correlations between these results and the testing of the amplifiers themselves, which will hopefully yield an understanding of the effects of variations in processing on the radiation susceptibility of the operational amplifiers, have not yet been reported.

Test structures have also been used in other programs aimed at improving bipolar survivability in total dose environments. In one effort, surface sensitive test devices were used in an attempt to develop screens for bipolar transistor degradation due to ionizing radiation.[28] The data developed in this program showed only limited success in this particular application of test structures; however, this might be due to lack of a statistically significant set of data. Another program applied MOS hardening techniques to bipolar device hardening.[29] An expanded metallization type test pattern for a 741 type operational amplifier was utilized to evaluate the hardening effects of process variations in oxide growth conditions, annealing cycles, and methods for aluminum evaporation. Slight improvements in total dose tolerance were achieved.

The effects of radiation on bulk properties of semiconductor devices can also be effectively studied with test structures. Smith and Hahn[30] used a specially designed test pattern to examine the correlation between post-irradiation bipolar transistor gain and pre-irradiation electrical parameters to determine a screening parameter for neutron hardness assurance. A high correlation of post-irradiation, saturated current gain with pre-irradiation collector resistance was observed. In further work, a collector test resistor incorporated on each chip of a power transistor was used as a hardness assurance screen with good results. Use of this test structure to measure collector resistance as a neutron hardness assurance screen was suggested as being applicable to any bipolar transistor, discrete or integrated, in which the effect of collector resistance on post-irradiation current gain is predominant. Measurements on this particular test structure can be made at the wafer level using the high-speed dc probe equipment typically used by device manufacturers.

A specially designed test chip was used by Fossum *et al.*[31] to examine the feasibility of using diffused resistors in dielectrically isolated integrated circuits. The test chip was used for experimentally determining the effects of ionizing radiation on diffused resistors fabricated according to this technology and as an aid in developing guidelines for radiation-hard, diffused resistors.

The decrease in gain of internal transistors is the primary degrading effect of neutron irradiation on TTL integrated circuits. Depending on the sensitivity of the circuit requirement, terminal measurements may be inadequate for fully assessing potential radiation susceptibility. In order to evaluate various parameters and analytical techniques as screens and controls for the radiation behavior of TTL integrated

circuits, Johnston and Skarland[32] compared three different approaches for neutron hardness assurance prediction. These were: (1) measurements using leads normally available with a packaged device; (2) measurements using special internal connections to the circuit which were provided by a modified metallization pattern; and (3) measurements on a breakout transistor which was available for each circuit with the special metallization from one of the gates on multiple gate devices. The latter two approaches are classified as test structure or test pattern methods. Rank correlation and linear regression techniques were used to assess the ability of these approaches to predict the radiation response of a large group of similar devices from a given production run or diffusion lot from measurements made on a sample. The prediction accuray was significantly improved for the circuit types on which test structure/test pattern measurements could be made. For example, the rms prediction error of one type of inverter circuit was reduced from 158% using terminal measurements to 9% when expanded metallization measurements on the output transistor were used. This example points to the power of the test structure concept for predicting circuit behavior. Both the measurements on transistors available through the modified metallization scheme and on breakout transistors were superior to terminal measurements for radiation hardness prediction. It was found that base-emitter forward bias voltage, V_{BE}, at a fixed value of collector current, I_C, measured for either of these transistors was a very good predictor of neutron damage in all of the device types studied. These test structure measurements described by Johnston and Skarland are compatible with high-volume dc wafer prober measurements and could be included in the qualification specification of devices intended for hardened systems.

3.3 Summary of Reported Work

In the preceding paragraphs, a number of examples of the application of test structures and test patterns in assessing a variety of radiation related questions have been cited. These activities have made a significant contribution to the development and evaluation of radiation hardened semiconductor devices. Without question, special test structures will continue to be used in the development of processes for the fabrication of radiation hardened devices and for the assessment of specific radiation effects.

Even though the application of test vehicles has met with a number of important successes, several factors interfere with wider usage and usefulness. In most instances reported, very little documentation is available which would allow others to use specific structures developed. Measurement details and reproducibility of measurements typically remain unaddressed. Often, the adequacy of a structure for evaluating a particular effect or problem cannot be ascertained from the information supplied. Efforts aimed at determining the adequacy, reproducibility, and appropriateness of methods of measurement for the test structures used along with design details need to be included to facilitate the use of test structures by both buyers and sellers. Also, a factor which can inhibit the use of test vehicles in a production environment is the speed

with which the test structure measurements can be made. Most of the results reported are based on relatively slow laboratory tests of small numbers of devices.

4. Future Applications of Test Patterns in the Production of Radiation Hardened Devices

Research and development phases of radiation hardened device development will continue to rely on the measurement information available from test vehicles in many of the modes of usage described in Section 3. If test structures and test patterns are to make the transition from this mode of application to a mode useful in the production phase of radiation hardened devices as a specification and assessement tool by the purchaser of these devices, several tasks need to be addressed.

The relationship between the behavior of devices in a radiation environment and measurements made on test structures needs to be firmly established. Test structures are extremely valuable in assessing the degree to which a manufacturer controls specific processing steps. The steps crucial to device radiation response and the allowable variation as determined from test structure parameters must be understood. Work on evaluating the relationship between the test structure parameters and device radiation behavior must be undertaken if a set of applicable structures, the appropriate parameters, and the necessary controls are to be defined for a given fabrication technology.

If the test structures are to be effectively applied to hardness screening and assurance in a production situation, they must be amenable to high-speed dc probe testing at the wafer level. Many of the structures now available or under development can be measured in this way. However, some of the parameters proposed for hardness screening and assurance will require the rapid measurement of low level currents, low level voltages, or both. These parameters are not currently measurable during high-speed wafer probe. This measurement problem can be overcome with the development of advanced test structures[33] which incorporate appropriate integral signal processing circuits. The development of these advanced test structures is particularly important if surface sensitive parameters related to total dose screening are to be measured accurately, quickly, and economically in a production environment.

Another aspect of test pattern application important from the buyer's perspective is standardization. Without standardization, each test pattern becomes a new adventure in design. This leads to unproven test structures and to uncertainty when comparing results from different test patterns. There are many examples of seemingly minor modifications to proven test structures which have negated the usefulness of the test structure. In addition to fixing the test structure design and its associated measurement and data reduction methods, the probe pad location and metal interconnections to the test structure cannot be left to the discretion of the individual designer. Constraints are necessary if well-characterized and standardized test structures are to be used effectively at the buyer-seller interface.

A key to the full utilization of test patterns is a modular arrangement of probe pads within test cells which allows the use of standardized test structures.[34] The test pattern is organized in a hierarchy whose smallest part is the test structure. These structures form test cells which comprise the test pattern. Modularization is crucial to test pattern design layout and testing strategies. Ultimately, it should be possible to assemble selected structures from a computerized library into a test pattern tailored to address the needs of a particular process or fabrication technology.

Future application of test patterns to hardness screening and hardness assurance in the production of semiconductor devices will be best accomplished through standardized modular test structures designed to measure parameters of known importance to device hardness which can be measured by high-speed wafer probe equipment. The availability of test patterns with these attributes would assist buyers of radiation hardened devices in vendor selection and qualification. Once devices are in production, these patterns can be used by the buyer to assure that the aspects of the process crucial to his requirements remain within his predetermined limits.

5. Conclusions

Test patterns have been used extensively and effectively in government-sponsored research and development work related to hardened semiconductor devices. This work has been important for the development of hardened designs and processes. The use of test patterns promises to be a cost effective method for obtaining high reliability semiconductor devices for application in radiation environments. However, there is much developmental work to be done on test structures and test patterns if they are to function as hardness screening and assessment measurement tools in the production of devices. The preceding sections have pointed to some of the problems which must be solved if this tool is to be made available for hardness assurance tasks in the procurement of devices.

6. References

1. Barone, F. J., and Myers, C. F., Getting Beneath the Surface of Multilayer Integrated Circuits, *Electronics* 41 (No. 15), 84-88 (1968).

2. Schlegel, E. S., and Schnable, G. L., The Application of Test Structures for the Study of Surface Effects in LSI Circuitry, *IEEE Trans. Electron Dev.* ED-16, 386-393 (1969).

3. Sahni, R. J., Use of Test Patterns in Evaluating the Reliability of Integrated Circuits, *8th Ann. Proc., Reliability Physics*, Las Vegas, Nevada, April 7-10, 1970, pp. 226-231.

4. Van Vonno, N. W., Reliability Assurance by Test Vehicle Qualification, *Proc. 22nd Electronic Components Conf.*, Washington, D. C., May 15-17, 1972, pp. 463-466.

5. Dell'Oca, C. J., Bipolar Processing and Production Control, Mini-Symposium on Semiconductor Test Patterns, *ASTM Committee F-1 on Electronics*, January 1974 (unpublished).

6. Poblenz, F., King, D., and Martin, K., Applications of Test Patterns, Mini-Symposium on Semiconductor Test Patterns, *ASTM Committee F-1 on Electronics*, January 1974 (unpublished).

7. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974).

8. Buehler, M. G., David, J. M., Mattis, R. L., Phillips, W. E., and Thurber, W. R., *Semiconductor Measurement Technology:* Planar Test Structures for Characterizing Impurities in Silicon, NBS Spec. Publ. 400-21 (January 1976).

9. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, NBS Spec. Publ. 400-22 (June 1976).

10. Schafft, H. A., Ed., *Semiconductor Measurement Technology:* ARPA/NBS Workshop III. Test Patterns for Integrated Circuits, NBS Spec. Publ. 400-15 (January 1976).

11. Kjar, R. A., Investigation of Chromium-Doped Oxides, *Rockwell International Final Report* (Contract No. N00014-72-C-0017), November 1973.

12. Aubuchon, K. G., Harari, E., and Chang, P., CMOS Radiation Hardening, *Hughes Aircraft Company Annual Report* (Contract No. N00014-72-C-0424), October 1974.

13. Sah, C. T., and Sah, L. C., Effects of Ionizing Radiation on the Characteristics of Metal-Oxide-Semiconductor Structures, *Harry Diamond Laboratory Report*, HDL-CR-75-013-1 (April 1975).

14. Srour, J. R., Curtis, O. L., Jr., Othmer, S., and Chiu, K. Y., Radiation Effects on Oxides, Semiconductors, and Devices, *Harry Diamond Laboratory Report*, HDL-CR-75-171-1 (May 1975).

15. Derbenwick, G. F., and Gregory, B. L., Process Optimization of Radiation-Hardened CMOS Integrated Circuits, *IEEE Trans. Nucl. Sci.* NS-22, 2151-2156 (1975).

16. Gregory, B. L., Process Controls for Radiation-Hardened Aluminum Gate Bulk Silicon CMOS, *IEEE Trans. Nucl. Sci.* NS-22, 2295-2302 (1975).

17. Goodman, A. M., An Investigation of the Silicon-Sapphire Interface Using the MIS Capacitance Method, *IEEE Trans. Electron Dev.* ED-22, 63-65 (1975).

18. Kokkas, A. G., Cullen, G. W., and Duffy, M. T., Radiation in MOS/SOS Devices, *AFCRL Report*, AFCRL-TR-0610 (February 1976).

19. Kjar, R. A., and Kuhlman, G. J., Radiation Resistance CMOS/SOS Circuitry, *Rockwell International Final Technical Report* (Contract No. N00014-74-C-0416), April 1975.

20. Blaha, F. C., Cricchi, J. R., and Gallager, R. C., MNOS Radiation Device Testing, *Westinghouse Final Technical Report* (Contract No. N60921-74-C-0115), October 1975.

21. Stewart, R. G., and Hampel, D., EMP Hardened CMOS Circuits, *IEEE Trans. Nucl. Sci.* NS-21, No. 6, 332-339 (1974).

22. Snow, E. H., Grove, A. S., and Fitzgerald, D. J., Effects of Ionizing Radiation on Oxidized Silicon Surfaces and Planar Devices, *Proc. IEEE* 55, 1168-1185 (1967).

23. Reddi, V. G. K., Influence of Surface Conditions on Silicon Planar Transistor Current Gain, *Solid-State Electronics* 10, 305-334 (1967).

24. Sivo, L. L., Hughes, H. L., and Kings, E. E., Effects of Ionizing Radiation on Various Devices of a Silicon Hybrid Array: Correlation Studies, *IEEE Trans. Nucl. Sci.* NS-19, No. 6, 313-319 (1972).

25. Sivo, L. L., Relative Roles of Charge Accumulation and Interface States in Surface Degradation (NPN Planar Transistors), *IEEE Trans. Nucl. Sci.* NS-19, No. 6, 305-312 (1972).

26. Lee, F., Improved Radiation Hardness of Bipolar Linear Circuits, *RCA Interim Report* (Contract No. N0014-74-C-0451), 1975.

27. Sivo, L. L., Service for Device Surface Analysis, *Boeing Aerospace Company Interim Report No.* D180-19044-1 (Contract No. N00014-74-C-0306), September 1975.

28. Bruncke, W. C. Crabbe, J. S., Hopkins, G. G., Lipman, J. A., Manus, D. J., and Matzen, W. T., Techniques for Screening Bipolar Transistor Degradation due to Ionizing Radiation, *Texas Instruments Final Report* (Contract No. N00164-73-C-0420), NAD Crane TR/7024/C74/121, November 1974.

29. Crabbe, J. S., Applications of MOS Hardening Techniques to Bipolar Device Processing, *Texas Instruments Final Report* (Contract No. N00164-74-C-0378), NWSC Crane TR/7024/C74/285, July 1975.

30. Smith, D. M. and Hahn, L. A., Neutron Hardness Assurance of Bipolar Transistors by Collector Resistance Determination, *IEEE Trans. Nucl. Sci.* NS-19, No. 6, 125-128 (1972).

31. Fossum, J. G., Sander, H. H., and Gerwin, H. J., The Effects of Ionizing Radiation on Diffused Resistors, *IEEE Trans. Nucl. Sci.* NS-21, No. 6, 315-332 (1974).

32. Johnston, A. H., and Skarland, R. L., Neutron Hardness Assurance Techniques for TTL Integrated Circuits, *IEEE Trans. Nucl. Sci.* NS-21, No. 6, 393-398 (1974).

33. Lonke, M. L. and Turley, A. P., Statistical Analysis of p^+/n Junction Leakage Characteristics for Si-Gate Processed Devices, *Electrochemical Society Extended Abstracts* 75-2, 355-357 (1975).

34. Buehler, M. G., Test Patterns with Modular Cells, Semiconductor Measurement Technology, Progress Report, July 1 to December 31, 1975, Bullis, W. M., Ed., NBS Spec. Publ. 400-25 (to appear).

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