NBSIR 73-302

RF NULL DETECTOR NBS/SND

Robert E. Stoltenberg

Electromagnetics Division
Institute for Basic Standards
National Bureau of Standards
Boulder, Colorado 80302

June 1973

Prepared for
Army/Navy/Air Force
Calibration Coordination Group

NBSIR 73-302

RF Null Detector NBS/SND

Robert E. Stoltenberg

Electromagnetics Division
Institute for Basic Standards
National Bureau of Standards
Boulder, Colorado 80302

June 1973

Prepared for
Army/Navy/Air Force
Calibration Coordination Group

U.S. DEPARTMENT OF COMMERCE, Frederick B. Dent, Secretary
NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, Director

Abstract

This report describes an ultrasensitive receiver for detecting low-level rf signals in the nanovolt region. The primary purpose of the instrument is to detect the balance condition in rf bridges; however, it is useful in any comparison measurement in which two or more signals can be adjusted in phase and magnitude such that their summation results in a null.

The receiver frequency is determined by individual plug-in units. Units have been built for selected frequencies from 100 kHz through 30 MHz. Detection is accomplished by double conversion. The first converts the signal of interest to a common intermediate frequency; the second performs a dual synchronous (homodyne) conversion. The dual detectors are sensitive to signals in quadrature with each other. A reference voltage synchronous with the null signal is required. Thus, the dual detection provides an indication of both the phase and the magnitude of the null unbalance.

The output of each detector is displayed on a zero-center meter, thus indicating the direction of unbalance as well as the magnitude. This information is also available at a rear panel jack for use in servo control of the external system.

Gain adjustment over a 90 dB range is provided by a single front panel control. Phase adjustment to compensate for differential phase delay between the reference and null signals is accomplished with a front panel 360° continuous phase control.

Key Words

Detector; phase sensitive; RF null detector.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF TABLES

NBS RF NULL DETECTOR

(Synchronous Detector)

I. General Information

1.1 Introduction.

This document contains a description, specifications, operating instructions, theory of operation, parts list, schematics, and wiring diagrams for the National Bureau of Standards RF Null Detector, Model NBS/SND. This unit is a general purpose calibration instrument which provides both magnitude and phase information at sensitivities not previously available.

1.2 Description

This unit consists of a main frame detector assembly which accepts individual specific frequency plug in units. The frequency coverage of the Null Detector is thus limited to only those plug in units available. This instrument has been designed for extremely high sensitivity consistent with simplicity of operation. The detector is frequency locked to the signal to be examined and thus requires a synchronous reference voltage. A single gain control adjusts sensitivity. The null signal is indicated by two front panel center-indicating meters. A continuously variable phase control enables in-phase and quadrature components of the null signal to be displayed individually on separate meters.

An additional unfiltered rear panel output is provided directly from the detector which can be used for servo control of external systems.

1.3 Specifications

1.3.1 Frequency Range:

Frequency is determined by plug in units. 100 kHz, 1 MHz, 10 MHz, and 30 MHz units are presently available.

1.3.2 Maximum sensitivity:

Nominally 1 nanovolt.

1.3.3 Dynamic Sensitivity Range:

90 dB.

1.3.4 Phase control:

360° continuously variable.

1.3.5 Total maximum gain to Synchonous detector output:

(for servo control) 150 dB.

1.3.6 Reference Voltage Requirement:

50-500 μv, synchronous with input signal.

1.3.7 VCLO Tracking Range:

Dependent upon plug in, nominally ± 20 kHz.

1.3.8 Noise figure:

2 dB.

1.3.9 Input Impedance:

Nominally 50 Ω Reference and Signal Inputs.

1.3.10 Dimensions:

13.3 cm x 48.2 cm W x 43 cm Deep 10.1 Kg

(5¼"H x 19"W x 17" Deep).

2.0. Operating Instructions

This section contains information and instructions for preparation and use of this instrument in a step-by-step procedure.

2.1 Introduction

The RF Null Detector provides synchronous detection of low level RF signals. The instrument uses double conversion. The first mixer converts the incoming RF signal to the main frame 20 kHz IF frequency. This is accomplished by the frequency plug-in unit which contains a VCLO (Voltage Controlled Local Oscillator) and a preamplifier appropriate for the frequency desired. The second conversion is a homodyne or synchronous converter (Synchronous Detector). The second conversion obtains its reference L.O. (Local Oscillator) from an internally generated 20 kHz signal. All RF cables are semi-rigid with SMA connectors, with one exception, which is a BNC coupler.

2.2 Description of Controls, Connectors, and Indicators

See figures 2.1A and 2.1B for location and description of controls, connectors and indicators.

2.2.1 AC Power.

A_1 AC Power Jack

A_2 AC Power Switch

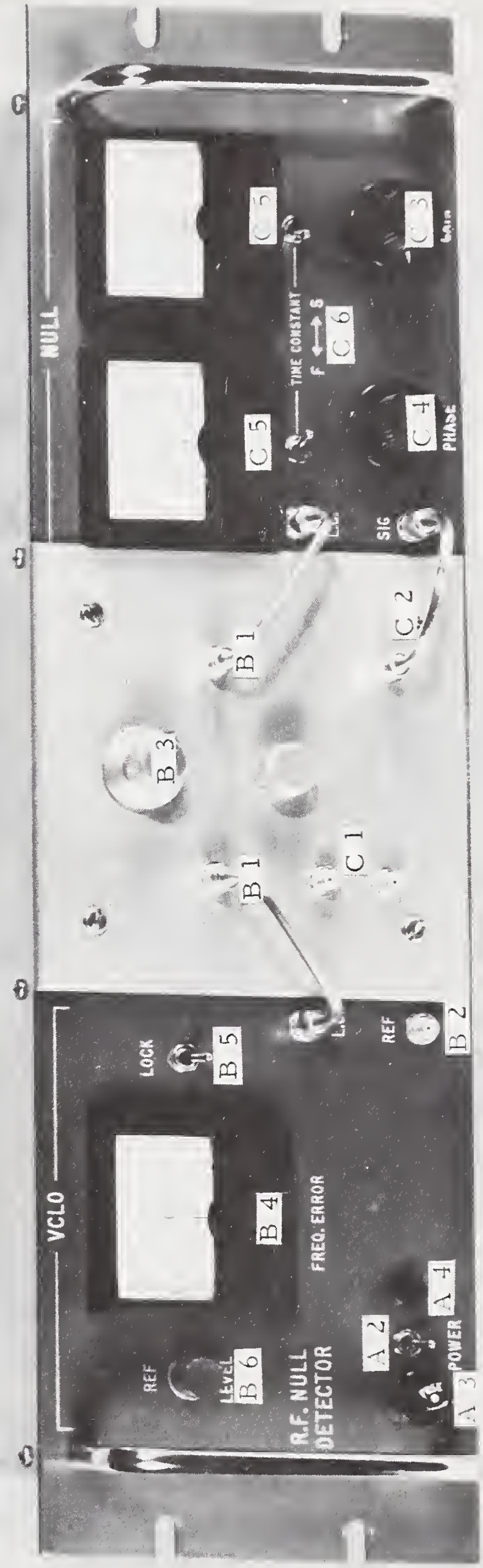


Figure 2.1A. Front panel control and indicator location

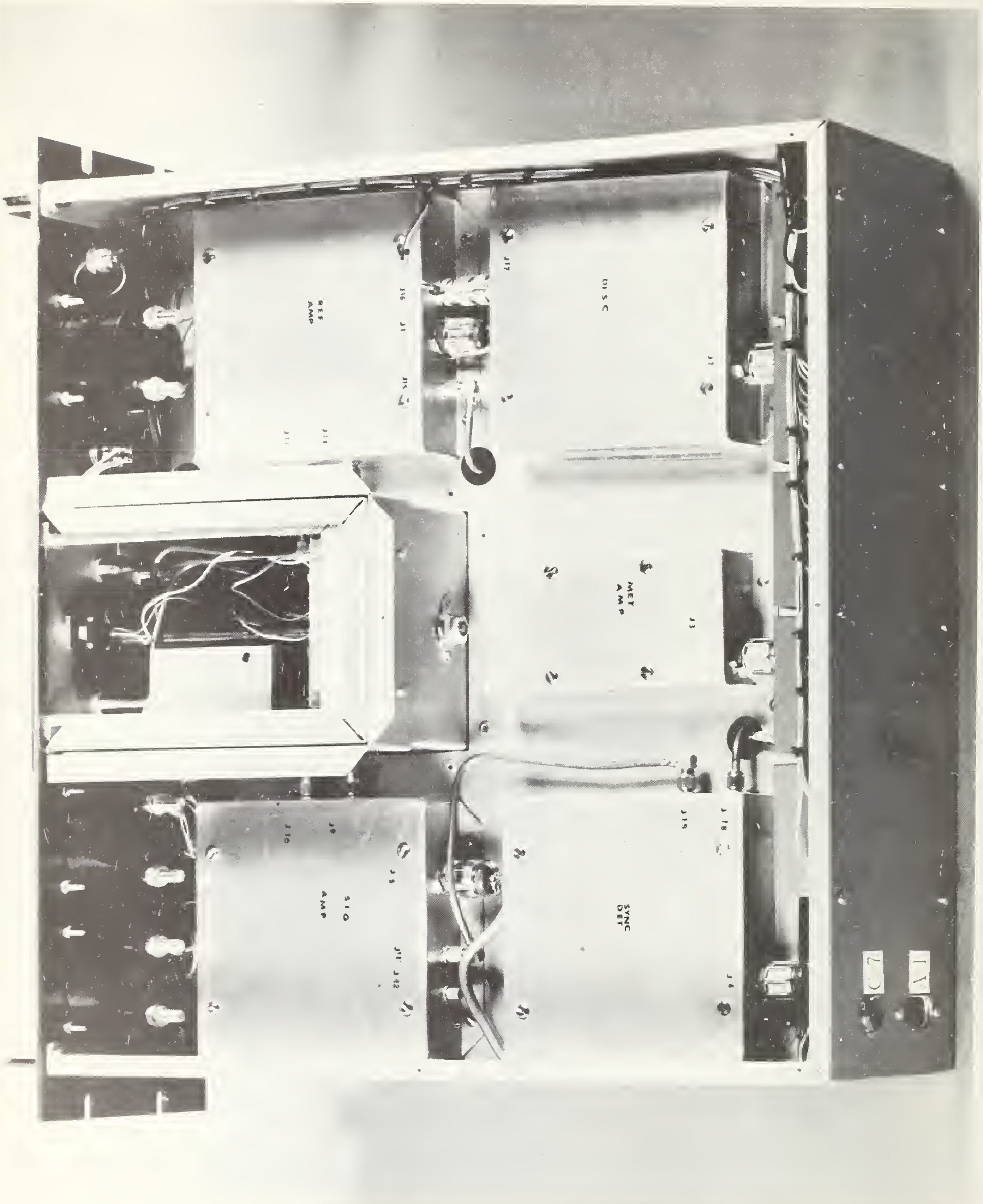


Figure 2.1B. Rear panel connector location

A_3 Fuse (½ A.)

A_4 AC Indicator Lamp

2.2.2 VCLO

B_1 J28-J29 VCLO outputs

Provide RF power to J24-J25 for first mixers.

B_2 J26 Reference Voltage Input

Connects reference voltage to Reference Amplifier Mixer.

B_3 VCLO Trim

Provides small frequency adjustments to VCLO for tuning precisely 20 kHz above incoming reference signal frequency.

B_4 Frequency Error Meter

Indicates frequency difference between VCLO and external reference voltage.

B_5 Lock Switch

Frequency locks the VCLO 20 kHz displaced from the reference signal.

B_6 Reference Level Indicator

Indicates adequate reference signal.

2.2.3 Null

C_1 J31-J39 RF Signal Input. J31 on Model SND/PI-30A Plug-in.

C_2 J27-J30 connects plug-in preamplifier to main frame.

C_3 Gain Control

Provides up to 90 dB attenuation for initial null adjustments.

C_4 Phase Control

Provides 360° continuously variable phase adjustment for the internal synchronous detectors.

C_5 M2-M3

Indicate input voltages. (Nominally ± 5.0 Nanovolts f.s. @ maximum gain setting.) Right-hand meter indicates quadrature voltage (90° phase displaced) with respect to left hand meter.

C_6 S2-S3 (Time Constant)

Control meter response time constant; Fast in left position, Slow in right position (approximately 7:1 ratio).

C_7 J8 Synchronous Detector output (unfiltered)

Pin F proportional to M2 (50 mV/10 μ amps)

Pin K proportional to M3 (50 mV/10 μ amps)

Pin J Ground.

2.3 Operating Procedures

The following steps must be performed to insure accurate and consistent null measurements.

2.3.1 These preliminary connections and checks should be performed prior to applying power.

a. Insure AC power switch is off.

b. Connect AC line cord to J6.

c. Insert appropriate frequency plug-in.

d. Connect the following semi-rigid RF cables (supplied with unit):

<u>MAIN</u> <u>FRAME</u> <u>PLUG</u> <u>IN</u>

Ref to VCLO out. (J24 to J28)

Sig to VCLO out. (J25 to J29)

Sig in to Sig out. (J27 to J30)

<u>WARNING</u>: <u>DO NOT APPLY AC POWER WITH THESE CABLES REMOVED</u>. <u>PRE AMP MAY BE DAMAGED</u>.

e. Lock switch off.

f. Time Constant switches to fast.

g. Gain Control to min (full CCW).

2.3.2 Connect Synchronous Reference Voltage to Ref in, (J26) (Do not exceed 500 μv).

2.3.3 Connect null signals to Sig In (J31). SND/P1-30A contains two inputs (J31-J39)

NOTE: Do not exceed -20 dBm (22 mv).

2.3.4 The following steps are required to insure frequency lock.

a. Turn power on.

b. Adjust frequency trim control until frequency error meter indicates null. Meter should indicate to the right with CW rotation of VCLO trim control. Ref Lamp should be on (indicating sufficient reference signal).

c. Lock switch to Lock.

d. In order to insure VCLO is locked, rotate VCLO Trim Control a small amount. The Frequency Error Meter should indicate right with CW rotation and left with CCW rotation. Re-zero the meter with the trim control.

The VCLO is now locked to the Ref. Voltage and should require no further attention unless the unit has AC power interupted or the Reference signal is lost. The frequency error meter indicates IF frequency deviation from 20 kHz. Meter sensitivity in the locked position is nominally 1 Hz/2 μamp. In the event of large reference frequency drifts resulting in frequency error indication of more than 20 μamps (10 Hz), either the external signal source should be readjusted to the nominal frequency of the plug-in, or the VCLO trim control should be adjusted to re-zero the meter.

Note: The Automatic Frequency Lock response is limited to approximately 100 Hz. A rapid change in the reference frequency can exceed the tracking response of the VCLO, resulting in the loss of frequency lock. This normally results in off-scale frequency error meter fluctuations coupled with blinking of the Ref Level lamp. If this occurs, repeat steps b through d of 2.3.4.

2.3.5 Null Measurement. The primary function of this instrument is to serve as the detector in an RF bridge or dual channel calibration system where the null balance signal is to be reduced to the minimum possible value. In this application a null unbalance in the system can occur as a result of either a differential magnitude or phase change in either of the two signal paths. This instrument provides the capability of distinguishing between the two types of unbalance (magnitude and phase) and, additionally, of indicating the direction of the unbalance by the direction of the meter deflection. The following steps are to be performed to reduce the null signal to a minimum value.

Note: In order to assure there are no external rf leakage paths from the external system, a 50 ohm termination should be connected to the signal input, and the gain turned fully CW. No meter deflection should be observed other than random noise.

2.3.5.1 Rotate the gain control CW until either one or both meters indicate half scale.

2.3.5.2 Alternately adjust the external phase and magnitude controls for zero meter indications.

2.3.5.3 Repeat steps 2.3.5.1 and 2.3.5.2 until the gain control is approximately 3/4 CW.

2.3.5.4 Unbalance the external system a small amount by using its magnitude control. Rotate the null detector phase control until the left hand null indicating meter indicates zero. Adjustment of the external system magnitude control should now be indicated on the right hand meter only. Re-zero the right hand meter with the magnitude control and unbalance the external system by adjusting its phase control. Only the left hand null meter should deflect. Re-zero the left hand meter.

2.3.5.5 Rotate the gain control CW for increased meter deflections (increased sensitivity). Reduce the off-null condition by adjusting the external system as indicated in 2.3.5.4. Repeat quadrature separation (2.3.5.4) adjustment if necessary.

2.3.5.6 Repeat step 2.3.5.5 until maximum desired sensitivity is reached or until an adequate null is achieved.

<u>Note</u>: In order to take advantage of the full sensitivity (1nv/10 μa), it is normally advantageous to switch the meter time constants to "S" when maximum gain is approached to reduce the effects of random noise fluctuations. This also severely restricts the meter response to system changes, thus requiring very slow adjustments in the external system.

3.0. Theory of Operation

The following section contains a functional description of the Null Detector operation. A Circuit description is contained in Section 4.0. See fig. 3.1 for the Block Diagram of the Null Detector. See fig. 3.2 and 3.3 for RF wiring diagrams. The main frame contains six modules plus the power supply board (MPS-1). The plug-in contains two modules and a circuit board containing the VCLO trim and filter components. Some frequency plug-ins additionally contain a third module, an isolation amplifier (Iso-Amp).

3.1 Reference Channel

The RF Null Detector is a double conversion frequency locked receiver. The first conversion provides a common main frame 20 kHz IF frequency. The second conversion is a homodyne synchronous detection.

The homodyne detection requires a reference signal source synchronous at the 20 kHz IF. Due to the critical differential phase stability required and the narrow band IF amplifiers incorporated, it is necessary to provide a local oscillator (L.O.) which is frequency locked to the incoming signal. Hereafter the L.O. is referred to as the VCLO (Voltage Controlled Local Oscillator).

3.1.1 VCLO

The 20 kHz IF is generated by using a common

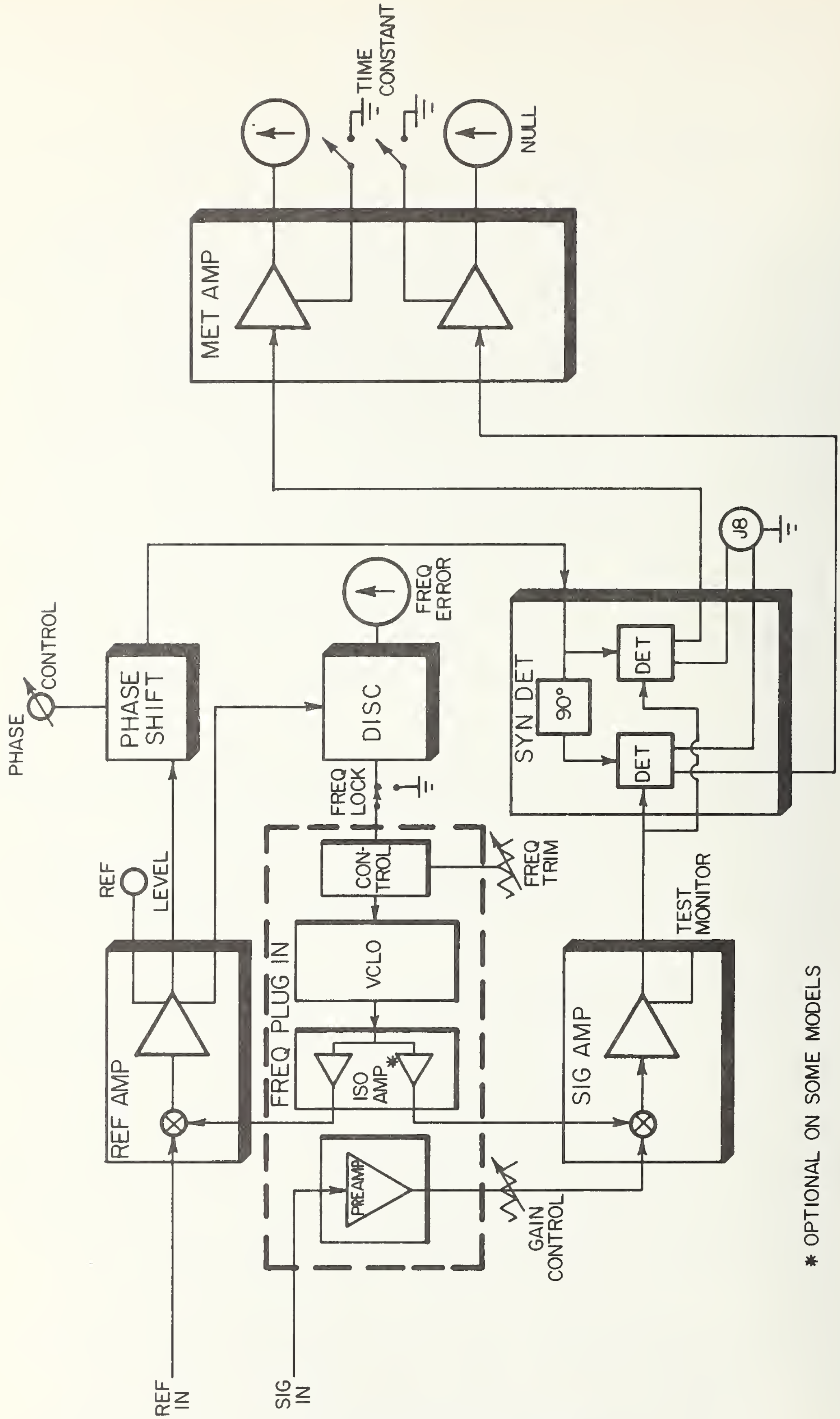


Figure 3.1. Functional block diagram

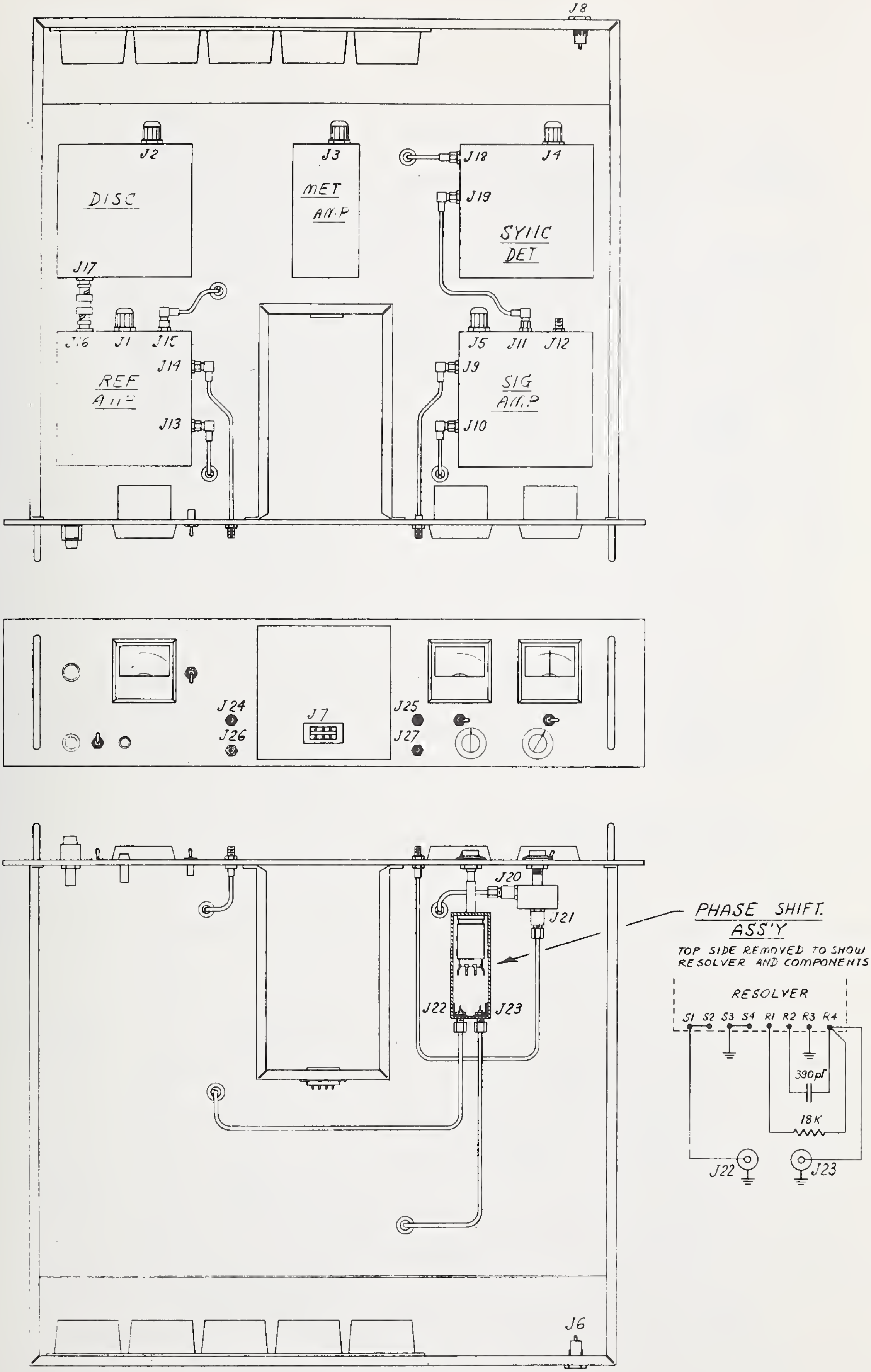


Figure 3.2. Main frame RF wiring diagram

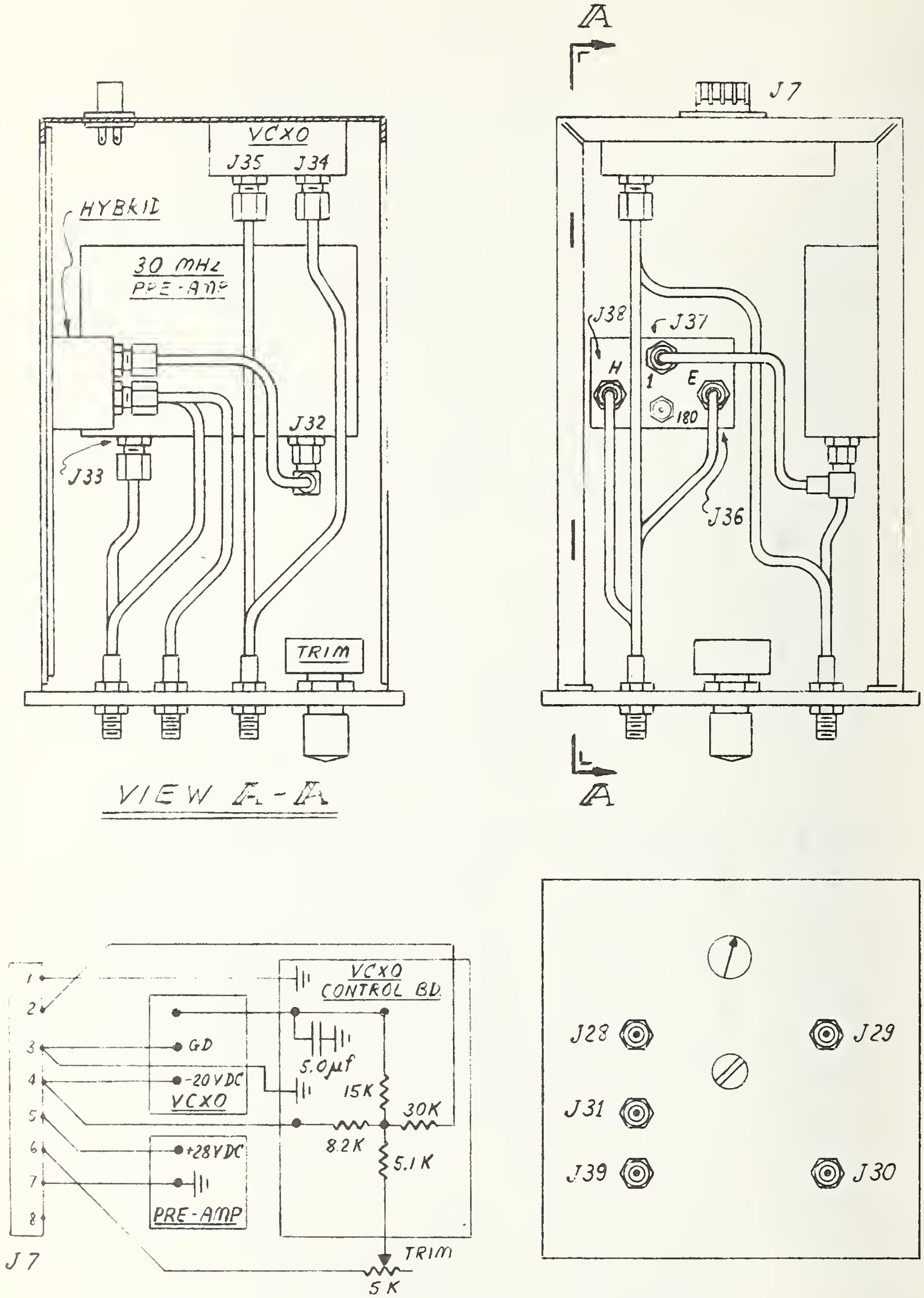


Figure 3.3. Frequency plug-in wiring diagram

VCLO (located in the frequency plug-in) as a mixer local oscillator for both the null signal and the reference signal provided from the external system. The VCLO output is coupled to the mixers through external cables (supplied with the unit). RF leakage from the Reference signal is prevented from entering the Null channel by either a separate optional Iso Amp or by providing isolation within the VCLO itself. The method used varies with each VCLO and is covered in the plug-in options.

3.1.2 Reference Amplifier

The external reference frequency signal is connected directly to the reference mixer located within the reference amplifier (Ref Amp). The reference amplifier is a three stage, 20 kHz, 80 dB gain Amplifier. Up to 20 dB AGC is provided to insure a constant amplitude reference voltage to the detectors, independent of amplitude changes in the external reference voltage. The Ref Amp contains an additional circuit, which lights the Ref Level Lamp when the 20 kHz Ref Signal is adequate for detector operation. Two outputs from the Ref Amp are available. The first connects the 20 kHz signal directly to a 20 kHz discriminator. The second passes through the phase shifter assembly and is applied to the Syn Det (Synchronous Detector) to provide the detector reference voltage.

3.1.3 Phase Shifter

The phase shifter assembly contains a resolver with appropriate circuitry to provide 360° of Electrical phase shift for 360° of mechanical rotation of the front panel phase control knob.

3.1.4. Discriminator

The first output from the Ref Amp is applied to the discriminator (Disc). The discriminator is an unconventional inductorless 20 kHz discriminator, producing a bi-directional voltage proportional to the frequency deviation from 20 kHz. This deviation is indicated by the frequency error meter on the front panel. The output from the Discriminator is amplified and connected through the frequency lock switch to the VCLO Control Board in the locked position. In the unlocked position the VCLO Control is grounded and the output amplifier gain is reduced by 15 dB to provide easier frequency trimming.

3.1.5 VCLO Control

The control board contains the servo loop filter and a provision for independent tuning of the VCLO with the frequency trim control. This control allows precise tuning of the VCLO to 20 kHz above the incoming reference frequency prior to locking the VCLO.

3.2.0 Signal Channel

As noted in 3.1 the instrument is a double conversion receiver. Initial preamplification is provided by the preamplifier located within the frequency plug-in. Its output is mixed with the common VCLO, thus providing a 20 kHz IF (first conversion) which is synchronous with the reference channel IF.

The signal channel IF and the Reference Channel IF are then synchronously detected (second conversion). This output is amplified, filtered, and displayed on the front panel Null Meters.

3.2.1 Pre Amplifier

The null signal is first amplified in a low noise 3 stage 66 dB preamplifier (Pre Amp) of appropriate frequency for the individual plug-in. The output from the Pre Amp is connected to the main frame through an external cable (supplied with the unit) from J27 to J30.

3.2.2 Gain Control

The Pre Amp output is connected to a main frame, front panel controlled, 90 dB attenuator. This attenuator functions as a gain control. The output from the attenuator is connected to the mixer of the signal amplifier (Sig Amp).

3.2.3 Signal Amplifier

The Sig Amp is a 90 dB gain (including the mixer) 20 kHz Amplifier. It contains three stages, two of which are tuned, resulting in a narrow band amplifier. Two outputs are provided, one as a test jack, and the second, which is connected to the synchronous detector (Syn Det) input.

3.2.4 Synchronous Detector

The Syn Det is in fact a dual detector, each channel of which is a full wave synchronous detector. These detectors provide a wide dynamic range in order to detect a signal of interest in the presence of up to +40 dB of noise. A fixed 90° phase shift is inserted in one reference path thus making one detector sensitive to voltages in quadrature with respect to the other.

Each detector has two outputs. One output from each detector is connected to rear panel connector J8 for use in an external servo control circuit if desired. The other output from each detector is connected to the meter amplifier (Met Amp).

NOTE: Synchronous detectors are characterized by their phase sensitivity. The output voltage is $E\cos\theta$ where θ is the phase angle between the reference and the signal of interest. Thus, at 0° and 180°, the detector will have maximum sensitivity and the output is bi-directional. At 90° and 270° the output will be zero in a perfect detector. By inserting the 90° phase separation in the Reference voltages for the detectors, one can be sensitive to the resistive component of the signal while the other is sensitive to the reactive component of the signal.

If there is capacitive coupling between windings within the detector transformer, this phase separation will be compromised, so the transformers used are specially NBS-designed toroidal units to approach the theoretical goal.

3.2.5 Meter Amplifier

This unit contains two identical DC Amplifiers with limited frequency response. The detector outputs are amplified and displayed on their respective front panel Null Meters. An additional time constant switch is available for each circuit to reduce the effect of indicated noise when operating in the maximum gain position.

4.0 Maintenance and Circuit Description

The following section contains a detailed circuit analysis of each individual module and assembly. Test and adjustment procedures for each separate unit are included in each subsection. Refer to Schematics and Parts pictorials, section 6, for parts identification.

4.1.0 Main Frame Assembly (fig. 7.1 - 3.2)

4.1.1 The main frame assembly contains the wiring, connectors, meters, and various switches which interconnect the replaceable modules.

4.1.2 A complete functional description of the entire unit is contained in section 3.0. No additional circuitry is contained independent of these replaceable modules, which are treated individually within this section.

4.1.3 Test Procedures (Plug In should be tested first. See Section 5.0).

a. Connect the RF Null Detector per instructions 2.3.1, 2.3.2, and 2.3.4. (Delete cable J27-J30 (C-2) and install a 50 Ω termination on J27 and J30.) Gain control fully CW.

Null meters should indicate 0 ± 1.0 μa.

b. Remove termination from J27 and connect a 3 μv signal synchronous with the input to J26. Adjust phase control for 0 indication on left null meter and positive indication on right null meter.

Right null meter should indicate +30 ± 10 μa.

c. Rotate Phase Control 180°.

Right null meter should indicate negative with the magnitude equal to b ± 3 μamp.

d. Rotate Phase Control 90° CW from c. position for zero indication on Right null meter.

Left null meter should show indicated value of b. (± 3 μa).

e. Rotate Phase Control 180° from d position.

Left null meter should indicate negative with the magnitude equal to d (± 3 μamps).

f. Power off.

Reconnect the cable from J27-J30.

Repeat steps 2.3.1, 2.3.2 and 2.3.4.

Connect 50 Ω termination to Sig In on the Plug-in

Gain Max CW.

Null meters should indicate a zero average with a maximum excursion of ± 15 μamps.

T.C. Switch to Slow, (S).

Null meters should indicate a zero average with a maximum excursion of ± 5 μa.

g. Connect the 3 μv signal from step b through a 60 dB attenuator to Sig In on Plug-in. (If two inputs are available attach a 50 Ω termination to one input.)

Repeat steps b through e on both fast and slow time constants.

Outputs should indicate the previous readings. Tolerance -0 + 6 dB.

NOTE Meter fluxuations in the fast position will require visual averaging of the meter indication.

Meter response time in the slow position will require several seconds to reach the final value.

4.2.0 Power Supply (fig. 7.1)

4.2.1 All DC power for circuit operation is provided from the master power supply board (MPS-1). This board is supplied with AC power from rear panel connector J6 via the front panel fuse (f1) and AC power switch (S2).

4.2.2 The board contains five commercial dual output regulated power supplies. Three units, (PS1,2,3) are adjusted to provide ± 15 VDC while PS4 is adjusted for ± 14 VDC and PS5 is adjusted to ± 10 VDC.

PS1 provides power via a shielded cable to the Signal Amplifier Module through P5. No common power ground exists on MPS-1. This prevents ground loops.

PS2 supplies DC power to the Discriminator via plug P2, Reference Amplifier via plug P1, and the Meter Amplifier via plug P3.

PS3 supplies power to the Synchronous Detector through P4. In addition, + 15 VDC is connected to J7 (pin 6) for use in some models of the Frequency Plug-In.

PS4 is connected such that the negative terminal is grounded, thus providing + 14 VDC and + 28 VDC. Each of these voltage sources is connected to J7 (Pin 5,8) for a preamplifier voltage selection. The + 28 VDC is additionally connected to DS2 (reference level indicator lamp).

The positive terminal of PS5 is grounded providing -20 VDC to J7 (Pin 4) for the VCLO within the Frequency Plug-In.

Resistor R1 on MPS-1 is the current limiting resistor for DS1 (power "on" indication) located on the front panel.

4.2.3 Test Procedures

The power supplies are preadjusted at assembly. The proper voltages are listed below.

Measurement Point		Voltage	Ripple
P-2	Pin A to H	+15VDC ± 200mV	5mV
	Pin B to H	-15VDC ± 200mV	5mV
P-4	Pin A to H	+15VDC ± 200mV	5mV
	Pin B to H	-15VDC ± 200mV	5mV
P-5	Pin A to H	+15VDC ± 200mV	10mV
	Pin B to H	-15VDC ± 200mV	10mV
J-7	Pin 5 to 7	+28VDC ± 400mV	10mV
	Pin 8 to 7	+14VDC ± 400mV	10mV
	Pin 4 to 3	-20VDC ± 400mV	10mV

4.3.0 Reference Amplifier (fig. 7.2 - 7.3)

4.3.1 The Reference Amplifier supplies the 20 kHz reference IF within the main frame. It is generated by mixing the VCLO signal (located within the Frequency Plug-In) and the externally supplied reference signal.

4.3.2 The Reference Amplifier requires two inputs, +5 DBM local oscillator input at J14 and 50 to 500 microvolts at J13. The frequency range is 100 kHz to 100 MHz with the local oscillator 20 kHz above the frequency of the input signal.

The two inputs are heterodyned in a commercial mixer (M1). The output is filtered by LP1 (50 kHz Low Pass) reducing harmonics and L.O. feedthrough at low frequencies. Resistor R4 provides a matched load for LP1, and C1 is a coupling capacitor.

The mixer output is amplified by Q1. Bias is provided by R1, R2, R3, and C2. R5 is the emitter resistor and C4 the RF bypass. L3 in conjunction with C5 and C21 (when required) are tuned to 20 kHz providing in excess of 50 db gain at 20 kHz.

Transistors Q2, Q3, and Q7 function as a voltage variable gain amplifier which automatically provides a constant output voltage independently of input changes. Q2 is an emitter follower which provides an impedance match between the high output impedance of Q1, and the low input impedance of Q3, R6 and R7 furnish bias for Q2 while R9 and R10 provide bias for Q3. C6, C7, and C8 are coupling capacitors. R8 is an emitter resistor for Q2.

The gain of Q3 is determined by the ratio of R11, the emitter resistor, and the collector load. The collector load is composed of R12 and Q7 a dual gate MOS field effect transistor (f.e.t.) whose effective resistance is controlled by the gate voltage. This voltage is supplied from U2. The output voltage of U2 thus controls the gain of this stage.

Additional gain (X100) for the module is provided by U1 and its associated components R13-R14. The output from U1 is coupled by C5 to two emitter followers Q4 and Q5. Common bias is supplied by R15-R16 while R17-R18 are the respective emitter resistors. Q4 output is connected to J16 (Discriminator input) via C12, while the output of Q5 is coupled to J15 (Phase Shifter input) through C13.

Automatic gain control is accomplished by sampling the output of Q5 and converting it to a negative DC voltage. This voltage is generated by C14, R19, D19, and C15. This voltage is connected to one side of a dual resistor divider composed of R20, R21, R22, and R23. The other side is supplied with a variable positive voltage from R25 and R26.

The output of the divider R20-R21 is connected to the input of U2, a X100 gain DC Amplifier. R27 is the feedback resistor. The output of U2 controls the effective resistance of Q7 through the low pass filter composed of R28-R29 and C18.

The circuit provides automatic leveling by the following analysis: Assuming an initial stable condition, an increase in output voltage results in a larger negative voltage at the voltage divider. This in turn results in a negative-going input to

U2. U2 is an inverting amplifier which provides a positive voltage on Q7 gate. The f.e.t. decreases its effective resistance thus decreasing the gain of Q6.

The output magnitude can thus be controlled by adjustment of R25, changing the level at which stability exists.

The second divider controls U3, which is connected as an inverting switch for Q6. When the input for the divider is insufficient for leveling to occur (less than 50 μv input), the output from the divider composed of R22-R23 will be positive. The output from U3 will be -15VDC under this condition, which will prevent conduction of Q6. When the amplifier output rises to a leveled condition, the negative voltage will be sufficient for the input to U3 to be negative, which provides a positive output. This positive output turns Q6 on, which supplies current to DS2 (Reference Level Indicator). R25 is a base current limiting resistor.

Frequency compensation for operational amplifiers U1, U2, and U3 is provided by C9, C16, and C17.

RF decoupling is provided by filters composed of L1C3, L2C11, L4C19, and L5C20.

4.3.3 Test Procedures

Connect the Reference Amplifier as indicated in fig. 4-1A.

a. Set RF Sig. Source #1 to 100 kHz.

Adjust output to 100 μv.

b. Set RF Sig. Source #2 to 20 kHz ± 100 Hz above the frequency of #1.

Adjust for +5 dBM.

c. Connect Scope to J15.

Output should be 0.8VPP (-0 + 0.5), 20 kHz.

If not, adjust R25 for 0.8VPP.

d. Reduce RF Sig. Source #1 to 50 μv.

Output should remain at 0.8VPP.

e. Increase RF source #1 output to 500 μv.

Output should remain at 0.8VPP.

f. Connect scope to J16.

Output should be 0.8VPP.

g. Repeat a, b, d, and e for RF source #1 frequency settings of 10 MHz, 30 MHz, and 60 MHz. Do not readjust R25.

4.4.0 Phase Shifter (fig. 3.2)

4.4.1 The phase shifter provides continuous electrical phase shift of the 20 kHz reference signal with mechanical rotation of the assembly shaft (360° of mechanical rotation equals 360° electrical).

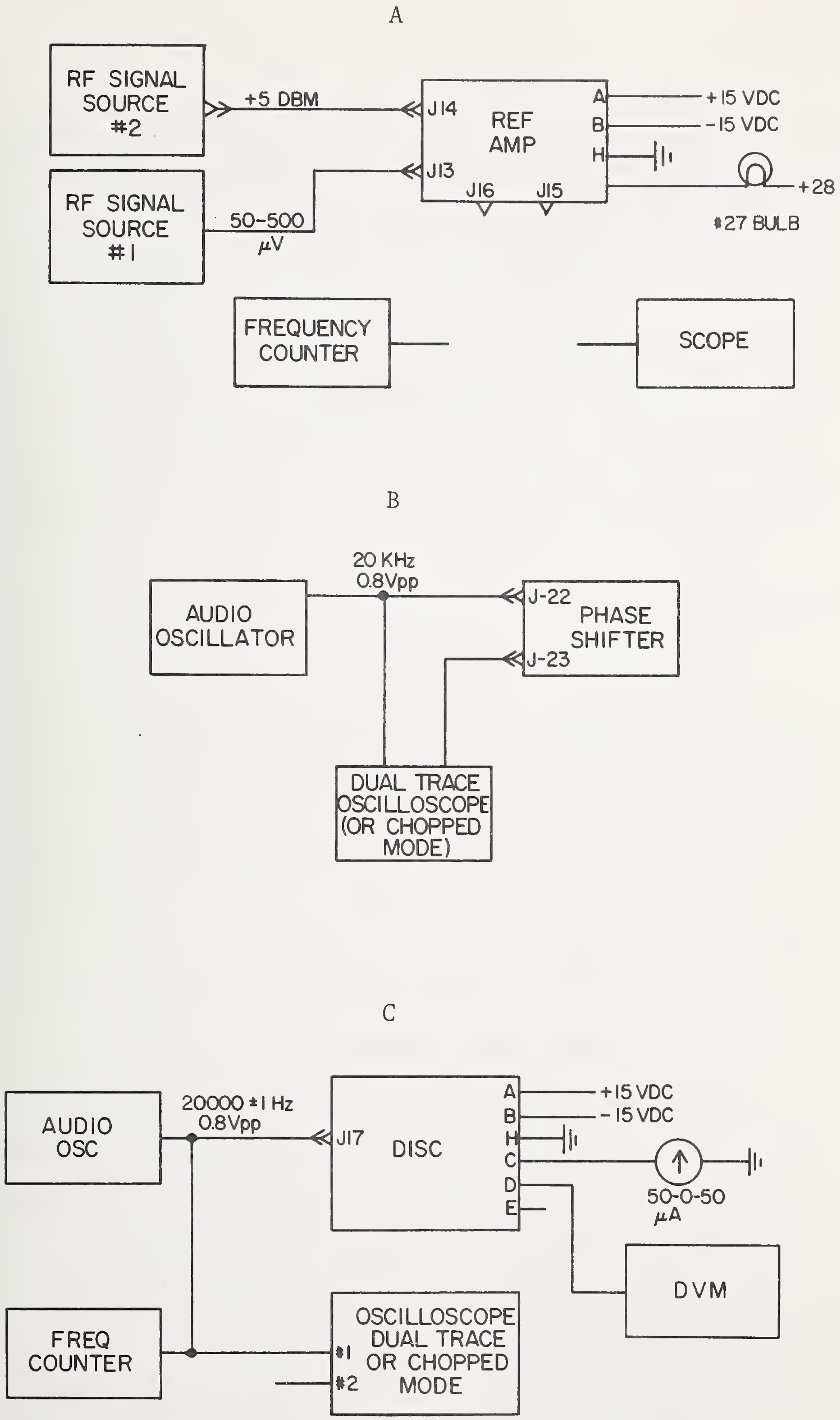


Figure 4.1 Test diagrams

4.4.2 The phase shift assembly consists of a commercial resolver with a resistor-capacitor divider connected across the rotor outputs. The 20 kHz signal from J15 of the reference amplifier is connected to J22 of the phase shift assembly. This input is connected in parallel to the two stators of the resolver. When the impedance of the capacitor is approximately equal to the resistor value, the output from the R1C1 junction is a constant-amplitude signal whose phase with respect to the stator input is variable with mechanical rotation of the input shaft. This output is connected to J23 of the assembly.

4.4.3 Test Procedures

Connect the phase shifter as indicated in fig. 4.1B.

a. Adjust the oscillator to 20 kHz ± 25 Hz and 0.8VPP.

b. Rotate resolver for in phase signal.
   Output should be 1.3VPP ± 0.1VPP.

c. Rotate resolver shaft slowly through 360 mechanical degrees. Electrical phase shift should rotate through 360°. Output amplitude should not vary more than 0.1VPP.

4.5.0 Discriminator (fig. 7.4 - 7.5)

4.5.1 The discriminator controls the frequency of the Voltage Controlled Local Oscillator within the frequency plug-in. It maintains the local oscillator precisely 20 kHz above the external reference signals by providing a bi-directional DC voltage proportional to differential frequency deviation from 20 kHz.

4.5.2 The Discriminator input (J17) accepts a 0.8VPP 20 kHz signal from the reference amplifier. The signal has two paths, one to a tuned amplifier, the other to a 90° fixed phase shift network.

The 90° phase shift is generated by U3 and U4 with their associated components. U3 provides a low output impedance to drive one input of the phase shift network (R23, R24, C18). C15 is a coupling capacitor while R19 provides a dc ground return for the amplifier input. The output of U3 is phase inverted by U4 producing a 180° shifted signal. R20, R21, and R22 provide unity gain. The output of U4 is connected to the second input of the phase shift network. Adjustment of R24 provides precisely 90° phase lag from the input.

The output from the divider is amplified by U5. R26 is a dc ground return while R25 and R27 produce a voltage gain of 10. This 90° phase lagging signal is coupled to the discriminator circuitry via C9.

The tuned circuit for the discriminator is an active filter composed of U1 and its associated components, (R1, R2, R3, R4, C1 and C2). This narrow band filter is tuned to precisely 20 kHz by adjustment of R3. U2 and its associated components, R5, R6, and R7 invert the tuned signal at unity gain. The in-phase and 180° out-of-phase signals are coupled to the discriminator circuitry by C8 and C10. These three signals generate a bi-directional dc voltage proportional to frequency deviation. This voltage is produced by subtracting the voltages of two rectifiers. Each of these rectifies the output of a separate voltage divider. One is composed of R8-R9 and the other by R11-R12. These dividers have a common terminal coupled to the 90° phase-shifted signal. R12 is coupled to the 180° signal while R8 is coupled to the in-phase signal.

The divider output voltages will be of equal magnitude at 20 kHz, and thus the dc voltage developed across R13C11 will be equal to that across R14C12.

Their subtraction results in 0 dc potential from R28 to pin 3 of U6. C6 provides an ac ground for the divider while R10 serves as a dc return for the rectified current. D1 and D2 serve to rectify the ac signal.

When the input signal rises in frequency the action of the tuned circuit provides a phase delay with respect to the input. In this condition the output of divider R11-R12 increases since the two signals are more nearly in phase. The inverse is true for the divider composed of R8-R9, since they will become farther out of phase.

Since the AC input to D1 is decreasing while the signal input to D2 is increasing, the rectified voltage will also undergo similar changes. The net result will be a negative potential applied to the input of U6. The inverse will be true when the frequency decreases.

This bi-directional voltage proportional to frequency is amplified by U6. The gain is determined by the ratio of R15, R16, and R17. The frequency lock switch (S1 on the front panel) is connected such that R16 is in parallel with R17 in the unlocked position, reducing the gain of U6 by 5.5. The output of U6 is connected to the VCLO through J7 (pins 1,2) in the locked position and controls the VCLO frequency. The output of U6 is also connected to the Frequency Deviation Meter (M1) through R18, producing a front panel display of the frequency deviation from 20 kHz.

Capacitors C3, C4, C5, C7, C14, C17, and C19 provide frequency compensation for the respective operational amplifiers.

L1C20, L2C21 provide dc filters for the input power. Pins f and k of J2 are shorted to make this unit compatible with a prototype model.

4.5.3 Test Procedures

Connect the Discriminator as indicated in fig. 4.1.C.

a. Connect #2 scope input to U1 Pin 6 (TP1).
   (See Parts Pictorial)
   Adjust R3 for precisely 180° shift (output 6-8VPP).
   (Phase meter can be used if available.)
b. Connect #2 scope input to U2 Pin 6 (TP2).
   Output should be in phase and of equal magnitude to TP1 output.
c. Adjust R24 for zero indication on the 50-0-50 μa meter.

d. Adjust audio oscillator frequency for -50 μa indication on frequency deviation meter (M1). Counter should indicate 20035 ± 5 Hz.

e. Record frequency.

Adjust audio oscillator frequency for +50 μa indication on frequency deviation meter (M1). Counter should indicate 20 kHz minus deviation in previous reading ± 3 Hz.

f. Connect Pin D and E of J2.

g. Adjust audio oscillator frequency for -50 μa indication on meter M1.

Counter should read 20250 ± 50 Hz.

h. Adjust audio oscillator frequency for +50 μa indication on meter M1.

Counter should read 19750 ± 50 Hz.

4.6.0 Signal Amplifier (fig. 7.6 - 7.7)

4.6.1 The signal amplifier provides a 20 kHz IF signal generated from the VCLO input and the output of the manual gain (front panel) control. This Amplifier has 90 dB gain.

4.6.2 The signal amplifier requires two inputs, a +5 DBM to the LO input J9 and a signal of no more than 100 μv to J10. The frequency range is 100 kHz to 100 MHz with the LO input 20 kHz above the signal.

The two inputs are heterodyned in a commercial mixer (M1). The output is filtered by LP-1, (a 50 kHz Low Pass) reducing harmonics and LO feedthrough at low input frequencies. R1 provides a matched load for LP1, and C2 is the coupling capacitor.

The mixer output is amplified in a tuned circuit composed of Q1 and associated parts. R3, R4, R5, and C1 provide bias while R2 is the emitter resistor.

C3 is the RF bypass. Tuning is accomplished by L1 and C4. R23 may be added at assembly to provide precise tuning.

Impedance matching to U1 is accomplished by Q2, an emitter follower. Bias for Q2 is provided by R6 and R7. R8 is the emitter resistor while C6 and C7 are coupling capacitors.

R9 and feedback resistor R11 produce a gain of 10 by U2. R10 is a dc return for U1.

The output of U2 is coupled directly to an active filter composed of U2 and associated components R12, R13, R14, R21, C11, and C12. This amplifier furnishes a gain of 100 with a 1 kHz bandwidth. Tuning adjustment is provided by R21.

Two emitter followers, Q3 and Q4, furnish identical outputs from the module. Common bias from R15-R16 controls both Q3 and Q4 while C16 is the coupling capacitor. R17-R19 and C17-C19 provide individual decoupling from the dc power. R18 and R20 are the emitter resistors while C18 and C20 couple the signals to J11 and J12.

Capacitors C8, C9, C10, C13, C14, and C15 provide frequency compensation for their respective amplifiers.

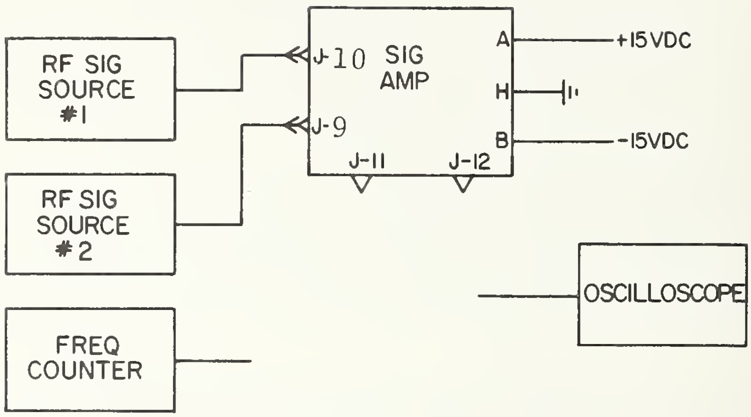
Power line filtering is provided by filters composed of L2C5, L3C21, and L4C22.

4.6.3 Test Procedures

Connect the Signal Amplifier as indicated in fig. 4.2A.

a. Set RF signal source #1 to 100 kHz.
   Reduce output to less than 1 μv.
b. Set RF signal source #2 to 20 kHz ± 100 Hz above the frequency of signal source #1. Adjust for +5 DBM.
c. Connect oscilloscope to J11.
   Noise output should be less than 100MVPP on scope.
d. Increase the output of RF signal source #1 to 30 μv. Adjust R21 for maximum indication on oscilloscope. Output should be 2VPP minimum at 20 kHz.

A



B

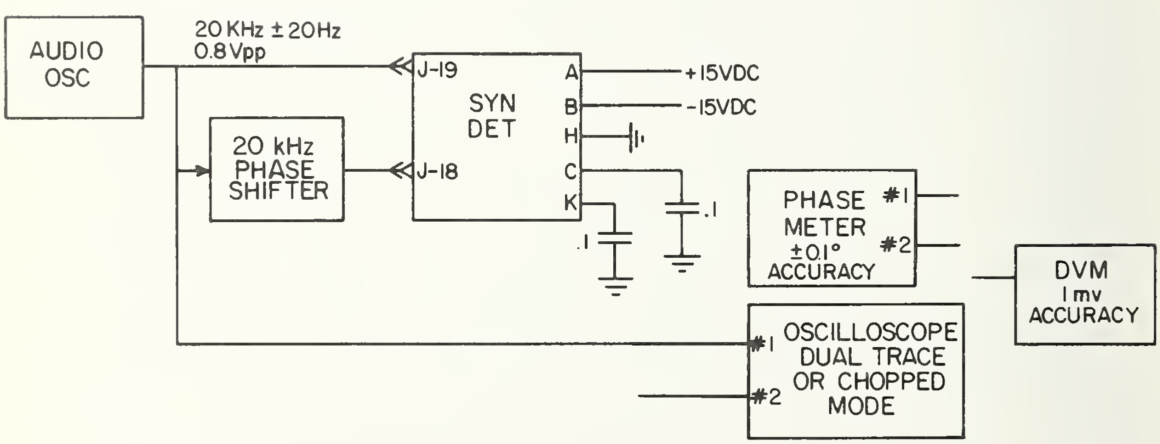


Figure 4.2. Test diagrams

e. Connect oscilloscope to J12. Output should be identical to that at J11.

f. Repeat above steps for RF signal source #1 frequencies of 10 MHz, 30 MHz and 60 MHz as desired. DO NOT READJUST R21.

4.7.0 Synchronous Detector (fig. 7.8 - 7.9)

4.7.1 The Synchronous Detector contains two identical homodyne or synchronous detectors whose output voltage is Ecosθ, where E is the signal input, and θ is the phase angle between the signal and Reference voltages. A 90° phase shift is inserted in one Reference path, making that detector sensitive to signals in quadrature with respect to the first signal.

4.7.2 The 1.3VPP 20 kHz reference signal from the phase shift assembly is injected at J18. C1 is the coupling capacitor and R1 a ground return for U1. U1 is a unity gain voltage follower. Its output is phase inverted at unity gain by U2 and associated resistors R2, R3, and R4. The output of U2 is the input for the Reference Driver (U3) for the #1 detector. The output of the voltage divider composed of C4, R5, and R6 is adjusted for a 90° leading signal by R5 and furnishes the input for the second detector driver U6. The two detectors are identical and only the number one detector will be discussed. U3 with R7, R8, and R9 amplify the input signal with a gain of 5, which in turn is connected to T1 through R10, a damping resistor.

The detector is an 8-diode full wave, wide dynamic range, synchronous detector. The circuit is designed to detect synchronous signals in the presence of up to 40 db noise.

This requires a reference voltage of sufficient magnitude to control diode switching in the presence of the maximum noise peak.

T1 is a 10:1 step up transformer which, when connected to the dual diode paths, alternately switches each set of diodes into conduction for half of each cycle of signal. The large voltage step-up insures the diode conduction is controlled by the reference voltage instead of the noise voltage from T3. C6 tunes the transformer to approximately 20 kHz to present a non-reactive load to the driver, U3.

The signal to be detected from J19 is coupled in common to both detectors by C8 and C10. Only that path to #1 detector will be discussed. U4 in conjunction with R11, R12, and R13 is a unity gain amplifier which drives T3 (a 1:3 step up) through R14 a damping resistor. C7 tunes the transformer just as C6 does.

When no signal is present the current in R27 alternately changes direction for each half cycle. When a signal is in phase with the reference signal, current in the load resistor R27 due to the signal voltage will flow only in one direction due to the alternate switching of the diodes. Noise voltages which are of random phase with respect to the reference can flow in both directions creating an average of zero.

When a signal is 90° or 270° with respect to the reference voltage, the current in the load resistor will reverse direction for half of the cycle thus giving a net voltage of zero. The detector is therefore insensitive to quadrature (90°, 270°) voltages. R23-R26 are current limiting resistors for the diodes. Detector output is taken from J4 (pin C and D).

Capacitors C2, C3, C5, C9, C11, and C12 provide frequency compensation for their respective operational amplifiers.

DC power is filtered by L1C15 and L2C16.

4.7.3 Test Procedures

Connect the Synchronous Detector as indicated in fig. 4.2B. See Parts pictorial and schematics for parts identification.

a. Observe voltage at J18 with scope input #2. Adjust Phase Shifter for in-phase condition. Voltage should be 1.2VPP (± 0.1).

b. Observe voltage at R23--R24 (TP1).

   Voltage should be 30VPP (± 2.5), 180° out of Phase.

c. Observe voltage at R25-R26 (TP2).

   Voltage should be 30VPP (± 2.5) in phase.

d. Observe voltage at R28-R29 (TP3).

   Voltage should be 30VPP (± 2.5), 90° leading the input signal.

e. Observe voltage at R30-R31 (TP4).

   Voltage should be 30VPP (± 2.5), 90° lagging the input signal.

f. Connect Phase Meter input #1 to junction of R21-R22 (TP5). Connect Phase Meter input #2 to junction of R9-R10 (TP6).

   Phase angle should be 90° ± 0.1°. If not, adjust R5.

g. Connect DVM to J4 Pin F. Disconnect OSC from J19. Short J19.

Voltage indicated should be less than 4 mv.

Connect DVM to J4 Pin E. Voltage indicated should be less than 4 mv.

h. Remove short from J19. Connect audio oscillator to J19.

Connect #1 Phase meter input to J19.

Connect #2 Phase meter input to J18.

Connect DVM to pin E, J4.

Monitor audio oscillator output for 0.8VPP during the following steps.

Adjust phase shifter for 0.000 VDC (± 1 mv) on Pin E with nominal 7° indication on Phase meter.

Record Phase angle.

Adjust phase shifter for 0.000 VDC (± 1 mv) on Pin E with nominal 187° indication on Phase meter.

Record Phase angle.

Difference in reading should be 180° (± 1°).

Connect DVM to pin F, J4.

DVM should read 0.85 VDC (± 0.05).

Adjust phase shifter for 0.000 VDC (± 1 mv) on Pin F, J4, with approximately 97° indicated on Phase meter.

Record Phase angle.

Adjust phase shifter for 0.000 VDC (± 1 mv) on Pin F with approximately 277° indicated on Phase meter.

Record Phase angle.

Difference in phase angle should be 180° (± 1.0)

Connect DVM to Pin E of J4.

DVM should read 0.85 VDC (± 0.05)

Average Phase angle readings 1 and 2.

Average Phase angle readings 3 and 4.

Differences between averages should be 90° ± 1°.

4.8.0 Meter Amplifier (fig. 7.10 - 7.11)

4.8.1 The meter amplifier contains two low pass DC amplifiers, each of which amplifies one detector output for display on the front panel null meters. An additional filter capacitor is provided to increase the indicated meter response time constant. These capacitors are activated by the front panel time constant switches.

4.8.2 The two amplifiers are identical so only one will be discussed. The frequency response of the synchronous detector signal at Pin C is reduced by the low-pass filter composed of R1C1. The front panel Time Constant switch provides a ground for C2 when activated, thus decreasing the frequency response of the filter by approximately a 7:1 ratio. U1 with R2-R3 provide an amplification of 4. R6 is a current limit resistor for the Null meter, which provides a meter sensitivity of 200 mV/10 μa. R4-R5 provides a DC output balance for the amplifier. C3 provides frequency compensation for the amplifier.

4.8.3 The following steps should be performed to insure proper operation of this assembly.

a. Connect ± 15 VDC to the appropriate pins of J3. (Allow 10 min. warm up.)

b. Connect ± 50 μa meter to pin F(+) and ground (-) of J3.

c. Short Pin c (J3) to ground.
   Meter should indicate zero. If not, adjust R5 for zero indication.

d. Connect + 200 mV to Pin c.
   Meter should indicate + 40 μamps.

e. Connect -200 mV to Pin c.
   Meter should indicate -40 μamps.
   Remove -200 mV to Pin c.

f. Connect low frequency oscillator to Pin c.
   Connect oscilloscope to TP1.
   Set oscillator for 1 Hz @ 200 mV PP.

Output on oscilloscope should indicate 175-225 mVPP.

g. Short Pin e to ground.

   Output should indicate 30-40 mVPP.

h. Repeat all steps above for second amplifier.

   Check output on TP2.

5.0 Frequency Plug-In

The following section contains a detailed description of the various units and parts contained in each of the plug-in available for use in the main frame assembly. Where modules which were designed at NBS are included, circuit description is provided. Schematics and wiring diagrams are included within Section 7. Parts lists are included in Section 6.

5.1.0 Plug-in SND/PI-30A (fig. 3.3 - 7.12)

5.1.1 This 30 MHz unit provides the local oscillator voltages for the reference and signal channel first mixers, the signal summation junction for use in dual channel null calibrations, and the preamplifier for the signal channel.

5.1.2 The reference and signal channel first mixers require a L.O. which is 20 kHz above the Plug-in frequency. This is provided by a commercially purchased VCLO which is tuned to 30020 kHz with the control voltage grounded. (Sensitivity-6kHz/V). Frequency control is provided by a control circuit mounted on a printed circuit board located on the left side of the plug-in.

This control functions as follows: In the unlocked position of the NBS/SND frequency lock switch Pin 2 of P7 is grounded. The resistor divider composed of R1, R3, R4, and R5 will produce zero voltage at the junction of R3-R5 by adjustment of R4, which is the front panel frequency trim control. This junction is connected through a low pass filter composed of R2-C1 to the control terminal of the VCLO. The low pass filter determines the tracking response of the VCLO. When the NBS/SND lock switch is in the locked position, the output of the Disc is connected to R1 through Pin 2 of P7. The output voltage of the Disc thus controls the voltage at the VCLO control terminal. This control voltage is of the proper polarity and magnitude to precisely maintain the VCLO 20 kHz above the reference voltage. This insures IF frequency stability independent of drift in either the Reference or VCLO.

The VCLO has two outputs whose magnitude are independently adjustable by a screwdriver adjustment. These adjusting screws are located under nylon cap screws on top of the VCLO. The two outputs have a minimum of 60 dB isolation at 30,000 kHz to insure isolation of Reference and the signal channel.

This plug-in is a special purpose unit designed to be used in a dual channel attenuator calibrator in which the channels are adjusted for equal output voltages. The plug-in contains the summation hybrid, which produces a null when the input voltages are of equal magnitude and are precisely in phase. If a single input is to be measured, this unit can be used with a 3 dB loss of sensitivity by installing a 50 Ω termination on the second input jack.

The output from the hybrid is connected to a 66 dB Pre Amp located at the right side of the plug-in. The Pre Amp output is connected to the Sig Out jack at the front panel.

5.1.2 Pre Amplifier (fig. 7.13 - 7.14)

5.1.2.1 The Pre Amp provides 66 dB gain at 30 MHz. This unit is specially designed to insure precisely 50 Ω input impedance consistent with a low noise figure.

5.1.2.2 This amplifier is a three-stage tuned amplifier operating from 28 VDC. The input signal is coupled through C2. Bias for Q1 is provided through R2 by adjustment of R1. C1 and C3 are RF bypass capacitors. L1 and C4 furnish input tuning, while R3, R4, and C4 enable the input impedance to be precisely adjusted to 50 Ω. These adjustments are made during construction and test and should not be adjusted without special instructions from NBS.

The first stage is tuned to 30 MHz by C6-C7 in conjunction with L2. R5 is a damping resistor to lower the Q.

The second stage of amplification is provided by Q2. C8 is a coupling capacitor and T1 in conjunction with C13 is tuned to 30 MHz. Bias is furnished by R8, and the output signal is coupled to the final stage of amplification, Q3, from the center tap of T1 through C14.

Bias current for Q3 is furnished by R10. Output tuning is provided by T2 and C17. The output is coupled from T2 to J33 through C8 from a tap selected to offer a 50 Ω output impedance.

RF decoupling is accomplished by filters composed of R6C1, R7C10C11, R9C15C16, and RF filter C9C12. Additional filtering is provided by ferrite beads on the resistor leads. D1 is a zener diode to reduce the supply voltage.

5.1.2.3 Test Procedures

Insert the SND/PI-30A into a NBS/SND. Do not connect the interconnecting cables.

a. Connect a 30 MHz generator to the Sig In.
Connect a 50 Ω load to the second input.
Connect a 50 Ω RF power meter to Sig Out.

b. Set 30 MHz generator to -70 dBm (70 μv).
Energize the AC power.
Output power should be -9 min -3 max dBm.

c. Repeat b with Sig In connections reversed.
Output power should be within 0.1 dB. Shut off all power.

d. Attach the RF cable from Sig Out of the SND/PI-30A to Sig of NBS/SND. Connect power meter to either VCLO output.
Energize AC power.
RF power should be 4.5 ± 0.5 dBm.
If not, adjust Osc output control under cap screw on VCLO.

e. Repeat d for second VCLO output.

f. Connect the RF cable from left VCLO output to Ref. L.O. input. Connect a frequency counter to the right VCLO output. Set freq trim control full CCW.
Frequency should be 30025 kHz min.

Set freq trim control full Cw.

Frequency should be 30015 kHz max.

g. Connect 100 μV 30000 ± 1 kHz signal to the Ref input. Lock Switch to unlock.

Adjust VCLO trim control for 0 indication of the freq error meter with Ref Indicator lamp on. Note frequency counter indication.

Adjust VCLO trim for -50 μa indication.

Frequency should be +300 ± 100 Hz from reading at 0 μa.

Adjust VCLO trim for +50 μa indication.

Frequency should be -300 ± 100 Hz from reading at 0 μa.

h. Rezero freq error meter with VCLO trim control and switch freq lock to lock position. Note frequency reading. Adjust VCLO trim control for -50 μa, switch lock to unlock and note frequency reading.

Frequency should be 3 kHz minimum from first reading.

i. Repeat step h except adjust VCLO for +50 μa.

Frequency should be -3 kHz min from first reading.

6.0 Parts List

6.1 Introduction

This section contains information necessary in ordering replacement parts. Table 6.1 lists parts in alpha-numerical order by reference designations. The list is arranged so that the components on each printed circuit board are listed together. Where possible, the manufacturer and manufacturer's part number are included.

A few parts listed will not be identical to those found in some instruments. The list contains the preferred component; and if it is necessary to replace it, the one listed should be used rather than one identical to the defective part.

Certain commercial equipment, components, or materials are identified in this paper in order to adequately specify the equipment. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

TABLE 6.1

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
		MASTER POWER SUPPLY		
MPS1	1	Master Power Supply Board	NBS	
PS1-PS3	3	Adjustable DC Power Supply	LAMBDA	LZD-22
PS4, PS5	2	Adjustable DC Power Supply	LAMBDA	LZD-23
R1	1	82KΩ 5% Carbon Resistor		
		REFERENCE AMPLIFIER		
RA1	1	Printed Circuit Board	NBS	
C1, C6, C7, C8, C10, C12, C14	7	Capacitor, .05 μf ceramic disc 100 V	Sprague	TG-S50
C2, C4,	2	Capacitor, 1 μf tantalum 35 V	Kemet	K1W35
C3, C11	2	Capacitor, 10 μf	G.E.	GE-62f-204-62
C5	1	Capacitor, 6200 pf mica 600 V	Elmenco	DM-10-622
C9	1	Capacitor, 5 pf mica 600 V	Elmenco	CDE6200
C13,C15,C18	3	Capacitor, 1 μf mylar	Sprague	5C023105X0250B3
C16	1	Capacitor, 20 pf mica 600 V	Elmenco	DM-10-2001
C17	1	Capacitor, 200 pf mica 600 V	Elmenco	DM-10-201J
C19, C20	2	Capacitor, 22 μf tantalum 35 V	Kemet	K22W6
C21	1	Capacitor, optional valve mica 600 V		
L1, L2, L4, L5	4	Choke 22 mh	J.W. Miller	70F222A1
L3	1	Choke 10 mh	J.W. Miller	9350-44
LP1	1	50 kHz Low pass filter	KAPPA	2A50BL
J1	1	Connector, 9 pin male power	Amphenol	126-219
J13, J14, J16	3	Connector, SMA bulkhead feed through	OSM	211
J15	1	Connector, BNC bulkhead feed through	Amphenol	OG-1094/U

Table 6.1. Parts list RF null detector NBS/SND

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
M1	1	Mixer	Merrimac	DMS-2-150
Q1	1	Transistor, NPN 2N3866	Motorola	
Q2	1	Transistor, NPN 2N697	T-I	
Q3, Q4, Q5	3	Transistor, PNP 2N3638		
Q6	1	Transistor, PNP 2N3904		
Q7	1	Transistor, Field Effect 3N 140 or 40822	RCA	
R1,R8	2	Resistor, 1.3 KΩ 5% Carbon		
R2	1	Resistor, 1.5 KΩ 5% Carbon		
R3,R10	2	Resistor, 24 KΩ 5% Carbon		
R4	1	Resistor, 51 Ω 5% Carbon		
R5	1	Resistor, 1 KΩ 5% Carbon		
R6, R7, R15, R16, R20, R21	6	Resistor, 100 KΩ 5% Carbon		
R9,R18	2	Resistor, 2.4 KΩ 5% Carbon		
R11	1	Resistor, 7.5 KΩ 5% Carbon		
R12	1	Resistor, 43 KΩ 5% Carbon		
R13,R17	2	Resistor, 10 KΩ 5% Carbon		
R14	1	Resistor, 1 MEG Ω 5% Carbon		
R19	1	Resistor, 30 KΩ 5% Carbon		
R23	1	Resistor, 120 KΩ 5% Carbon		
R24	1	Resistor, 3.9 KΩ 5% Carbon		
R25	1	Resistor, Adj 1 K	Helitrim	PR77
R26	1	Resistor, 10 Meg Ω 5% Carbon		
R27,R28	2	Resistor, 10 Meg Ω 5% Carbon		
R29	1	Resistor, 22 Meg Ω 5% Carbon		
U1, U2, U3	3	Operational Amplifier LM301A	Fairchild	UA301A
Misc	1	Reference Amp Box	NBS	
Hardware:	4	Pan Head Screw #6x32x½"		

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
Misc Hardware, continued	8	Nut #6x32		
	4	Nylon Washer #6		
	4	Flat Steel Washer #6		
	4	Lock Washer #6		
	6	Steel Washer ¼"		
	3	Solder Lug ¼"		
	1	Solder Lug 3/8"		
		PHASE SHIFTER ASSEMBLY		
	1	Resolver	American Electronics	1R11N16-138
		Purchased from AST/Servo Systems Newark, N.J.		R-215
C1	1	Capacitor, 390 pf mica 600 V	Elmenco	DM-10-391J
R1	1	Resistor, 18 KΩ 1% metalfilm		
J22, J23	2	Connector, SMA bulkhead feedthrough	OSM	211
	1	Resolver Box	NBS	
	2	Solder lugs ¼"		
	8	Solder lugs		
	1	Shaft coupler 3/16" to 1/4"	NBS	
		DISCRIMINATOR		
DC1	1	Printed Circuit Board	NBS	
C1, C2	2	Capacitor, 1500 pf mica	Elmenco	DM-10-1525
C3	1	Capacitor, 47 pf mica	Elmenco	DM-10-470J
C4	1	Capacitor, 270 pf mica	Elmenco	DM-10-271J
C5	1	Capacitor, 510 pf mica	Elmenco	DM-10-511J
C6, C11, C12	3	Capacitor, 0.1 μf ceramic disk	Sprague	TG-P10
C7, C16, C19, C20	4	Capacitor, 10 pf mica	Elmenco	DM-10-100J
C8, C9, C10, C13	4	Capacitor, 1 μf mylar	Sprague	5C023105X025033

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
C14	1	Capacitor, 200 pf mica	Elmenco	DM 10 201J
C15	1	Capacitor, .01 ceramic disk	Sprague	
C17	1	Capacitor, 20 pf mica	Elmenco	DM-10-200J
C20, C21	2	Capacitor, 10 μf @ 25 VDC tantalum	General Electric	62F-204-62
L1, L2	2	Choke 22 mh		
J1	1	Connector, 9 pin male	Amphenol	126-219
J17	1	Connector, BNC bulkhead feedthrough	Amphenol	UG1094/C
R1	1	Resistor, 10 KΩ 1% metal film		
R2	1	Resistor, 121 Ω 1% metal film		
R3	1	Resistor, 50 Ω Adjustable	Helitrim	PR77
R4	1	Resistor, 200 KΩ 1% metal film		
R5, R6, R7	3	Resistor, 90.9 KΩ 1% metal film		
R20, R21, R22	3	Resistor, 82 KΩ 5% carbon		
R8, R9, R11, R12	4	Resistor, 2 KΩ 1% metal film		
R10	1	Resistor, 2 K 5% carbon		
R13, R14	2	Resistor, 10 KΩ 5% carbon		
R15, R16, R18	3	Resistor, 20 KΩ 5% carbon		
R17	1	Resistor, 200 KΩ 5% carbon		
R19, R25, R26	3	Resistor, 100 KΩ 5% carbon		
R23	1	Resistor, 3.2 KΩ 1% metal film		
R24	1	Resistor, 1K Adjustable	Helitrim	PR77
R27	1	Resistor, 1 Meg 5% carbon		
U1	1	Operational Amplifier U715	Fairchild	U5F7715393
U2, U3, U4, U5, U6	5	Operational Amplifier LM301	Fairchild	UA301A

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
Misc. Hardware	1	Reference Amp Box	NBS	
	4	Pan head screw #6x32x½"		
	8	Nut #6x32		
	4	Nylon Washer #6		
	4	Flat Steel Washer #6		
	4	Lock Washer #6		
	1	Solder lug 3/8"		
		<u>SIGNAL AMPLIFIER</u>		
SA1	1	Printed Circuit Board	NBS	
C1, C17, C19	3	Capacitor, 1 μf @ 35 VDC tantalum	Kemet	K1 W35
C2, C6, C7, C16, C18, C20	6	Capacitor, .05 μf ceramic disc	Sprague	TG-S50
C3	1	Capacitor, 4.7 μf @ 25 VDC tantalum	Kemet	CDE-6200
C4	1	Capacitor, 6200 pf mica	Elmenco	
C5	1	Capacitor, 47 μf @ 20 VDC tantalum	Sprague	150D476X0020R2
C8, C13	2	Capacitor, 47 pf mica	Elmenco	DM-10-470J
C9, C10	2	Capacitor, 330 pf mica	Elmenco	DM-10-331J
C11, C12	2	Capacitor, 1500 pf mica	Elmenco	DM-10-511J
C14	1	Capacitor, 510 pf mica	Elmenco	DM-10-271J
C15	1	Capacitor, 270 pf mica	Kemet	K22 W6
C21, C22	2	Capacitor, 22 μf @ 35 VDC tantalum		
C23	1	Capacitor, optional mica		
L1	1	Choke 10 mh	J.W. Miller	9350-44
L2, L3, L4	3	Choke 22 mh	J.W. Miller	70F222A1
J5	1	Connector, 9 pin male	Amphenol	126-219
J9, J10, J11, J12	4	Connector, SMA bulkhead feedthrough	OSM	211

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
M1	1	Mixer	Merrimac	DMS-2-150
Q1	1	Transistor, NPN 2N3866	Motorola	
Q2	1	Transistor, NPN 2N697	TI	
Q3, Q4	2	Transistor, PNP 2N3638		
R1	1	Resistor, 51 Ω 5% carbon		
R2,R3	2	Resistor, 1 KΩ 5% carbon		
R4, R18, R20	3	Resistor, 10 KΩ 5% carbon		
R5	1	Resistor, 43 KΩ 5% carbon		
R6, R7	2	Resistor, 100 KΩ 5% carbon		
R8	1	Resistor, 4.3 KΩ 5% carbon		
R9, R10	2	Resistor, 5.1 KΩ 5% carbon		
R11	1	Resistor, 51 KΩ 5% carbon		
R12	1	Resistor, 2 KΩ 1% metal film		
R13	1	Resistor, 151 Ω 1% metal film		
R14	1	Resistor, 200 KΩ 1% metal film		
R15, R16	2	Resistor, 100 KΩ 5% carbon		
R17, R19	2	Resistor, 820 Ω 5% carbon		
R21	1	Resistor, Adjustable 20 Ω	Helitrim	PR77
U1, U2	2	Operational Amplifier U715	Fairchild	U5F7715393
Misc Hardware	1	Signal Amplifier Box	NBS	
	4	Pan head screws #6x32x½"		
	8	Nut #6x32		
	4	Nylon Washers #6		
	4	Flat Steel Washers #6		
	4	Lock Washer #6		
	4	Solder Lugs ¼"		
	8	Steel Washer ¼"		

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
		SYNCHRONOUS DETECTOR		
SD1	1	Printed Circuit Board	NBS	
C1, C8, C10	3	Capacitor, .1 μf ceramic disc	Sprague	TG-P10
C2, C3, C5, C9, C11, C12	6	Capacitor, 20 pf mica	Elmenco	DM-10-200J
C4	1	Capacitor, 1000 pf mica	Elmenco	DM-10-102J
C6, C13	2	Capacitor, 82 pf mica	Elmenco	DM-10-820J
C7, C14	2	Capacitor, 270 pf mica	Elmenco	DM-15-271J
C15, C16	2	Capacitor, 47 μf @ 25 VDC tantalum	Sprague	150D476X0020R2
D1 thru D16	16	Diode Germanium IN270		
J4	1	Connector, 9 pin	Amphenol	126-219
J18, J19	2	Connector, SMA bulkhead feedthrough	OSM	211
L1, L2	2	Choke 22 mh	Miller	70F222A1
R1, R7, R8, R19, R20, R23, R24, R25, R26, R28, R29, R30, R31	13	Resistor, 51 KΩ 5% carbon		
R2, R3, R4	3	Resistor, 10 KΩ 5% carbon		
R5	1	Resistor, Adjustable 5% carbon	Helitrim	PR77
R6	1	Resistor, 4.75 KΩ 1% metal film		
R7, R21	2	Resistor, 200 KΩ 5% carbon		
R10, R22	2	Resistor, 10 Ω 5% carbon		
R11, R12, R13, R15, R16, R17	6	Resistor, 100 KΩ 5% carbon		
R14, R18	2	Resistor, 51 Ω 5% carbon		

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
R27, R32	2	Resistor, 20 K 5% carbon		
T1, T2	2	Transformer 10:1 step up	NBS	
T3, T4	2	Transformer 3:1 step up	NBS	
U1 thru U6	6	Operational Amplifier LM-301A	Fairchild	LM301A
Misc Hardware	1	Syn Det Box	NBS	
	4	Panhead Screw #6x32x½"		
	8	Nuts #6x32		
	4	Nylon Washer #6		
	4	Flat Steel Washer #6		
	4	Lock Washers #6		
	2	Solder Lug ¼"		
		METER AMPLIFIER		
MA1	1	Printed Circuit Board	NBS	
C1, C4	2	Capacitor, 5 μf Non Polar	Sprague	151D505X0006X2
C2, C5	2	Capacitor, 28 μf Non Polar	Sprague	151D286X9006X2
C3, C6	2	Capacitor, 330 pf mica	Elmenco	DM-10-201J
J3	1	Connector, 9 pin male	Amphenol	126-219
R1, R2, R7, R8	4	Resistor, 100 KΩ 5% carbon		
R3, R9	2	Resistor, 300 KΩ 5% carbon		
R4, R10	2	Resistor, 1 Meg Ω 5% carbon		
R5, R11	2	Resistor, Adjustable 100 K	Helitrim	PR77
R6, R12	2	Resistor, 20 KΩ 5% carbon		
U1, U2	2	Operational Amplifier LM301A	Fairchild	LM301A

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
Misc. Hardware	1	Meter Amplifier Box	NBS	
	4	Pan Head Screw #6x32x½"		
	8	Nut #6		
	4	Nylon Washer #6		
	4	Flat Steel Washer #6		
	4	Lock Washer #6		
		MAIN CHASSIS		
ATT-1	1	Attenuator Variable	Texscan Corporation	CA100/50 with SMA Connectors
CBL-1	1	Cable, P9-J25	OSM Connectors	221-1 to 210-2
CBL-2	1	Cable, P10-P20	OSM	221-1 to 201A
CBL-3	1	Cable, P11-P19	OSM	221-1 to 221-1
CBL-4	1	Cable, P13-J26	OSM	221-1 to 210-2
CBL-5	1	Cable, P14-J24	OSM	221-1 to 210-2
CBL-6	1	Cable, P15-P22	OSM	221-1 to 201-A
CBL-7	1	Cable, P16-P17	Amphenol	UG-491 A/U
CBL-8	1	Cable, P18-P23	OSM Connectors	201-A to 201-A
CBL-9 thru CBL-11	1	Cable, P24-P28	OSM	201-A to 201-A
CBL-12	1	Cable, P25-P29	OSM	201-A to 201-A
CBL-13	1	Cable, P27-P30	OSM	201-A to 201-A
DS1	1	AC power indicator	Dial Co.	Cup 186-1472
DS2	1	Reference amp indicator bulb	Dial Co.	Body 183-9730-14-602
		Bulb	GE	327
fL1	1	Fuse and holder (½ amp)	Littlefuse	342012
J6	1	Syn Det output	Amphenol	126-221
J7	1	Freq Plug in Connector	Amphenol	26-183
J8	1	AC Power	Amphenol	

TABLE 6.1 (continued)

RF NULL DETECTOR MOD. NBS/SND

Reference Designation	Quantity	Description	Manufacturer	Part No.
M1	1	Freq Error Indicator	Simpson	2122TB
M2, M3	2	Null Indicator	Simpson	2122TB
P1 thru P5	5	Connectors for modules	Amphenol	126-222
S1	1	Freq Lock Switch	Alco	MST 205N
S2	1	AC Power Switch	Alco	MST 105D
S3, S4	2	Time Constant Switch	Alco	MST 105D
Misc. Hardware	1	Center Shelf	NBS	
	1	Outside front panel	NBS	
	2	Handles	NBS	
	2	Knobs gain and phase control		
	20	Pan head screw #4x40x¼"		
	8	Pan head screw #6x32x5/8"		
	8	Nuts #6		
	8	Nylon Nuts #6		
	8	Flat Steel Washers #6		
	8	Lock Washers #6		
	2	Pan head screws #4x40x3/8"		
	2	Nuts #4		
	2	Flat Steel Washers #4		
	2	Lock Washers #4		
	1	Solder lug #4		
	6	Flat head screw #6x32x3/8"		
	4	Rubber Grommets 9/16"		
	4	Sheetmetal Screws #4x3/8"		
	1	Fiber Shaft ¼"x1-3/4		
	1	Collar 1/4" x 3/8"		
	1	Floating Captive Nut 1/4" x 28		

TABLE 6.2

PLUG-IN SND/PI-30A

Reference Designation	Quantity	Description	Manufacturer	Part No.
		PRE AMP		
PA1	1	Printed Circuit Board	NBS	
C1,C2,C3,C9, C10,C14,C15, C18	8	Capacitor, .01 Ceramic disc	Sprague	
C4,C7,C13, C17	4	Capacitor, Adj. 7-25 pf		
C5	1	Capacitor, 68 pf mica		
C6	1	Capacitor, 33 pf mica		
C8	1	Capacitor, 47 pf mica		
C11,C12,C16	3	Capacitor, 1 μf @ 35 tantalum		
D1	1	Diode zener IN748		IN748
L1	1	Choke adj .2-4 mh		
L2	1	Choke 22 mh	Miller	
J32,J33	2	Connector (in)(out)	OSM	211
Q1,Q2,Q3	3	Transistor 2N3866	Motorola	
R1	1	Resistor, 50 K Adjustable	Helitrim	PR77
R2	1	Resistor, 220 K 5% carbon		
R3	1	Resistor, 680 K 5% carbon		
R4	1	Resistor, 1 K Adjustable	Helitrim	PR77
R5	1	Resistor, 270 Ω 5% carbon		
R6	1	Resistor, 4.7 KΩ 5% carbon		
R7	1	Resistor, 1 KΩ 5% carbon		
R8	1	Resistor, 47 KΩ 5% carbon		

Table 6.2. **Parts list plug-in SND/PI-30A**

TABLE 6.2 (continued)

PLUG-IN SND/PI-30A

Reference Designation	Quantity	Description	Manufacturer	Part No.
R9	1	Resistor, 220 Ω 5% carbon		
R10	1	Resistor, 100 KΩ 5% carbon		
Hardware	1	Box	NBS	
	4	Screws #6x32x½		
		VCLO CONTROL BOARD		
VCLO-1	1	Printed Circuit Board	NBS	
C1	1	Capacitor, 5.0 µf Non Polar	Sprague	151D
R1	1	Resistor, 3.0 KΩ 5% carbon		
R2	1	Resistor, 15 KΩ 5% carbon		
R3	1	Resistor, 8.2 KΩ 5% carbon		
R4	1	Resistor, 5 KΩ Adjustable		
R5	1	Resistor, 5.1 KΩ 5% carbon		
VCLO	1	Voltage Controlled Oscillator	Electronic Research Co.	EROS 600NW-2
Hybrid	1	Four port combing Hybrid	Merrimac	
	1	Termination, 50 Ω load	Narda	
P1	1	Connector, Power Input	Amphenol	26-182
CBL-1	1	Cable, P32-P37	OSM Connector	201A-201A
CBL-2	1	Cable, P33-J30		201A-210-2
CBL-3	1	Cable, P34-J28		201A-210-2
CBL-4	1	Cable, P35-J29		201A-210-2
CBL-5	1	Cable, P36-J39		201A-210-2
CBL-6	1	Cable, P38-J31		201A-210-2

TABLE 6.2 (continued)

PLUG-IN SND/PI-30A

Reference Designation	Quantity	Description	Manufacturer	Part No.
Misc. Hardware	1	Chassis Outside	NBS	
	1	Chassis Bottom	NBS	
	1	Front Panel	NBS	
	1	Knob trim control	USECO	1000-20
	1	Knob securing	USECO	625-20
	1	Shaft securings	NBS	
	2	Nut ¼x28		
	6	Pan head screw #4x40x¼		
	4	Pan head screw #6x32x¼"		
	4	Lock washers #4		
	12	Lock washers #6		
	4	Pan head screw #6x32x½"		
	8	Nuts #6		
	8	Flat steel washers #6		
	6	Flat head screw #4x¼"		
	4	Pan head screw #8x32x3/8		
	4	Nuts #8		
	4	Lock washers #8		

7.0 Schematics, Wiring Diagrams, and Component Location

7.1 Introduction.

This section contains schematics, parts pictorials, and wiring information for all non-purchased assembly. This section also contains complete information on the various Plug-in units available.

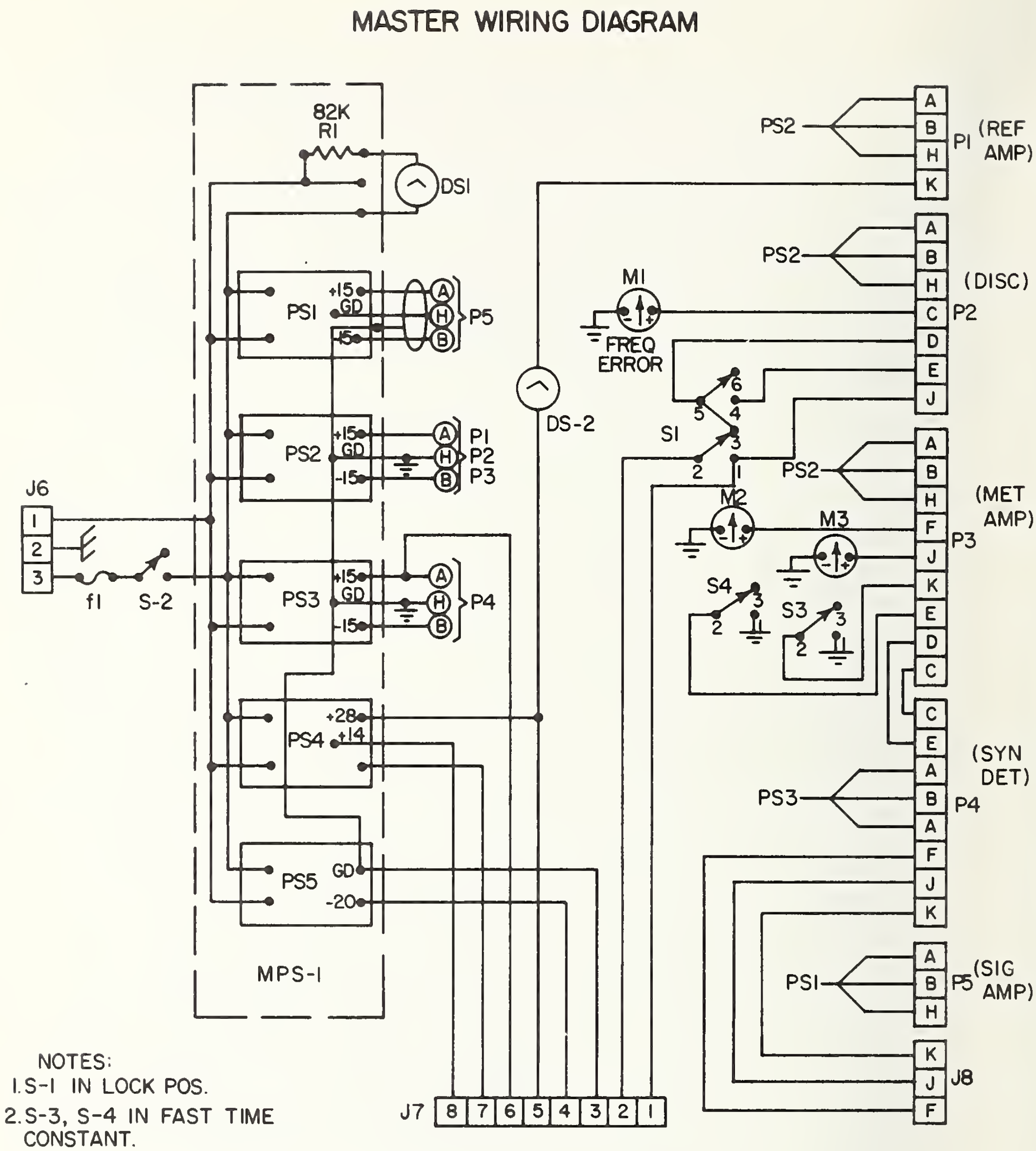


Figure 7.1 NBS/SND master wiring diagram

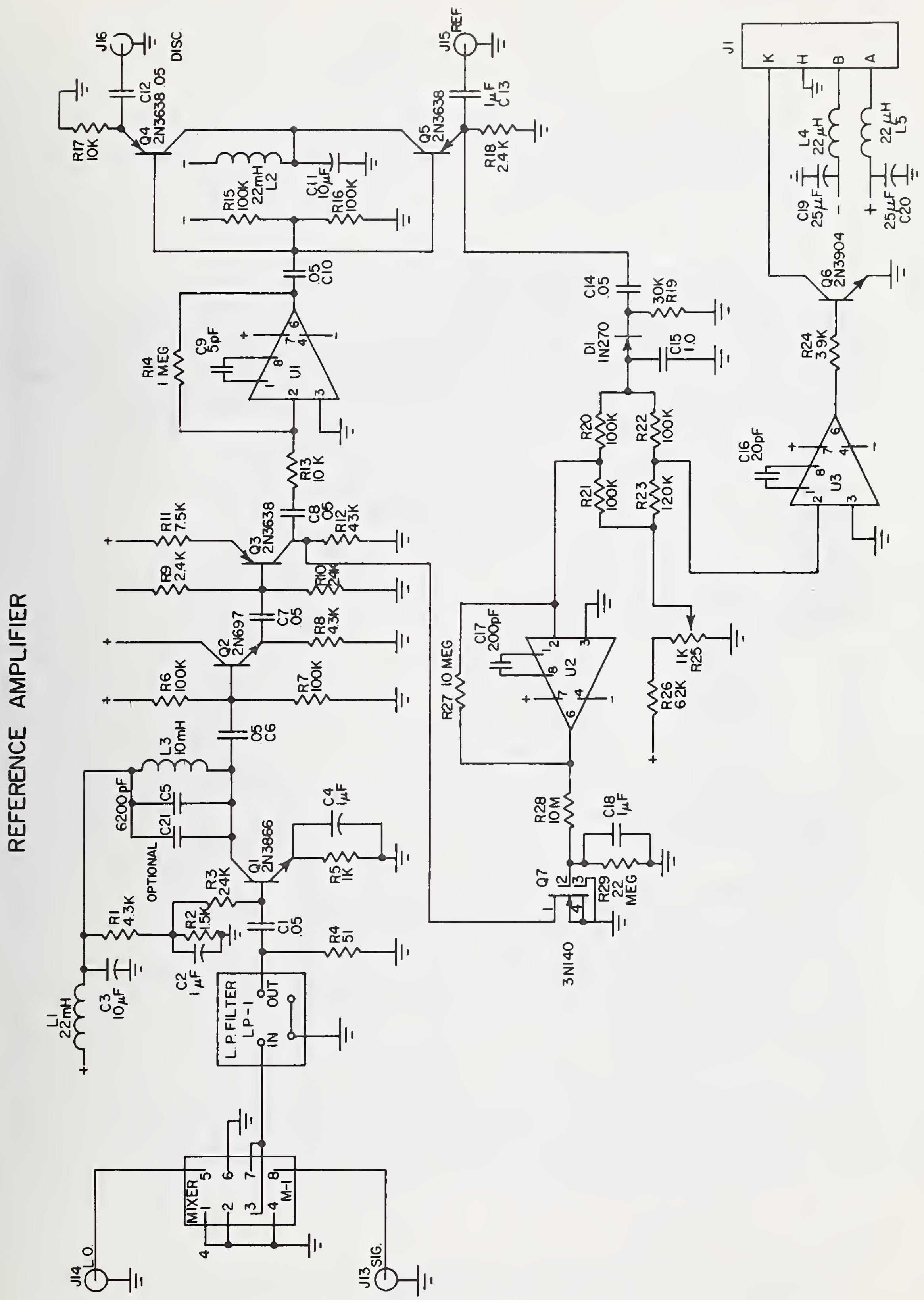


Figure 7.2 Reference amplifier schematic

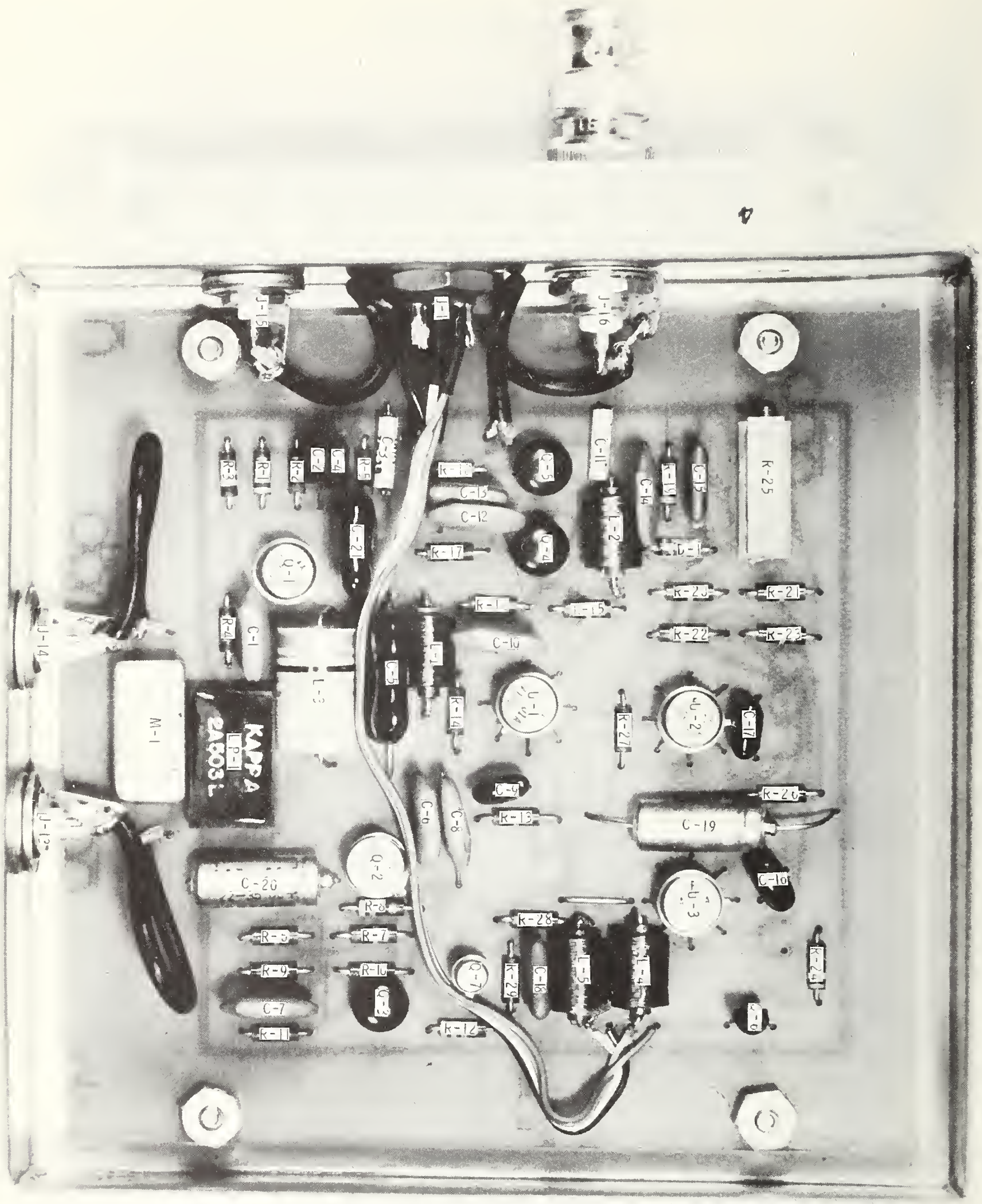


Figure 7.3.   Reference amplifier parts pictorial

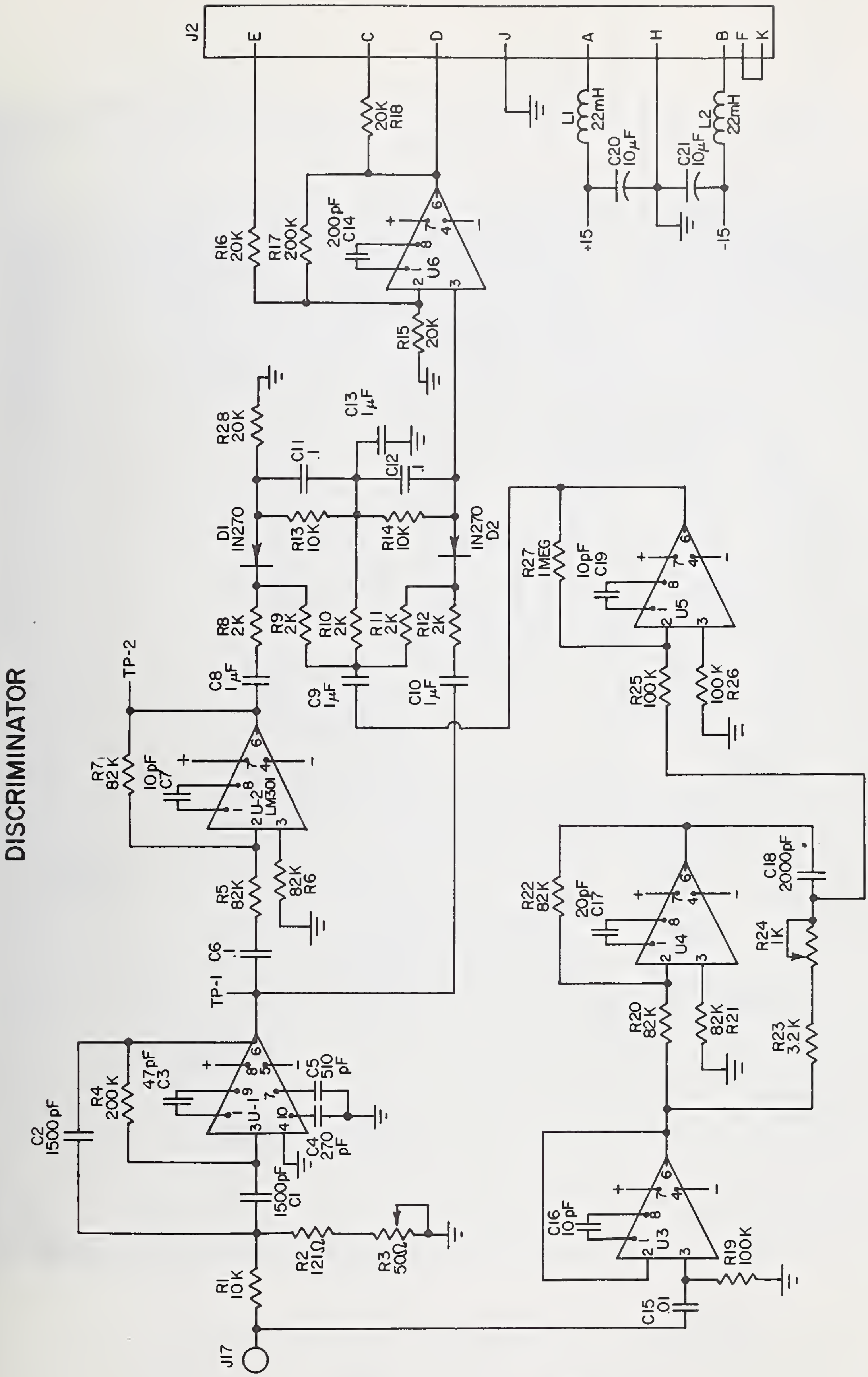


Figure 7.4. Discriminator schematic

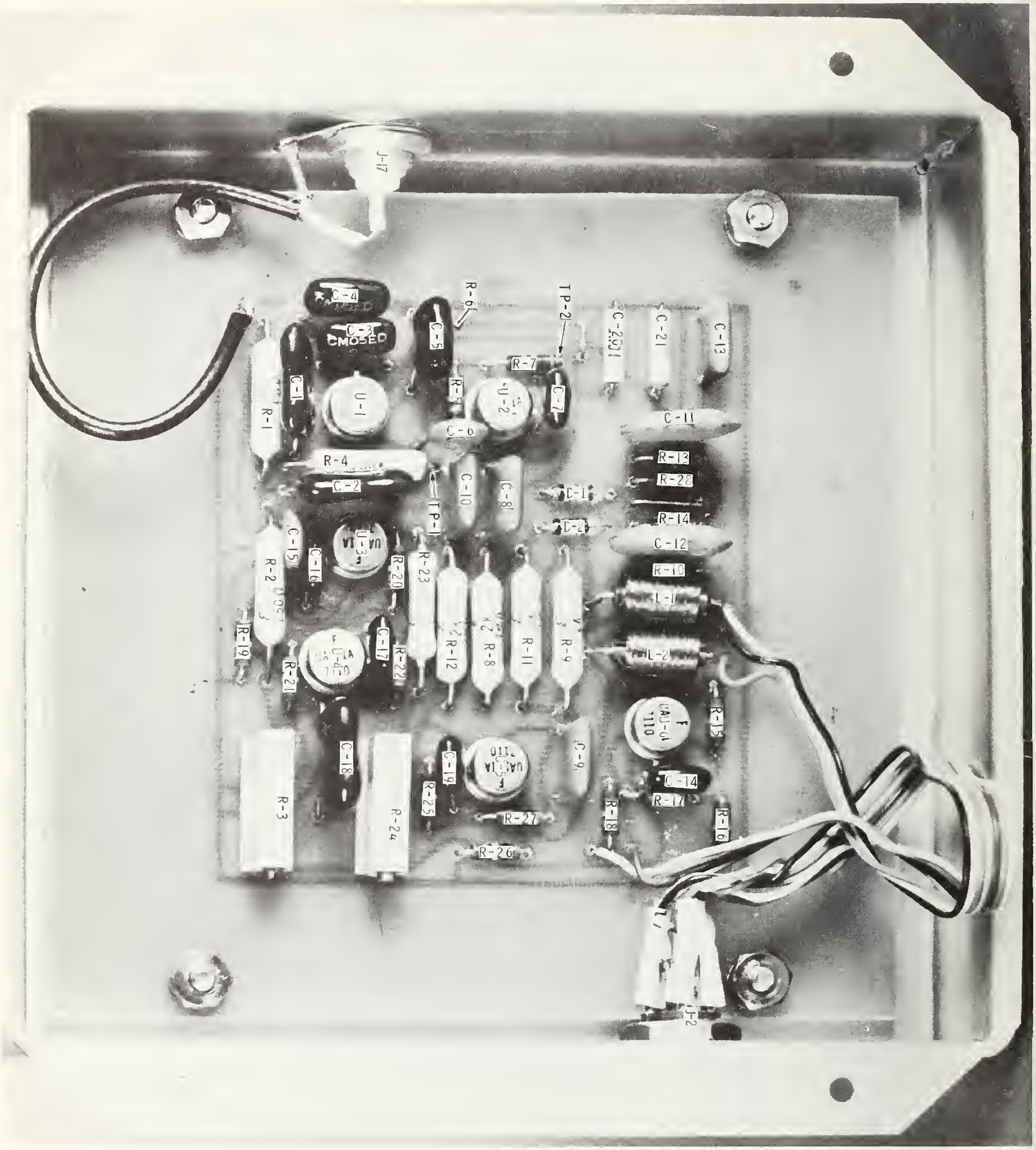


Figure 7.5. Discriminator parts pictorial

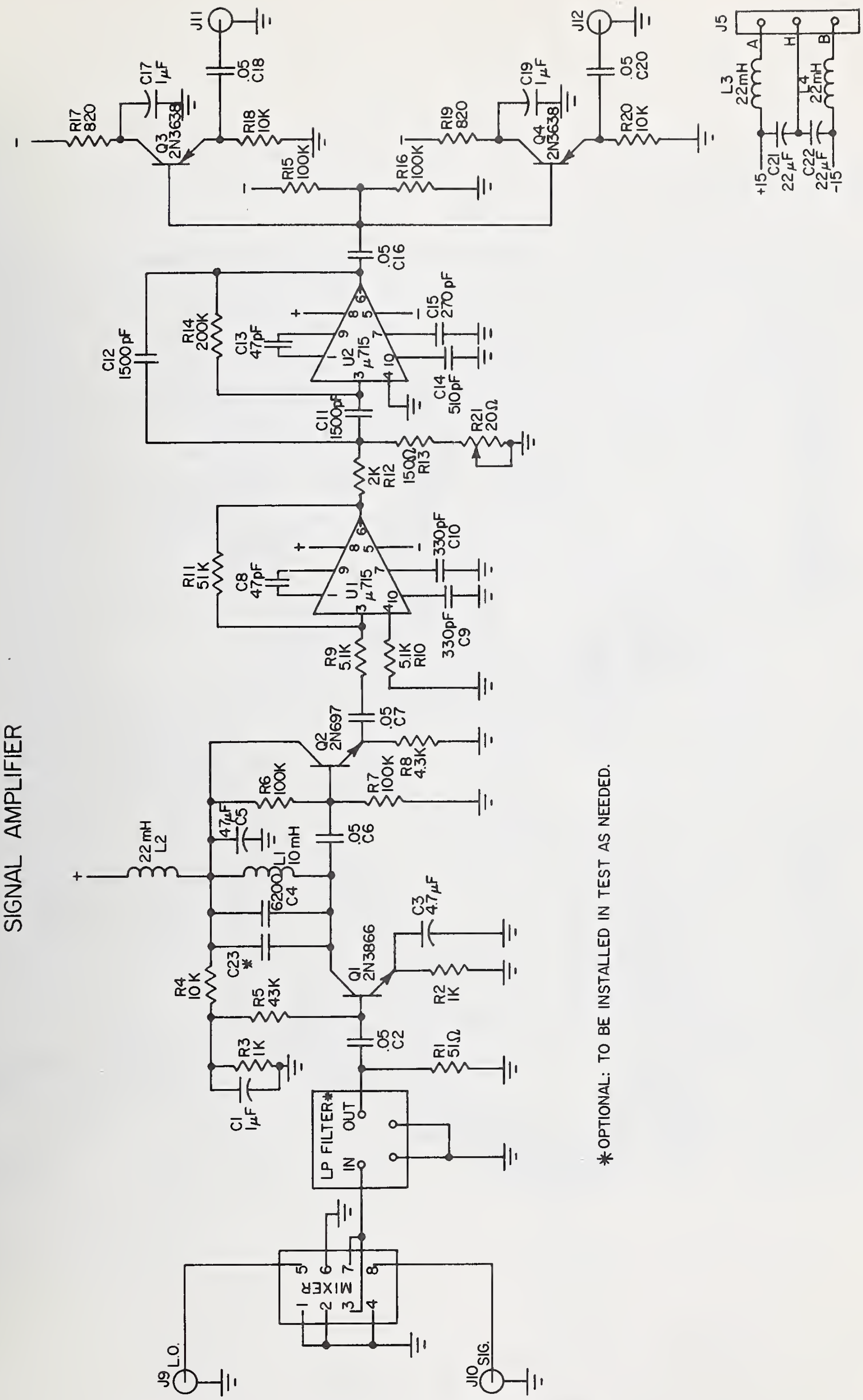


Figure 7.6. Signal amplifier schematic

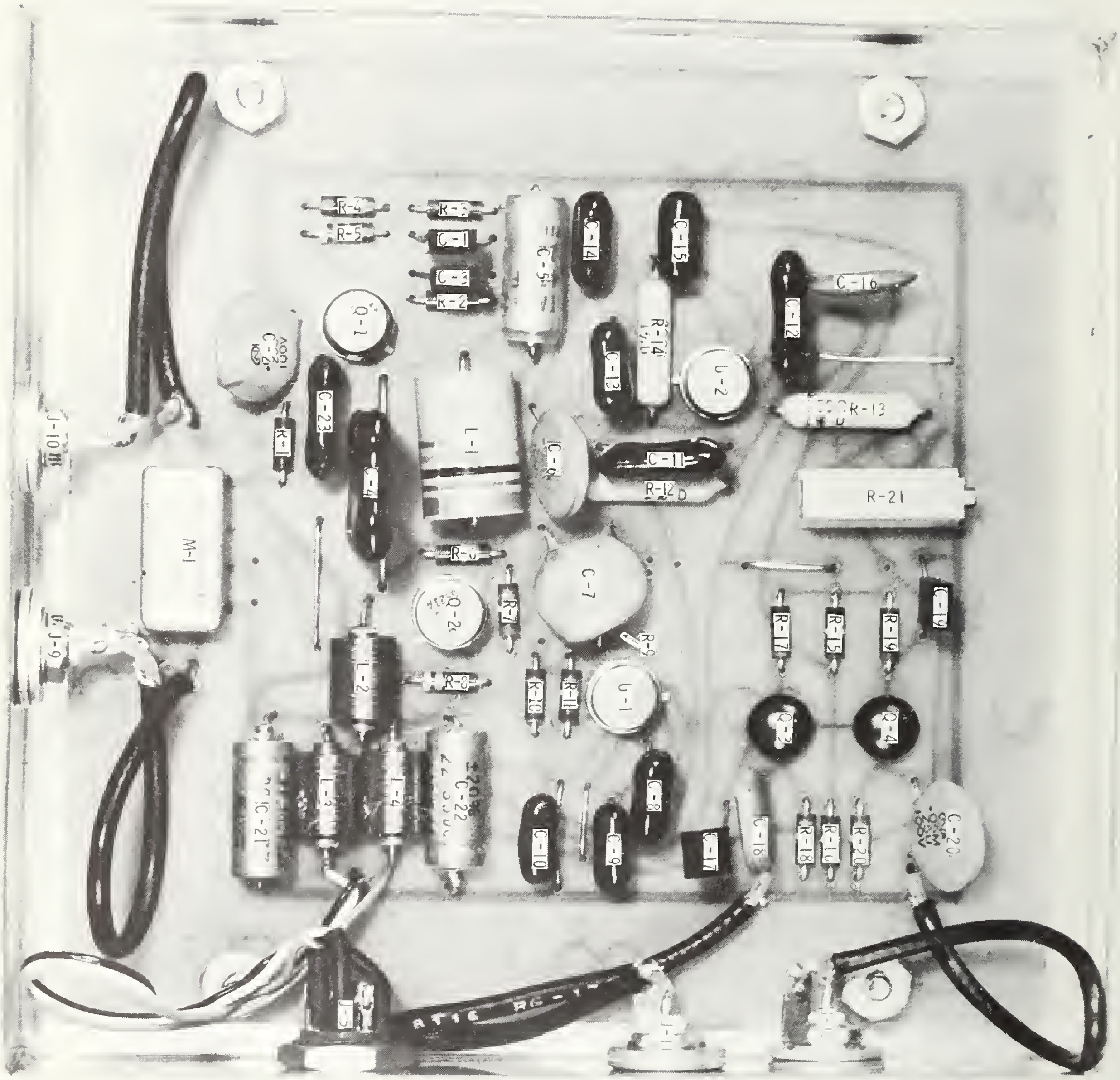


Figure 7.7. Signal amplifier parts pictorial

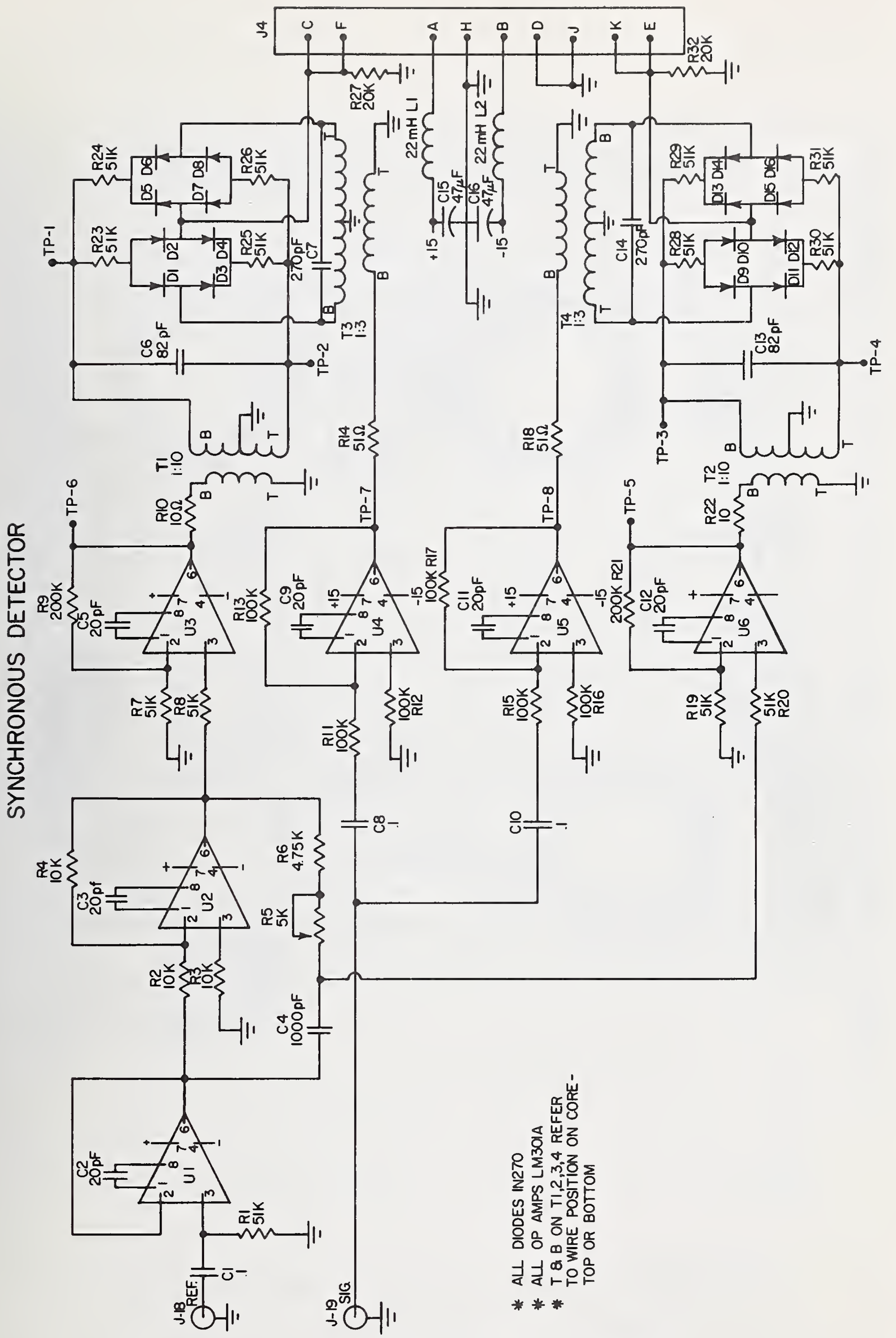


Figure 7.8. Synchronous detector schematic

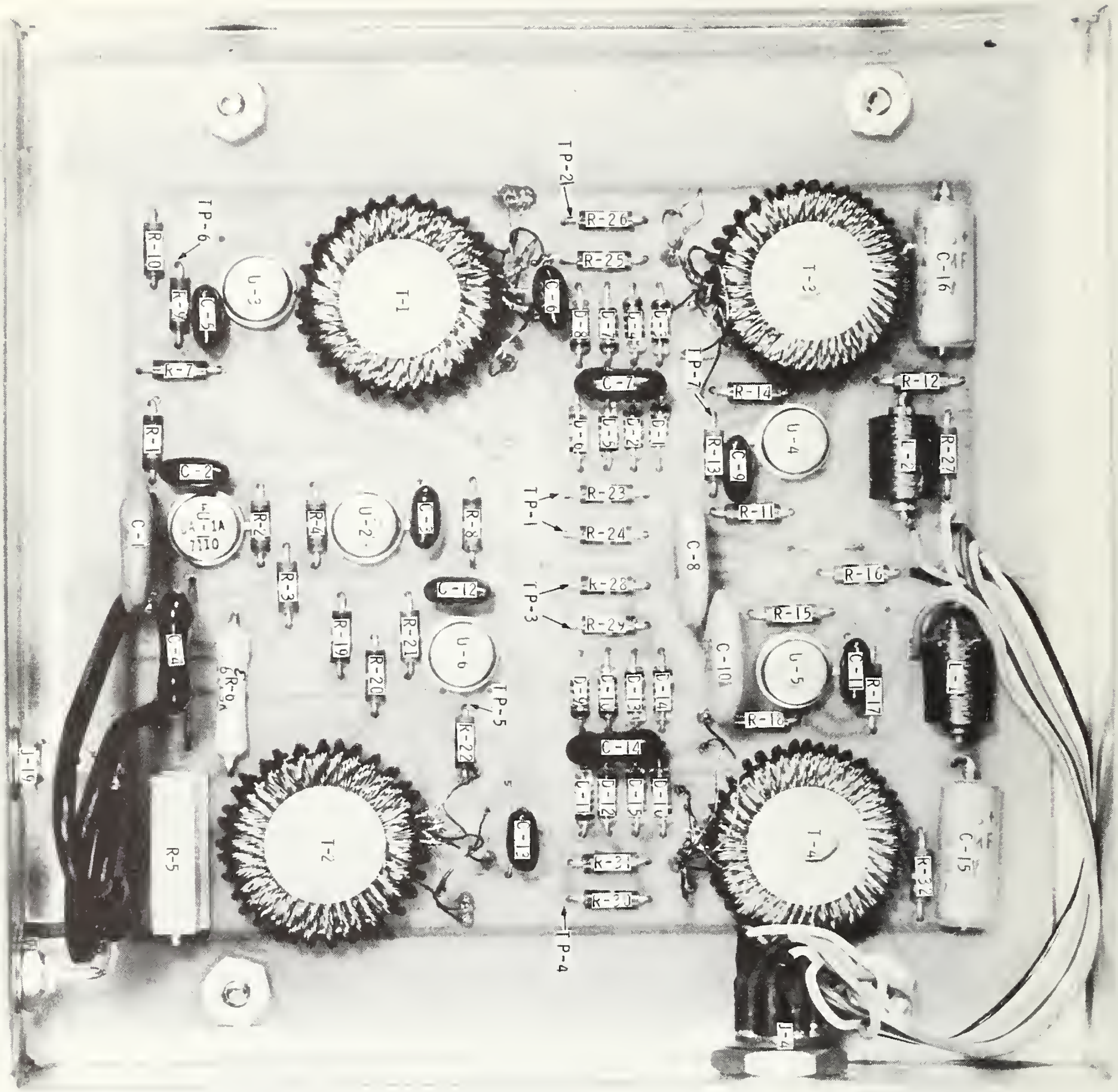


Figure 7.9. Synchronous detector parts pictorial

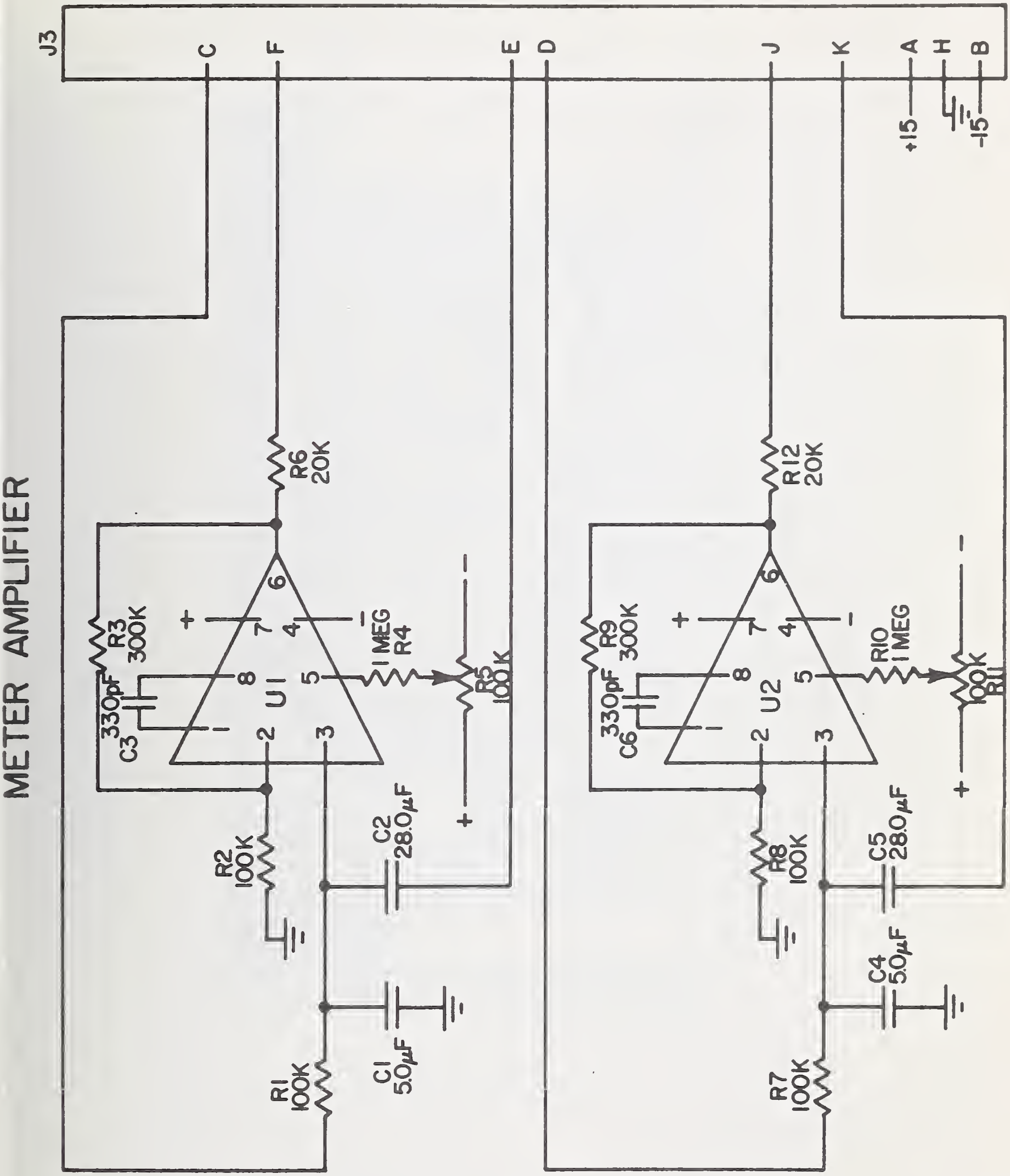


Figure 7.10. Meter amplifier schematic

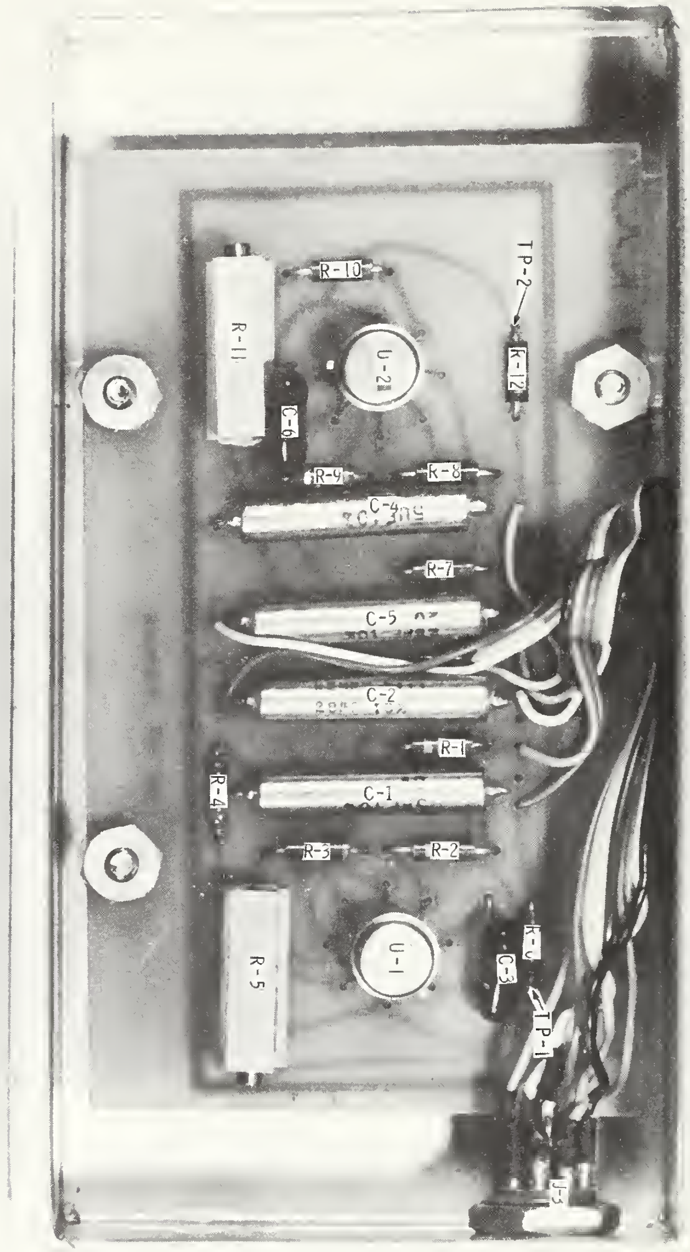


Figure 7.11. Meter amplifier parts pictorial

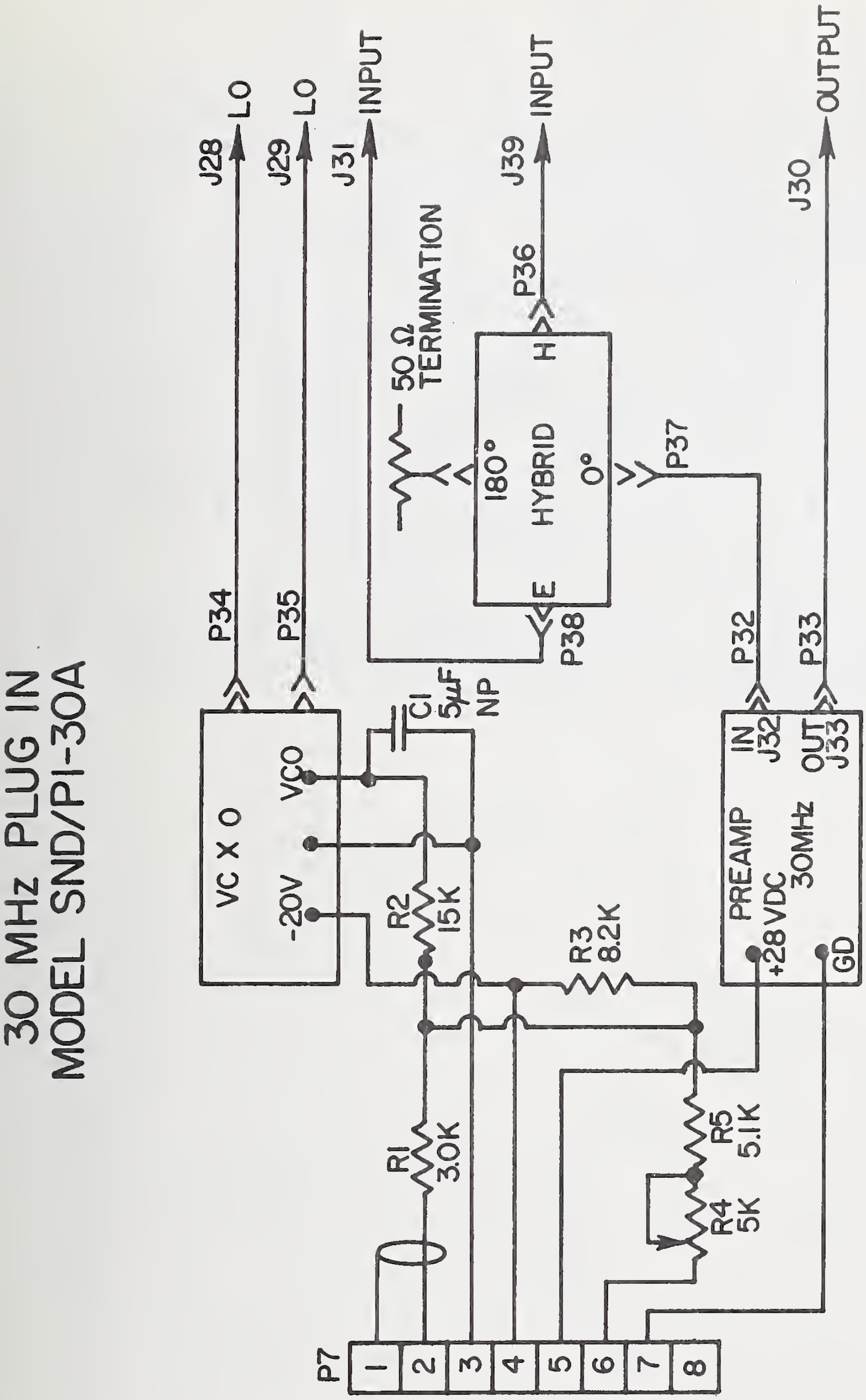


Figure 7.12. SND/PI-30A schematic

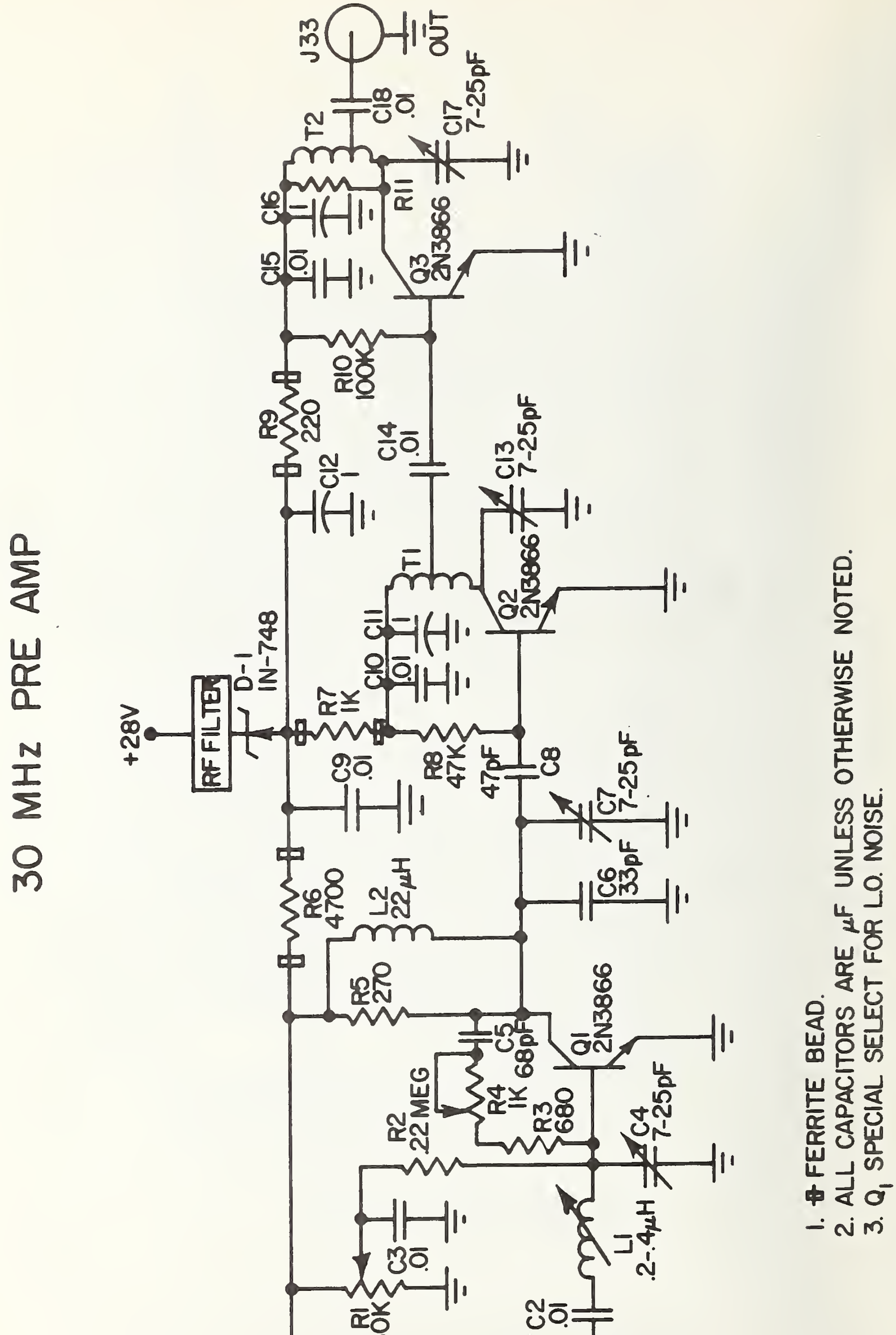


Figure 7.13. 30 MHz Pre Amp schematic

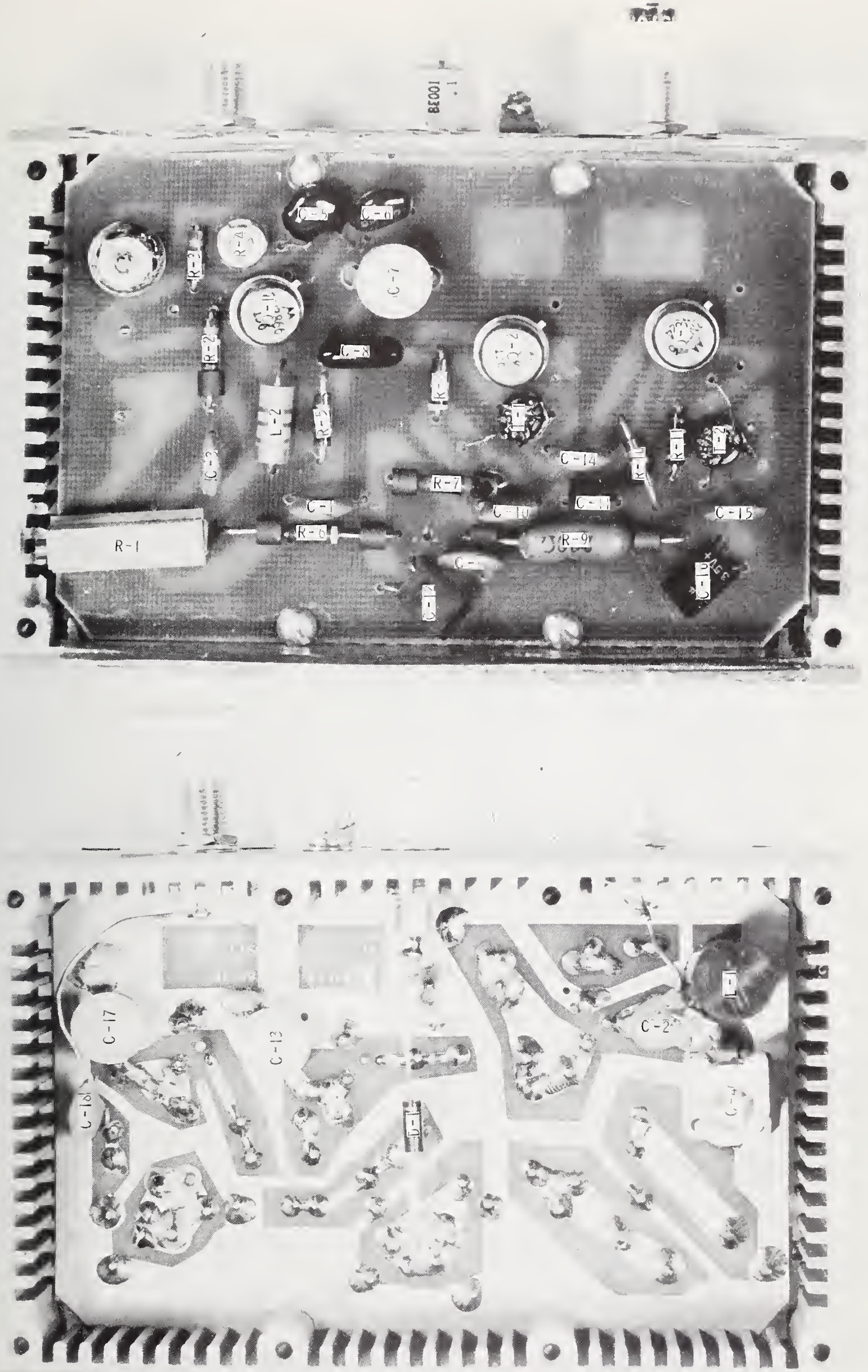


Figure 7.14. 30 MHz Pre Amp parts pictorial

FORM NBS-114A (1-71)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 73-302	2. Gov't Accession No.	3. Recipient's Accession No.
4. TITLE AND SUBTITLE RF NULL DETECTOR NBS/SND			5. Publication Date June 1973
			6. Performing Organization Code
7. AUTHOR(S) Robert E. Stoltenberg			8. Performing Organization
9. PERFORMING ORGANIZATION NAME AND ADDRESS NATIONAL BUREAU OF STANDARDS, Boulder Labs. DEPARTMENT OF COMMERCE Boulder, Colorado 80302			10. Project/Task/Work Unit No. 2724457
			11. Contract/Grant No. CCG No. 71-44A
12. Sponsoring Organization Name and Address ARMY/NAVY/AIR FORCE Calibration Coordination Group			13. Type of Report & Period Covered
			14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This report describes an ultrasensitive receiver for detecting low-level rf signals in the nanovolt region. The primary purpose of the instrument is to detect the balance condition in rf bridges; however, it is useful in any comparison measurement in which two or more signals can be adjusted in phase and magnitude such that their summation results in a null.

The receiver frequency is determined by individual plug- in units. Units have been built for selected frequencies from 100 kHz through 30 MHz. Detection is accomplished by double conversion. The first converts the signal of interest to a common intermediate frequency; the second performs a dual synchronous (homodyne) conversion. The dual detectors are sensitive to signals in quadrature with each other. A reference voltage synchronous with the null signal is required. Thus, the dual detection provides an indication of both the phase and the magnitude of the null unbalance.

The output of each detector is displayed on a zero-center meter, thus indicating the direction of unbalance as well as the magnitude. This information is also available at a rear panel jack for use in servo control of the external system.

Gain adjustment over a 90 dB range is provided by a single front panel control. Phase adjustment to compensate for differential phase delay between the reference and null signals is accomplished with a front panel 360° continuous phase control.

17. KEY WORDS (Alphabetical order, separated by semicolons)

Detector; phase sensitive; RF null detector.

18. AVAILABILITY STATEMENT	19. SECURITY CLASS (THIS REPORT)	21. NO. OF PAGES
[X] UNLIMITED.	UNCLASSIFIED	
[ ] FOR OFFICIAL DISTRIBUTION. DO NOT RELEASE TO NTIS.	20. SECURITY CLASS (THIS PAGE) UNCLASSIFIED	22. Price

USCOMM-DC 66244-P71

USCOMM - ERL