NBSIR 73-271 (R)

Field Service Test Model: Computer-Controlled U System Manual for System

R. J. Carpenter

Electronic Instrumentation
Measurement Engineering
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K. M. Gray
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August 23. 1973

Instruction Manual

Prepared for
Department of the Air Force
HQ - USAF (AFTAC/TAP)
Patrick A. F. B., Florida 32925

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U. S. DEPARTMENT OF COMMERCE, Frederick B. Dent, Secretary

NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, Director

FIELD SERVICE TEST MODEL: COMPUTER-CONTROLLED U SYSTEM MANUAL FOR SYSTEM

by
R. J. Carpenter, K. M. Gray
D. S. Grubb and L. J. Palombo

1. INTRODUCTION

The Field Service Test Model uses a computer to control the operation of from 1 to 15 EECO 881 receivers for unattended operation. Each receiver is connected to the computer by an ADACS (Automatic Data Acquisition Control System) Interface Chassis, which provides the necessary decoding and conversion for communication between the receiver and the computer (see figure 1).

This manual describes the operation of the overall system.

2. GENERAL DESCRIPTION

The purpose of the receivers is to produce a record of the phase of several VLF radio signals over a long period of time. As originally used, each receiver was run independently with its own output recording device and with some operator monitoring of the receiver controls.

The computer-controlled U system uses a small computer to monitor the status of the receiver and its output signal; perform the necessary programmed calculations on the status and signal; manipulate the receiver's controls for proper operation of the

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Certain commercial equipment and materials are identified in this paper in order to adequately specify the components used. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

receiver; and record the phase of the output signal.

The system consists of a minicomputer with a 16-bit word size and 32K words of core memory, several computer peripheral devices (teletypewriters, etc.), an analog subsystem for receiving analog signals from the receivers, a digital subsystem for digital signals to and from the computer, a connector panel, and up to 15 receivers with their attached ADACS Interface Chassis units (see figure 1).

The receiver functions that must be computer-controlled for proper operation of the receivers in unattended usage are: RF gain, uncorrected phase, tracking rate, and blanking level. See figure 2.

2.1 RF GAIN

In manual operation, the RF gain is set by the operator, using the RF Gain control on the front panel of the receiver. In automatic (computer-controlled) operation, the computer controls the RF Gain by monitoring the amplitude of the receiver's output signal and by sending the appropriate gain level information back to the receiver. (The RF Gain control on the front panel of the receiver is deactivated when the receiver is in automatic operation.)

The amplitude is converted into binary bits by the analog subsystem of the computer. The computer specifies the gain level in the form of 5 binary bits. These bits at decoded into 14 lines by the ADACS unit for the operation of relays in the receiver, which select the resistance to be used in the receiver's RF gain circuit.

2.2 PHASE

In automatic operation, the computer monitors the difference between the corrected and uncorrected phase signals of the receiver to determine when to order a phase shift of the uncorrected phase signal. The phase difference is converted into binary bits in the analog subsystem of the computer. When a phase shift is needed, the computer sets the Phase Change bit (15) and generates an output transfer. Each output transfer is accompanied by a flag, which is a 10-microsecond pulse. The Phase Change bit and the flag pulse are used by the circuitry in the ADACS unit to generate a 10-microsecond Phase Change Pulse, which is sent to the receiver to shift the uncorrected phase signal 50 microseconds.

2.3 TRACKING RATE

In manual operation, the tracking rate of the receiver is adjusted using the Tracking Rate switch on the front panel of the receiver. In automatic operation, the computer uses the peak-to-peak noise (phase variation) on the phase output of the receiver to determine the tracking rate for the receiver.

The computer specifies the tracking rate in the form of 4 binary bits. These bits are decoded into 6 lines by the ADACS unit for the operation of relays in the receiver, which select the receiver's tracking rate.

2.4 BLANKING LEVEL

In manual operation, the Blanking Level control on the front panel of the receiver is set by the operator. In automatic operation, the computer monitors the blanking pulses from the receiver to determine the blanking level for the receiver. (The Blanking Level control on the front panel of the receiver is deactivated when the receiver is in automatic operation.)

The blanking pulses from the receiver are converted into an analog voltage level by circuitry in the ADACS unit. The voltage is called Blanking Percentage and it is converted into binary bits by the analog subsystem of the computer. The computer specifies the blanking in the form of 6 binary bits. These bits are converted into an analogblanking level voltage by the ADACS unit for use by the receiver.

2.5 FREQUENCY

The frequency of the receiver is always determined by the setting of the Channel Select switches on the front panel of the receiver. The setting of the switches is monitored by the computer.

2.6 OPERATIONAL STATUS

A change in the operational status of a receiver will cause a computer interrupt. Since a single interrupt line is shared by all of the receivers, when the computer receives an interrupt it must examine the status lines for each of the receivers to determine which has changed its status. The status lines are for INE (Invalid Data Equipment sensed), Manual/Automatic switch, and Maintenance/ Normal switch.

2.7 MANUAL/AUTOMATIC SWITCH

The Manual/Automatic switch is on the front panel of the ADACS Interface Chassis. Its output is used by both the receiver and the computer.

2.8 MAINTENANCE/NORMAL SWITCH

The Maintenance/Normal switch is on the front panel of the ADACS Interface Chassis. Its output is used only by the computer (as a status indicator).

2.9 CARDIOID

The three binary bits from the cardioid are monitored by the computer. A change in the least significant bit will cause an interrupt to the computer, which will then examine the status of digital input word that contains the three bits.

3. SYSTEM COMPONENTS

The system components consist of the computer subsystem; the real-time clock; the a-c power loss detector; the missing pulse detector; the receivers and ADACS Interface Chassis units; and the Test Unit. All except the Test Unit are shown in figure 1.

3.1 COMPUTER SUBSYSTEM

The computer subsystem consists of the CPU (central processing unit), the computer peripherals (teletypewriters, paper tape reader, etc.), the analog subsystem, the digital subsystem, and the connector panel.

The computer subsytem is described in the Manual for Computer Subsystem. The computer is a general-purpose digital computer with a 16-bit word size and 32 K words of core memory.

3.2 REAL-TIME CLOCK

A real-time clock is attached to the system via the digital portion of the Connector Panel. The clock uses a Cesium beam standard and may be set to an accuracy of one microsecond. It generates an interrupt to the computer every second and every minute. As used with this system, it provides time information in days, hours, minutes, and seconds (see figures 8 and 9).

3.3 A-C POWER LOSS DETECTOR

The power loss detector is shown in figure 10. It is used to alert the operator in the event of a power failure.

3.4 MISSING PULSE DETECTOR

The missing pulse detector (figure 11) is used to detect the condition that exists when the computer, due to a programming error or computer malfunction, is locked in a program loop. Since the computer program is no longer controlling the system when it is in this state, an external detector is needed to return the receivers to manual operation.

The missing pulse detector circuit receives a 10-microsecond pulse from the computer at least once every 20 seconds from the flag bit (the pulse generated on all digital output transfers). As long as these pulses occur, the retriggerable one shot circuit, NE555, will be on. The output of the NE555 circuit is used by the optical isolator circuit, TI 112, to provide the gate voltage for the SCR (silicon-controlled rectifier), which completes the circuit to the relay. When the relay is energized, it connects the input power to the ADACS units.

If the computer becomes locked in a program loop, it will no longer be generating output pulses. Without these pulses, the NE555 circuit will time out and drop its output to the optical isolator. Without its input, the optical isolator will no longer provide the gate voltage for the SCR, and the SCR will open the circuit to the relay. When the relay circuit is opened, the relay contacts will disconnect the power to the ADACS units. The loss of power to the ADACS units will cause the Manual/Automatic relays in the various receivers to drop to the Manual position, thereby forcing the receivers into the manual mode of operation.

3.5 RECEIVERS AND ADACS INTERFACE CHASSIS UNITS

The receivers and ADACS units are described in the Manual for Receiver and ADACS Interface Chassis. Up to 15 receivers may be attached to the system.

3.6 TEST UNIT

The Test Unit is not a part of the operational system, but is used for maintenance of the receiver and ADACS units. The Test Unit is described in the Manual for Test Unit.

4. SYSTEM INTERFACES

The interfaces between the component units of the system are shown in figure 1. Interfaces within the computer subsystem are shown in the Manual for Computer Subsystem and are covered in detail in the manuals supplied by the computer manufacturer. The interfaces between the receiver, the ADACS Interface Chassis unit, and the Connector Panel are shown in more detail in figure 2. The unit/detachment input is merely a connector wired to denote the appro-

priate number.

4.1 CABLING AND PIN ASSIGNMENTS

The cable connections for the system are shown in figures 3 and 4. The receiver and the ADACS Interface Chassis are interconnected as shown in figure 3. The dotted lines within the box for the ADACS unit show relationships between inputs and outputs. The interrupt lines are "daisy-chained" from unit to unit, so that only a single line is sent to the Connector Panel.

The assignment of cable connectors on the Connector Panel to the various receivers and other units is shown in figure 4. The LSB (least significant bit) of the cardioid information from each ADACS unit (pin number P in the cable) is wired to the Common Alarm card (1191) of the computer subsystem's I/O Digital Interface (1100). The output of the alarm is wired to interrupt number 8.

Pin assignments for the various cables are shown in figures 5 through 9.

4.2 ELECTRICAL

The digital signals of the system all use TTL levels. A logical "one" is nominally plus 5 volts and a logical "zero" is at ground.

There are three types of analog signals used between units of the system: phase difference, amplitude, and blanking percentage. The phase difference signal has a voltage range of from zero to plus 10 volts. The amplitude signal has a voltage range of from zero to plus 7.816 volts. The blanking percentage signal has a voltage range of from zero to plus 10 volts.

4.3 MECHANICAL

The connector part numbers and other mechanical details are covered in the manuals on the associated units. The construction of cables using BNC connectors is common to the system and is shown in figure 12. The construction of cables using multi-pin connectors is also common to the system and is shown in figure 13.

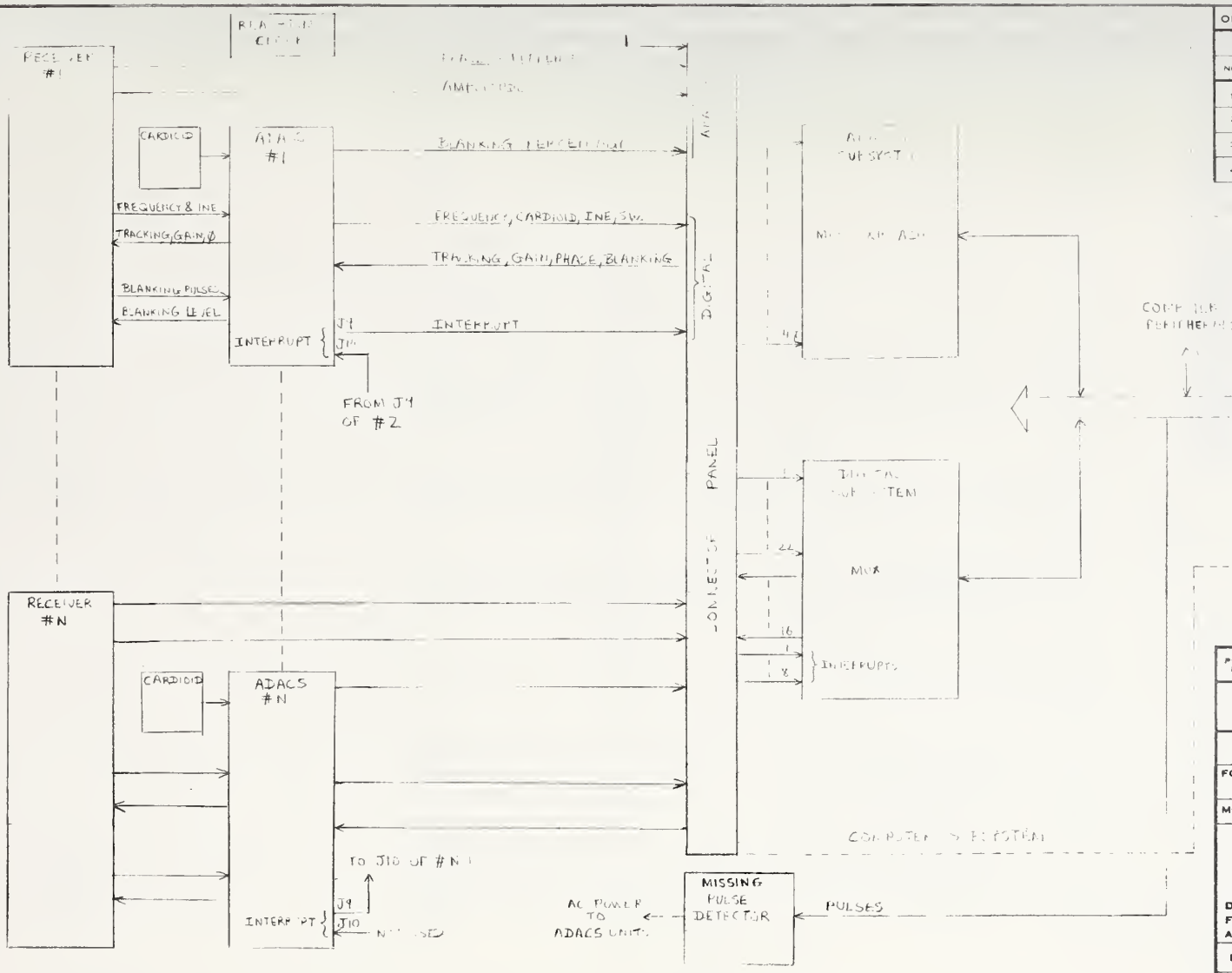
5. COMPUTER WORD ASSIGNMENTS

The digital inputs to the Connector Panel (frequency, cardioid, INE, and the switch settings in the ADACS unit) are formed into a word for the computer. This is shown in figure 5.

The digital outputs from the Connector Panel (tracking rate, RF gain, blanking level and phase) are generated from a computer word, which is shown in figure 6.

The analog inputs to the Connector Panel (phase difference, amplitude and blanking percentage) are each used (in turn) as the input to the analog-to-digital converter in the analog interface to generate digital bits, which are formed into a word for the computer. The bits are arranged with the least significant bit from the converter as bit 15 and the remaining bits in order of increasing significance.

The real-time clock provides time information in terms of day, hour, minute and second. The two words are shown in figures 8 and 9.



OVERALL SYSTEM

FIGURE 1

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OVERALL SYSTEM

FOR

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DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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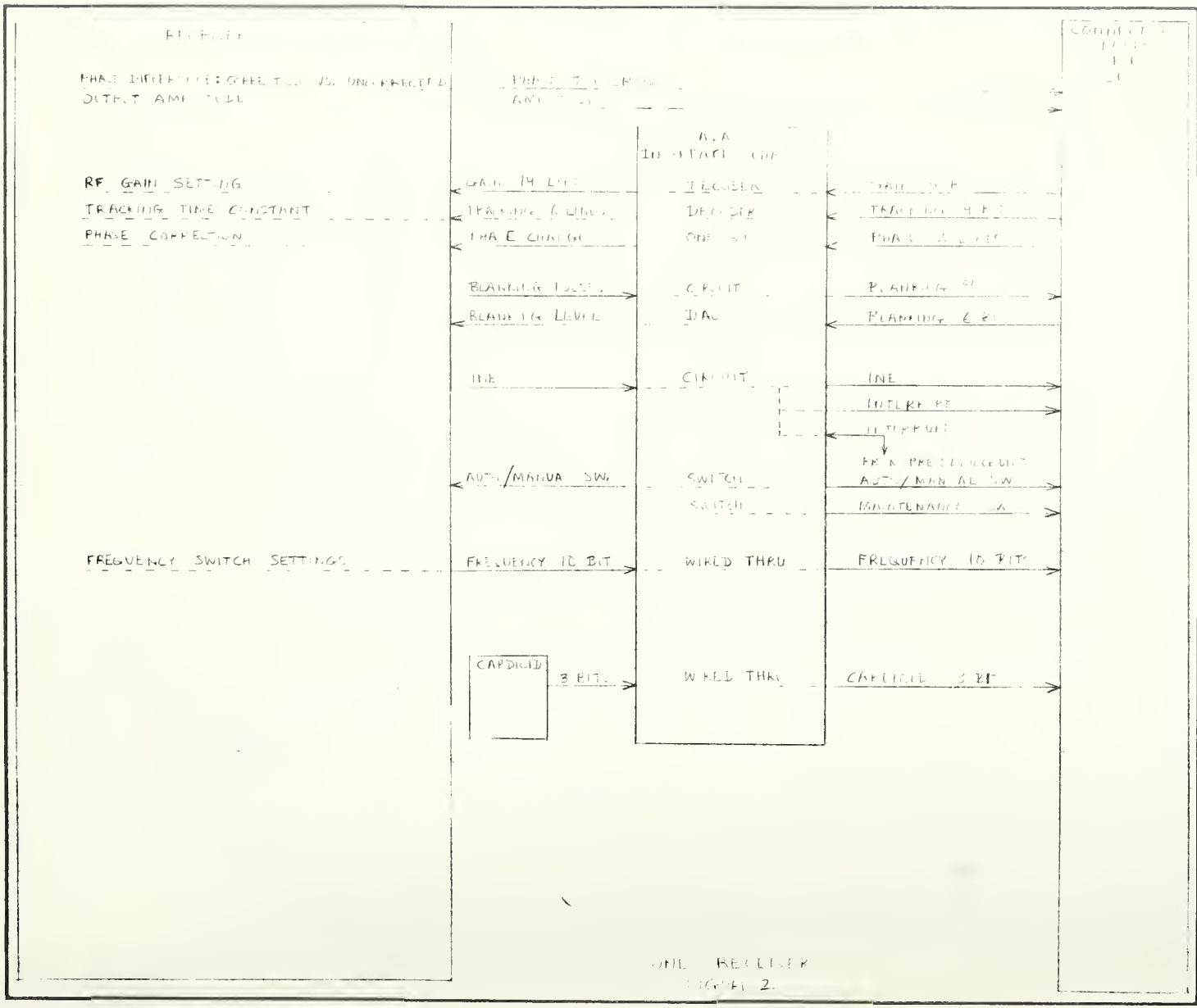

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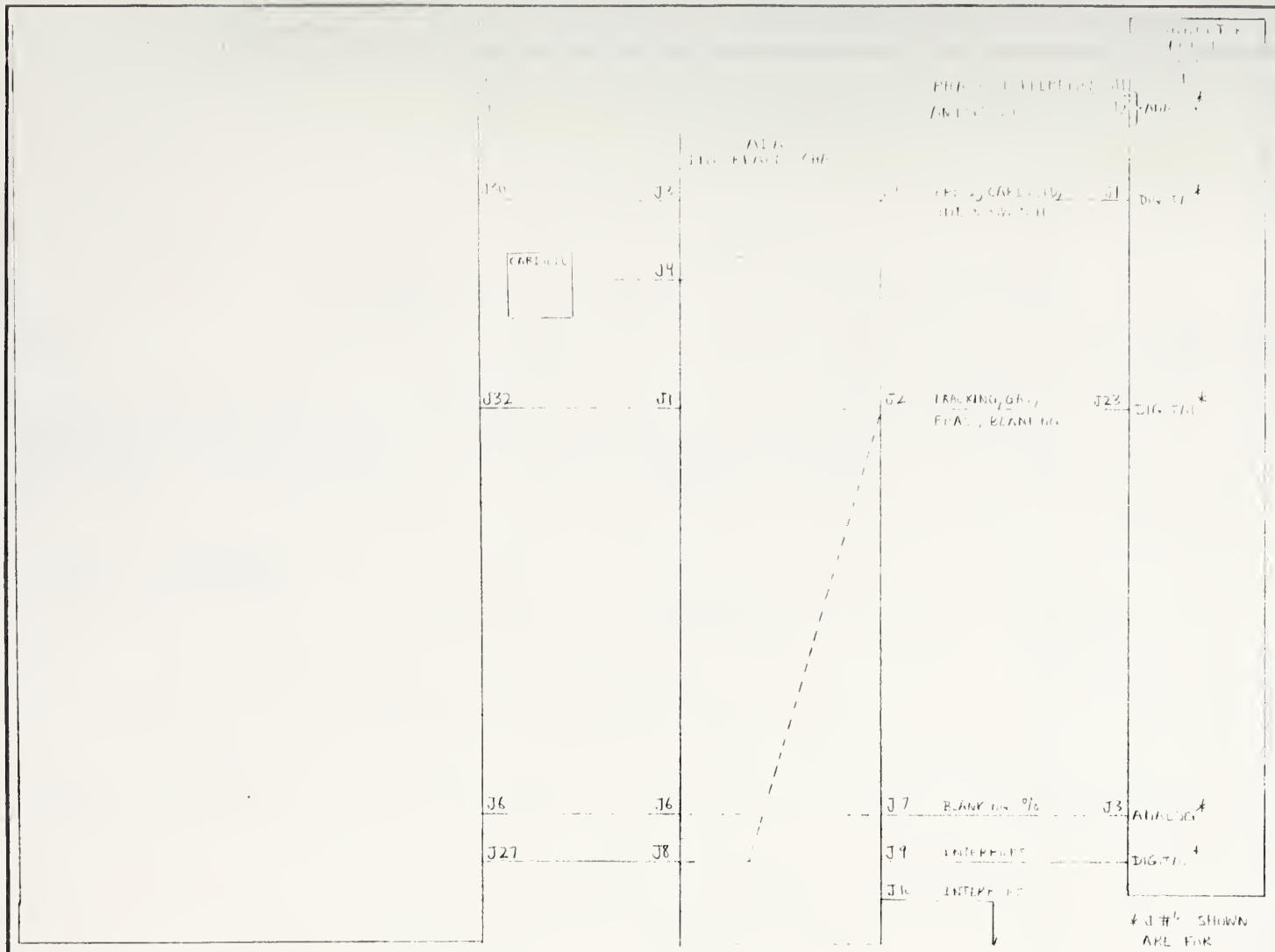

CABLING FOR RECEIVER & ADACS

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CABLING FOR RECEIVER & ADACS

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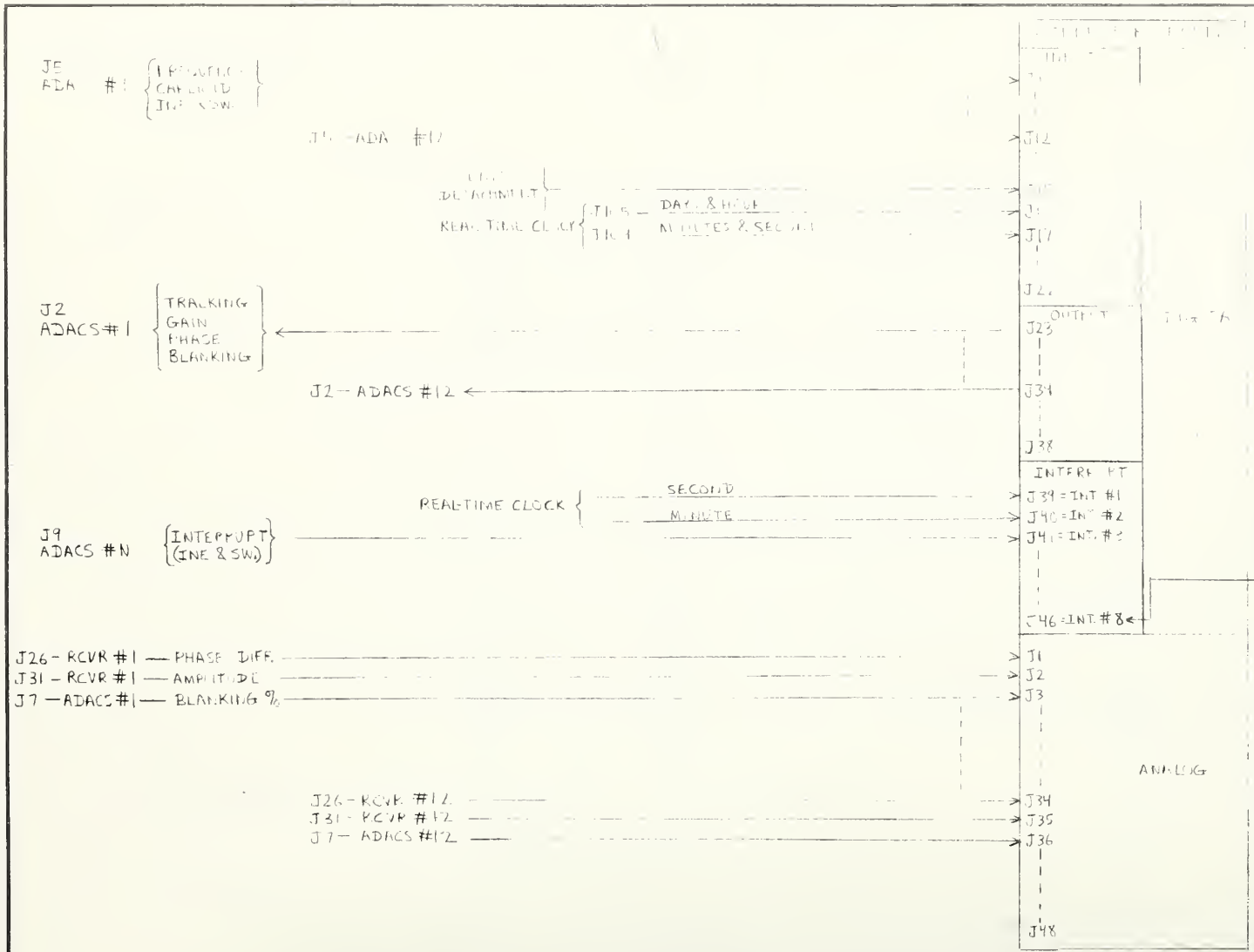

CONNECTOR PANEL CABLING

FIGURE 4

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CONNECTOR PANEL CABLING

FOR

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CPU BIT #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15					
FUNCTION	FREQUENCY										CABLE		INH.	NOT	A	GROUND					GROUND
CABLE* PIN #	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	
CHANNEL SELECT SW. IN RECEIVER	MSD		MIDDLE DIGIT				LEAST SIGNIFICANT DIGIT														
	2	1	8	4	2	1	8	4	2	1											

* CPU TO ADACS

DIGITAL INPUT W[illegible]
[illegible] CABLE TO CABLE + PANEL
[illegible]

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[illegible] INPUT W[illegible]

FOR

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CPU B.T #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	FLAG
FUNCTION	TRACKING RATE				RF GAIN					BLANKING LEVEL						PHASE BT	FLAG PULSE	—	—	GP. IND
CPU CONN. PIN #	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	W	U	V	X
ADACS CONN. PIN #	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T		V	W	X
				LSB					LSB						LSB					
2^N	3	2	1	0	4	3	2	1	0	5	4	3	2	1	0					

DIGITAL OUTPUT WORD

OUTPUT CABLING FROM CONNECTOR PANEL

FIGURE 6

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DIGITAL [illegible]

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J32 PIN #		J1 PIN #	
A	W-[illegible]	A	[illegible]
B	W-[illegible]	B	[illegible]
C	W-BK	C	[illegible]
D	W-BK	D	[illegible]
E	W	E	[illegible]
F	W-BL	F	[illegible]
H	[illegible]	H	GRAIN [illegible] 1
J	BK	J	[illegible] 2
K	R	K	[illegible] 3
L	W-V	L	[illegible] 4
M	W-GY	M	[illegible] 5
N	W-GRA	N	[illegible] 6
P	W-GR	P	[illegible] 7
R	W-[illegible]	R	[illegible] 8
S	V	S	[illegible] 9
T	BLUE	T	[illegible] 10
U	GR	U	[illegible] 11
V	W-BK-BK	V	[illegible] 12
W	W-R	W	[illegible] 13
X	GRAY	X	[illegible] 14
Y	OR	Y	PHASE CHANGE PULSE
Z	W-V-BK	Z	MAINT./NORMAL
a	W-BK	a	AUTO / MANUAL
b	W-BK-R	b	+5 VOLTS
c	SHIELD	c	DIGITAL GR [illegible]
d	W-BK-GRA	d	—
e	BK	e	—
f	W-BLUE-BK	f	—

J1 PIN #		J2 PIN #	
A	[illegible]	A	[illegible]
B	[illegible]	B	[illegible]
C	R [illegible]	C	[illegible]
D	[illegible]	D	[illegible]
E	BK [illegible]	E	[illegible]
F	W	F	[illegible]
H	[illegible]	H	[illegible]
J	R	J	[illegible]
K	[illegible]	K	[illegible]
L	[illegible]	L	[illegible]
M	[illegible]	M	[illegible]
N	SHIELD	N	DIGITAL GR [illegible]
P	W-BK	P	—
R	BLUE	R	—
S	W-R	S	—
T	[illegible] BK	T	—
U	R-BK	U	—
V	BLUE [illegible]	V	—
W	[illegible]	W	
X	SHIELD	X	DIGITAL GROUND

ADACS J4 PIN #	CABLE [illegible]	DESTINATION
A	H	CARRIED BIT IC
B	A	[illegible]
D	B	[illegible]
E	D	GROUND
H	E	+5 VOLTS

RECEIVER, CABLES, & ADACS CABLE

FIG. 11-7

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	RECEIVER, CABLES & ADACS CABLE	
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WORD 0

REAL-TIME CLOCK CONNECTOR

LSI BIT #	0											11	12	13	14	15				
TIME	DAYS X 100																			
2^N	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	GRD	—	—	—
CPU CONN. PIN #	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	X	U	V	W
COLOR CODE	GRN/BK	WHT	BLU	WHT	RED	RED	WHT	GRN	GRN	ORG-BK	WHT	BRN	GRN	GRN	BLUE	YEL	BRN (SHIELD)	BRN (SHIELD)	BLUE	GRN-WHT
RTC CONN. P.N. # J105	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	X	U	V	W

REAL-TIME CLOCK WORD 0 &
CABLING TO CONNECTOR PANEL
RIGHT X

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REAL TIME CLOCK WORD 0

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REAL-TIME C[illegible] CONNECTOR J104

CPU BIT #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TIME	NOT USED		MINUTES x 10			MINUTES				HOURS x 10			SECONDS			
2^N	—	—	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	GF	M	—	—
CPU CONN. PIN #	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	X	V	W		
COLOR CODE	BK (SHIELD)	BK (SHIELD)	GRN-BK	W-BK	BLUE	W-BK	R-BK	R-W	ORN	[illegible]	R	[illegible]	W	BK-W	GRN	R, GRN	BK (SHIELD)	BK-W	GRN-W		
RTC CONN. PIN # J104	A	B	T	S	K	P	N	M	L	K	J	H	F	E	D	C	X	V	W		

R M [illegible] CLOCK W R D 1 X
CABLING TO CONNECTOR PANEL
FIGURE 1

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REAL-TIME CLOCK W R D 1

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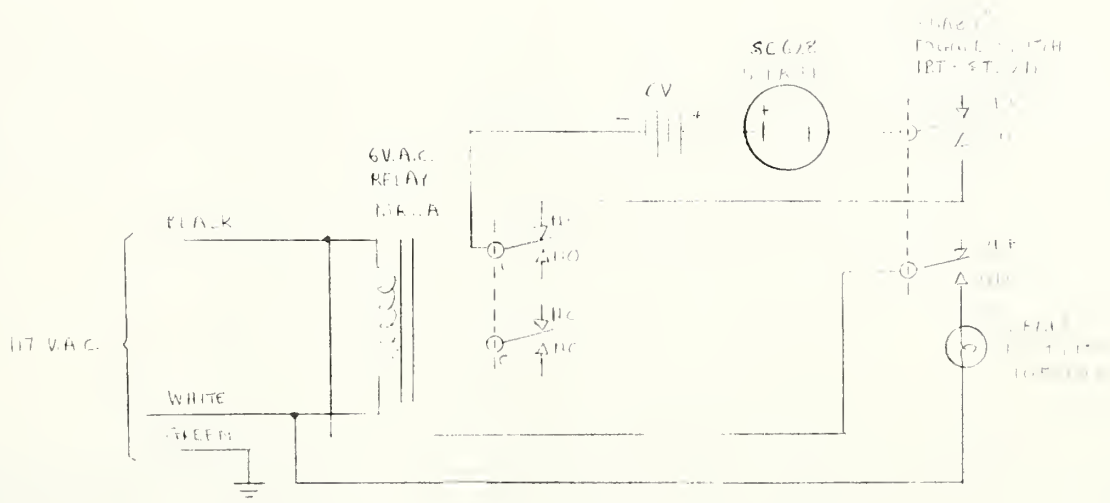

A-C POWER LOSS DETECTOR

FIGURE 10

PIECE NO	NOMENCLATURE	NO REQ'D
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	A-C POWER LOSS DETECTOR	
	FOR	

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
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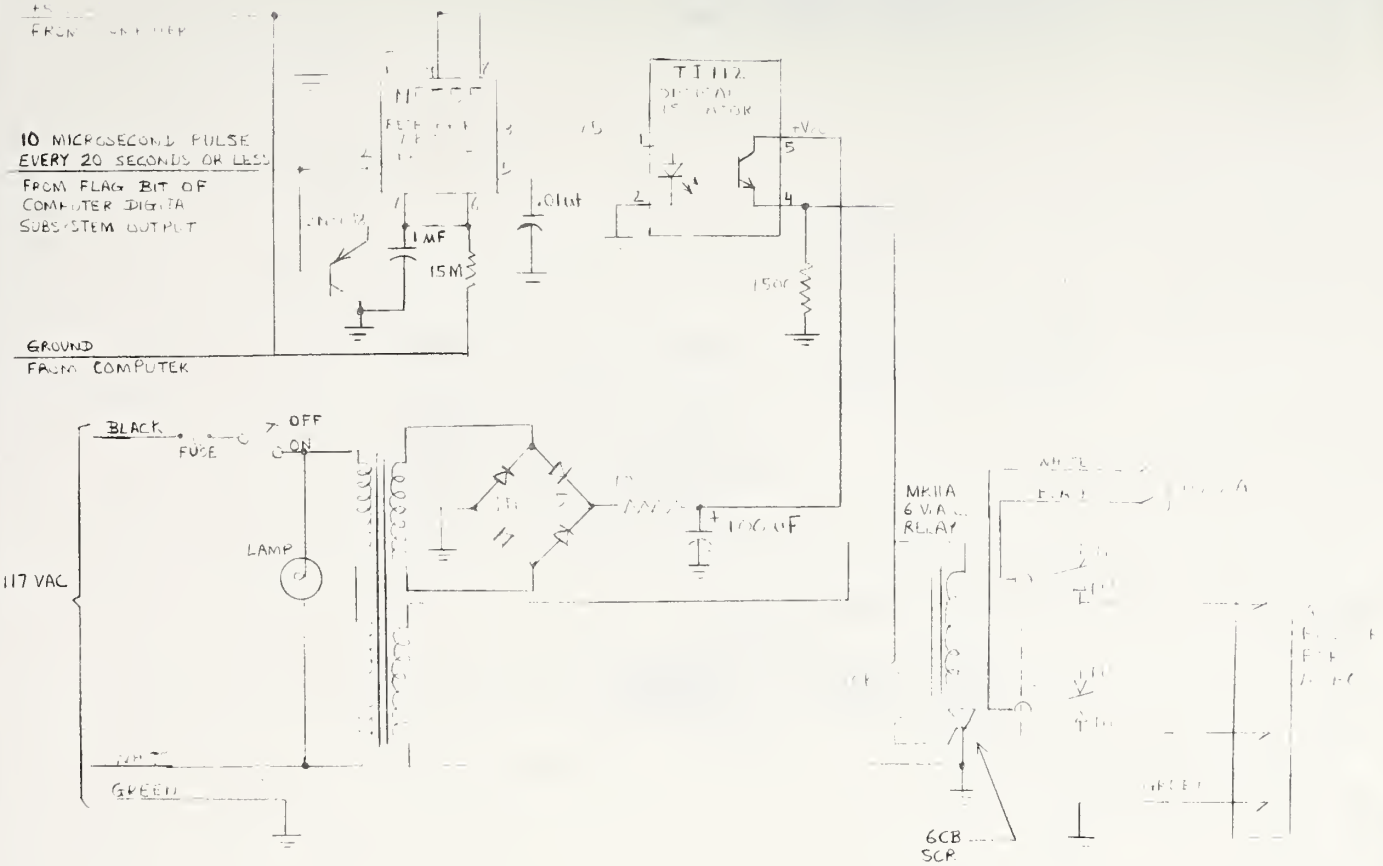

MISSING PULSE DETECTOR

FIGURE 11

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

MISSING PULSE DETECTOR

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.016		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
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ORIGINAL DATE OF DRAWING			
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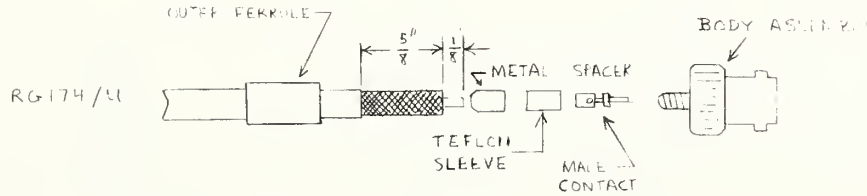

1. STRIP TO THE ABOVE DIMENSIONS.
2. SLIDE ON OUTER FERRULE.
3. SLIDE THE METAL SPACER AND TEFLON SLEEVE ON BETWEEN BRAID AND CENTER CONDUCTOR
4. CRIMP ON MALE CONTACT.
5. CRIMP ON BODY ASSEMBLY.

BNC CABLE CONSTRUCTION
FIGURE 12

PIECE NO.	NOMENCLATURE	NO. REQ'D

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BNC CABLE CONSTRUCTION

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
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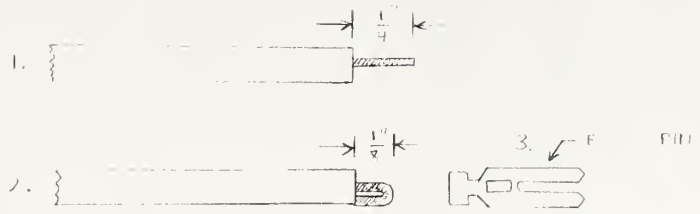

1. STRIP BACK 1/4"

2. FOLD BACK 1/2"

3. CRIMP ON ELCO PIN

20 CONDUCTOR CABLE CONSTRUCTION

FIGURE 13

PIECE NO	NOMENCLATURE	NO REQ'D

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20 CONDUCTOR CABLE CONSTRUCTION

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
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FORM NBS-114A (1-71)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 73-271	2. [illegible]	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

FIELD SERVICE TEST MODEL: COMPUTER-CONTROLLED U SYSTEM MANUAL FOR SYSTEM

5. Publication Date: August 23, 1973

6. [illegible]: 650.01

7. AUTHOR(S)

8. Performing Organization: NBSIR 73-271

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project, Task, Work Unit No.: 6505413

11. Contract/Grant No.: AFTAC T/230/U/NES

12. Sponsoring Organization Name and Address

Department of the Air Force
HQ USAF (AFTAC/TAP)
Patrick A.F.B., Florida 32925

13. Type of Report & Period Covered: Instruction Manual

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This manual contains an overview of the U system, which uses a small computer to provide automatic control of up to 15 special-purpose radio receivers. The diagrams show the overall system configuration, cabling, data flow and computer word bit assignments.

17. KEY WORDS (Alphabetical order, separated by semicolons)

ADACS; computer-controlled receivers; U system

18. AVAILABILITY STATEMENT

[ ] UNLIMITED.

[X] FOR OFFICIAL DISTRIBUTION. DO NOT RELEASE TO NTIS.

19. SECURITY CLASS (THIS REPORT): UNCLASSIFIED

21. NO. OF PAGES

20. SECURITY CLASS (THIS PAGE): UNCLASSIFIED

22. Price

USCOMM-DC [illegible]