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Field Service Test Model: Computer-Controlled U System Manual for Computer Subsystem

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Instruction Manual

Prepared for
Department of the Air Force
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NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, Director

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by
R. J. Carpenter, K. M. Gray
D. S. Grubb and L. J. Palombo

1. INTRODUCTION

The computer subsystem monitors the status of the receiver and its output signal; performs the necessary programmed calculations on the status and signal; manipulates the receiver's controls for proper operation of the receiver; and records the phase of the output signal. The overall system is shown in figure 1 and the computer subsystem is shown in figure 2.

The computer subsystem includes a minicomputer with a 16-bit word size, 32K words of core memory, and processing power adequate for the control of up to 15 receivers. It also includes input/output logic for the use of several computer peripheral devices and for input/output data for the receivers. The peripheral devices include two teletypewriters, a high-speed paper tape reader, and a magnetic tape unit. Interface logic is provided for a high-speed paper tape punch.

Each receiver provides three analog inputs to the receiver: Phase Difference, Amplitude, and Blanking Percentage. The first two are from the receiver and the latter from the ADACS Interface

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Certain commercial equipment and materials are identified in this paper in order to adequately specify the components used. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Chassis. Each input is filtered to remove high frequency noise. The inputs are then multiplexed and the multiplexer output used with a sample and hold circuit as the input to a 12-bit analog-to-digital converter. The digital outputs of the converter are input data for the computer. The 15 receivers use 45 of the available 48 input channels.

Each receiver provides, via its ADACS unit, a 16-bit word of digital data to the computer. The real-time clock provides 2 words of time information and a wired connector plug is used to provide 1 word of information for the unit/detachment number. These words are multiplexed to provide a stream of 16-bit words to the computer. The 15 receivers (if that many are used), the 2 real-time clock words and the unit/detachment word use 18 of the 22 available digital input channels.

The computer program generates a 16-bit digital output word to send to each of the receivers via its ADACS unit. The 15 receivers use 15 of the available 16 digital output channels.

Interrupts from the receiver's ADACS units are "daisy-chained" to provide a single computer interrupt. The real-time clock provides one interrupt for seconds and another for minutes. The least significant bit from each cardioid unit is used with the Common Alarm circuit of the computer subsystem to generate an interrupt when the status of one of the cardioid units changes. These interrupts use 4 of the available 8 interrupts for the computer subsystem.

2. CONFIGURATION

The computer subsystem requirements were specified, and the MODCOMP III computer was selected. In the following descriptions of the system the MODCOMP model number is given for each of the features and attachments (see figure 2).

2.1 CENTRAL PROCESSING UNIT (CPU)

The CPU, a MODCOMP III, is a general-purpose, 16-bit digital computer mounted in a 19-inch wide rack enclosure with the necessary power supplies for use on 117 volt a.c. The CPU contains an arithmetic unit, a read-only memory for the instruction controls, a 32K word core memory, 15 general registers, 8 priority interrupt levels, an operator's console, and a built-in controller for a teletype unit and a high speed paper tape reader.

Logic was added to provide hardware multiply and divide (model number 3503). The core memory uses 4 sections of 8K words (model number 3608) for a total of 32K words, with byte parity (model number 3606) for the detection of memory errors. A power-fail-safe and automatic start feature (model number 3739) feature was added to protect against power failures. "Direct Memory Processor" for automatic block transfers (model number 3704) was provided.

2.2 PERIPHERAL DEVICES

Several peripheral devices are attached to the computer for operator use. An ASR-35 console Teletypewriter (model number 4235) is attached using the computer's built-in control logic. The ASR-35 contains a keyboard, a page printer, a paper tape reader, and a paper tape punch. The printer, reader and punch are relatively

slow devices. All of the devices use USASCII code.

An ASR-28 console typewriter is also attached to the computer. It is similiar to the ASR-35 in its general features, but uses 5-bit Baudot code. It is attached to the computer by an asynchronous communications interface (model number 4810).

A high-speed paper tape reader (model number 4511) capable of 625 characters per second is attached to the computer using the computer's built-in controller.

A magnetic tape unit (model number 5149) for 7 track, 25 inches per second, 556/800 bit-per-inch magnetic tape using 10.5-inch reels is attached to the computer using the peripheral controller interface (model number 4901). The latter is designed to permit the attachment of a high-speed paper tape punch and up to two other input/output controllers.

2.3 RECEIVER INTERFACING

The analog and digital data to and from the receivers is interfaced with the computer via the Connector Panel and the I/O interface subsystems. The Connector Panel provides a common point for the connection of the cables from the various receivers and the real-time clock. Card plugging for the interface subsystems is shown in figure 3.

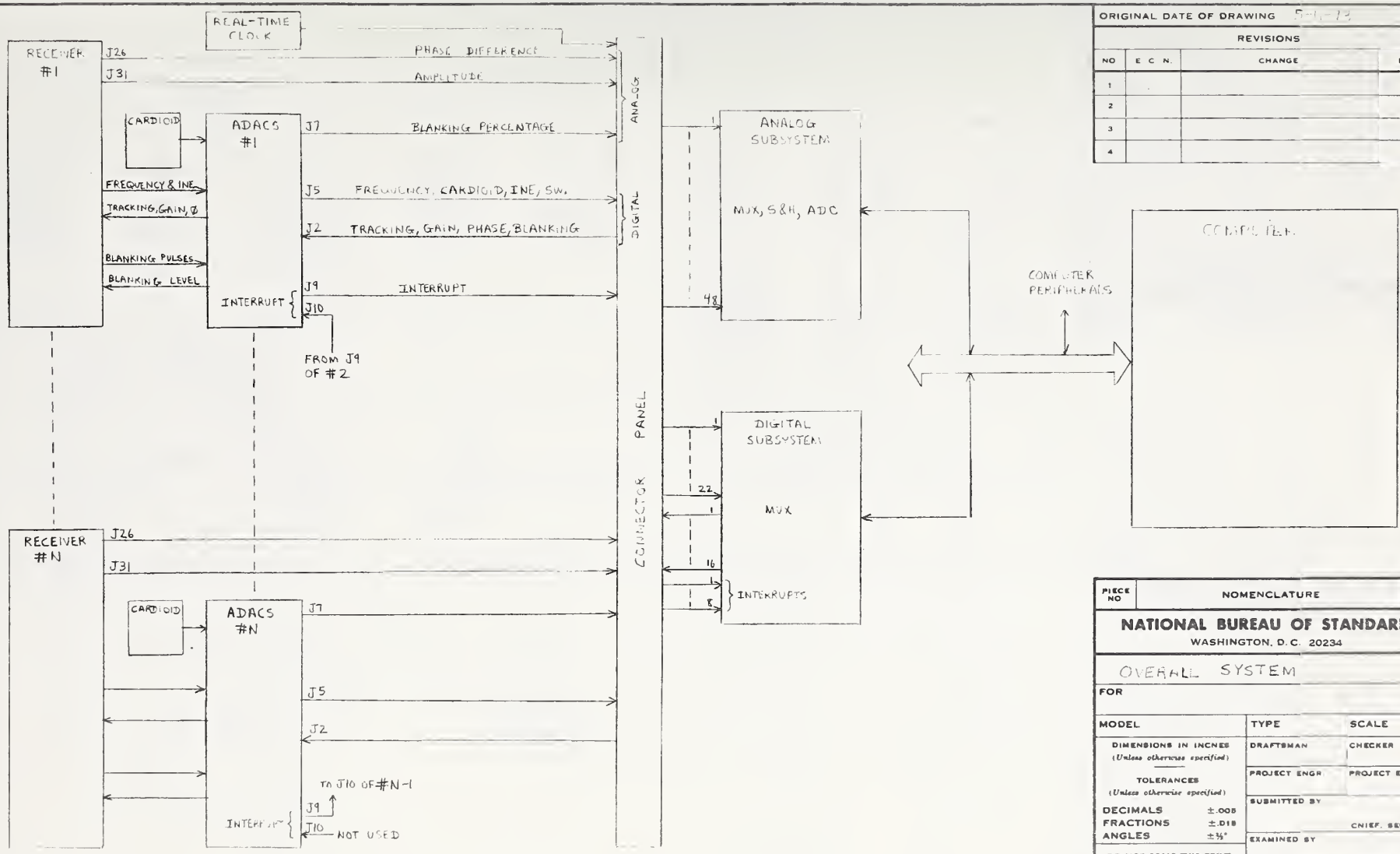
The three analog input lines for each receiver are filtered to remove high frequency noise and harmonics of the 60 hertz power. Each filter unit (model number 1224) contains filters for 16 lines and uses a cutoff frequency of 148 hertz. The analog lines are multiplexed on the multiplexer gate cards (model number 1210). The

output from the multiplexing is used with a sample and hold circuit as the input to the analog-to-digital converter. The output of the analog-to-digital converter is a 12-bit digital for the computer. For more details on the 1200 interface subsystem, see the manufacturer's technical manual on the Analog Input Subsystem 1200.

The 16 digital bits from each receiver's ADACS unit to the computer enter the interface subsystem logic via the Connector Panel. From there the bits are sent to a digital input channel card (model number 1124 in the 1100 chassis), which provides the signal conditioning. The 16 digital bits and flag pulse to each receiver's ADACS unit from the computer leave via the digital output channel card (model number 1131 in the other 1100 chassis), which drives the lines through the Connector Panel to the ADACS units. The flag pulses are generated by 1101 cards that have been modified to produce 10 microsecond pulses. Only one interrupt line is received from the ADACS units, as the interrupts are "daisy-chained". This interrupt enters via the Connector Panel to an I/O Interrupt Coupler card (model number 1161). For more details, see the manufacturer's technical manual on the I/O Interface Subsystem 1100.

3. REFERENCES

The manuals for the various units of the computer subsystem contain detailed descriptions and diagrams. Programs supplied with the computer are also described in the manuals on programming.



OVERALL SYSTEM

FIGURE 1

ORIGINAL DATE OF DRAWING 5-1-73

REVISIONS

NO	E C N.	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO. REQ'D

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WASHINGTON, D. C. 20234

OVERALL SYSTEM

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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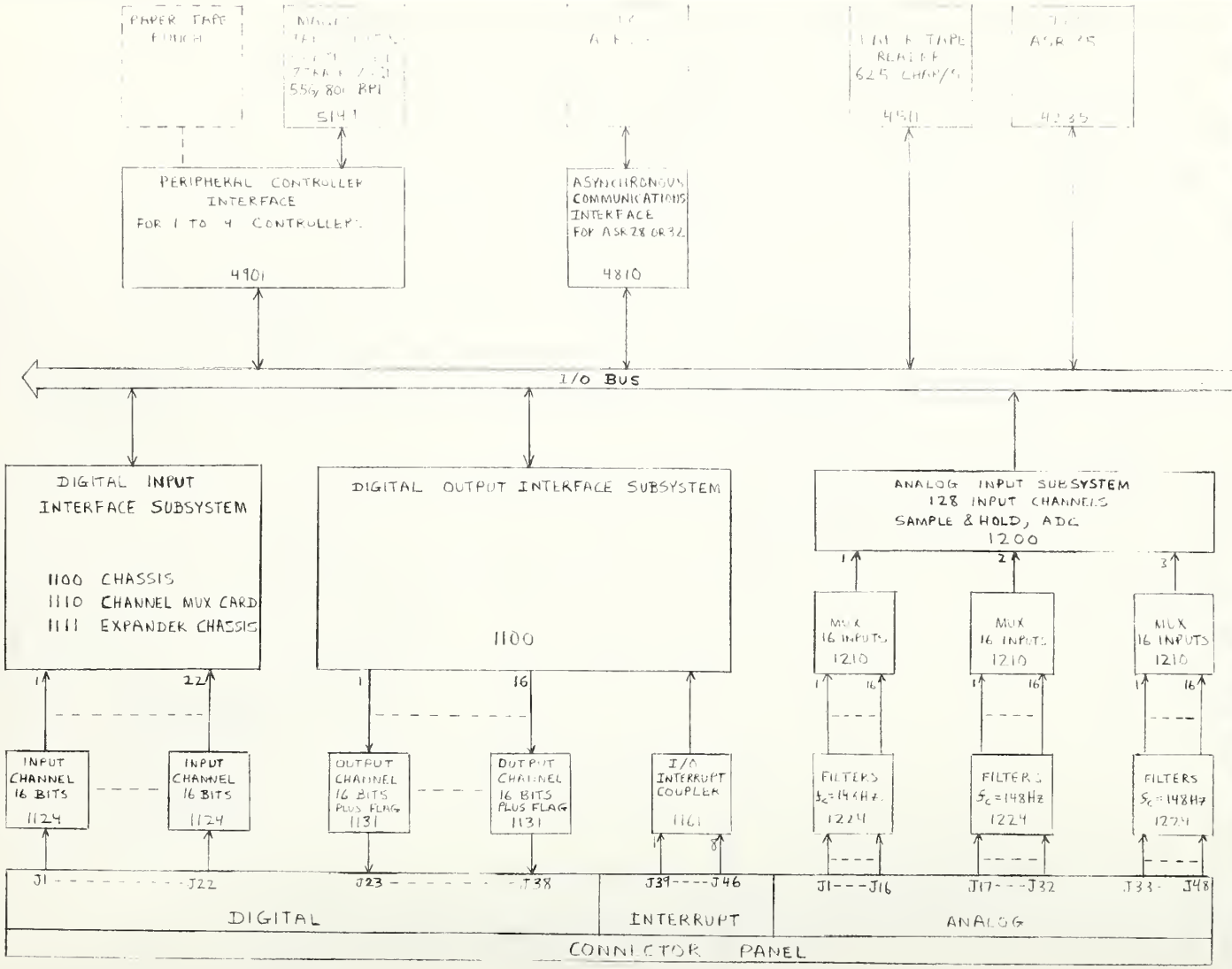

COMPUTER SUBSYSTEM
FIGURE 2

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

MULTICOMP III
COMPUTER

32 K 16 BIT WORDS CORE MEMORY, 800 NANOSECOND, BITE PARITY 4-3602 & 3616
POWER FAIL SAFE & AUTO START 3734

DIRECT MEMORY PROCESSOR, BLOCK TRANSFERS TO/FROM 16 PERIPHERAL DEVICES CONCURRENTLY, 300K WORDS/S. 3704
MULTIPLY/DIVIDE HARDWARE - 3503

PIECE NO.	NOMENCLATURE	NO. REQ'D

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WASHINGTON, D.C. 20234

COMPUTER SUBSYSTEM
FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
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ORIGINAL DATE OF DRAWING

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

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WASHINGTON, D.C. 20234

1100/1200 CONFIGURATION

FOR

MODEL | TYPE | SCALE

DIMENSIONS IN INCHES (Unless otherwise specified)

TOLERANCES (Unless otherwise specified)

DECIMALS ±.005
FRACTIONS ±.016
ANGLES ±4°

	DRAFTSMAN	CHECKER
	PROJECT ENGR	PROJECT ENGR
SUBMITTED BY		CHIEF SEC
EXAMINED BY		CHIEF ENGINEER
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1200

1111 EXPANDER

1106

1100

1131 DIGITAL OUTPUT TTL

1124 DIGITAL INPUT CONTACT SENSE

1124 DIGITAL INPUT CONTACT SENSE

1124 DIGITAL INPUT CONTACT SENSE

1191 DIGITAL INPUT COMMON ALARM

1124 DIGITAL INPUT CONTACT SENSE

1110 CHANNEL MUX

1124 DIGITAL INPUT CONTACT SENSE

1131 DIGITAL OUTPUT TTL

1110 I/O INTERRUPT CLOCK

1101 * SYNC CARD CH. 8-15

1101 * SYNC CARD CH. 0-7

LOGIC CONTROL CARD #2

LOGIC CONTROL CARD #1

LOGIC CONTROL CARD #2

LOGIC CONTROL CARD #1

LOGIC CONTROL CARD #2

LOGIC CONTROL CARD #1

A-TO-D CONVERTER

SPARE

SPARE

TEST MUX #1

HIGH LEVEL MUX #2

SUBSYSTEM CONTROL LOGIC

DRIVER/ DECODER

ANALOG

DIGITAL

* OUTPUT PULSE (FLAG) MODIFIED FOR 10. MICROSECOND WIDTH.

I/O INTERFACE SYSTEM

FIGURE 3

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This manual contains a description of the computer subsystem used to control the operation of the receivers in the U System. The diagrams show the connection of the computer subsystem to the other units in the system, the arrangement of the components within the computer subsystem, and the card locations in the I/O interface portion of the computer subsystem.

17. KEY WORDS (Alphabetical order, separated by semicolons)

ADACS; computer-controlled receivers; U system

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