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Field Service Test Model: Computer-Controlled U System Manual for Receiver and ADACS Interface Chassis

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U. S. DEPARTMENT OF COMMERCE, Frederick B. Dent, Secretary

NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, Director

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FIELD SERVICE TEST MODEL: COMPUTER-CONTROLLED U SYSTEM MANUAL FOR RECEIVER AND ADACS INTERFACE CHASSIS

by

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1. INTRODUCTION

The Field Service Test Model uses a computer to control the operation of from 1 to 15 EECO 881 receivers for unattended operation. Each receiver is connected to the computer by an ADACS Interface Chassis, which provides the necessary decoding and conversion for communication between the receiver and the computer (see figure 1).

This manual describes the overall operation of the system, modifications needed for the receivers, and construction of the ADACS Interface Chassis. All necessary drawings and parts lists are included. The operation of the receivers is described only to the extent of the modifications for computer control, as it is assumed that the reader is thoroughly familiar with the operation of the receivers.

2. GENERAL DESCRIPTION

The receiver functions that must be computer-controlled for unattended operation are RF gain, uncorrected phase, tracking rate and blanking level. See figure 1. The computer controls the RF gain by monitoring the AGC level of the receiver and sending the appropriate gain level value back to the receiver. The computer monitors the difference between the corrected and uncorrected phase signals of the receiver. The computer uses the difference to determine when to order a phase shift of the uncorrected phase signal and to determine the desired tracking rate of the receiver. The computer monitors the blanking pulses output of the receiver to determine the blanking level to be used by the receiver. The computer also monitors the operational status of the receiver and the position of the Channel Select (frequency) switches. If the operational status of any receiver changes, the change causes an interrupt to the computer, which then determines which receiver has changed status.

A receiver may be changed to manual operation by use of the Manual/ Automatic switch on its ADACS (Automatic Data Acquisition Control System) Interface Chassis. (In manual status a receiver is controlled by an operator.)

When maintenance is being performed on a receiver, the Maintenance switch on its ADACS unit should be on to inform the computer that the receiver is being serviced.

The cardioid unit for the receiver is interfaced to the computer through the ADACS unit, so that the computer may monitor the status of the cardioid unit.

The receiver modules affected by the use of computer control are the Local Oscillator and Servo Module and the RF-IF Amplifier Module. Receiver cards D582-AB (only the one in socket B7), D586-AB and D592-AA are modified. Three new cards are added to the receiver: S1001 and S2001 in the Local Oscillator and Servo Module, and S3001 in the RF-IF Amplifier Module. Wiring changes have been made to both modules.

The ADACS Interface Chassis is a 19-inch wide rack-mounted chassis containing the necessary signal decoding and conversion circuits to interface the receiver to the computer. There is one ADACS unit per receiver. Each ADACS unit contains two circuit cards (both custom), two power supplies and miscellaneous switches, indicator lamps and connectors. The bare chassis is shown on figure 41 prior to completion. The front and rear panels of the unit are shown on figures 42 and 43. A top view of the unit with the cards installed is on figure 46. The schematics for the ADACS unit are on figures 26 through 29, which are labelled internally as sheets 1 through 4, respectively, for convenient designation of interconnections.

3. COMPUTER CONTROL OF RECEIVER

3.1 RF GAIN

The system diagram, figure 1, shows the AGC level (Amplitude) of the receiver being sent directly to the computer. The computer program uses the AGC level to determine the RF Gain setting to be used by the receiver. The computer sends 5 bits defining the gain level to be used to the ADACS Interface Chassis, where the 5 bits are decoded and signals sent to the receiver to operate relays on the Gain Control card, S3001. These relays connect the proper resistors into the receiver's RF gain circuit.

The AGC level is taken from pin E of card A3 in the Receiver Section and is shown on figure 7. This signal is connected to pin 18 of J40 (figure 9) as an input to card S1001. On card S1001 (figure 14) two operational amplifiers, AR2 and AR4, amplify the signal for driving the cable to the computer and filter off some higher frequency noise. R28 is used to compensate for non-zero "zero" output from the receiver and R31 is provided to set full-scale. The output is connected to pin 10 of S1001. The connection from the card to the back of the receiver is shown on figure 6, and from the receiver to the computer on figure 2.

The computer generated Gain bits are sent to the Gain-Tracking-Phase card in the ADACS Interface Chassis. This is shown on figure 27. The decoder circuitry on the Gain-Tracking-Phase card is shown on figure 31. This circuitry decodes the 5 bits and drives lines to operate the proper relays in the receiver. (The chart showing which relays are operated and the resulting gain level in the receiver is on figure 30.) The lines to the receiver are shown on figure 27 as they leave the ADACS unit. The gain relay lines are shown entering the receiver on figure 5, where they go to the Gain Control card, S3001, shown on figure 16.

Gain control in the receiver is accomplished by variation of the negative feedback resistor in an amplifier consisting of Q6 and Q7 on the Receiver Amplifier card, ZA35279. As the resistor is made smaller, the gain is decreased. In fact, the gain is almost linearly proportional to the value of the resistor. For the lowest gain value, a short circuit using K1 is used in place of the feedback resistor, so that only the internal 2.2 ohm resistor, R17, of ZA35279 is in the circuit. An attempt has been made to obtain 3 dB gain steps, thus the feedback resistance for each step should be 1.4 times that of the previous step. In order to reduce the number of relays and resistors required, the steps are approximated by a scheme where R1 and R2 are in parallel, then R1 alone, then R2 and R3 in parallel, then R2 alone, etc. In this manner the 6 dB steps are essentially correct and the intermediate steps are approximately correct. Examination of the circuit shown on figure 16 will show that relays K1 through K14 are used to control the gain. The next to highest

gain value is obtained with K13 and K14 closed and the next highest value with only K13 closed. (K14 is never used alone.)

The S3001 card also contains a relay, K15, which is used to control whether the relay-controlled resistors on S3001 will be used for automatic (computer-controlled operation) or whether the RF Gain control on the front panel of the receiver for manual control will be used instead.

3.2 PHASE

The phase difference between the corrected and uncorrected phase is shown on figure 1 going directly from the receiver to the computer. The computer program uses the phase difference to determine the need for changing the phase of the uncorrected phase. When a phase change is needed, the computer has the ADACS Interface Chassis send a 10-microsecond pulse to the receiver. In the receiver there is circuitry (added for computer control) that causes the uncorrected phase signal to be shifted by 50 microseconds.

The phase difference signal is taken from pin M of card A1 in the Servo Section and is shown on figure 8. (Part of the Servo Section circuitry is shown on the diagram for the Reference Divider Section.) The phase difference signal enters the S1001 card on pin 17, as shown on figure 14. On card S1001 two operational amplifiers, AR1 and AR3, amplify the signal for driving the cable to the computer and filter off some of the higher frequency noise. R38 is used to compensate for non-zero "zero" output from the receiver and R41 is provided to set full-scale. The output is connected to pin 9 of S1001. The connection from the card to the back of the receiver is shown on figure 6, and from the receiver to the computer on figure 2.

The computer-generated phase-change-signal and 10-microsecond pulse are sent to the Gain-Tracking-Phase card in the ADACS Interface Chassis as shown on figure 27. The card circuitry gates a single 10 microsecond pulse to the receiver when commanded to do so by the computer. See figure 32. The phase change pulse is shown on figure 27 going to the receiver and on figure 6 entering the receiver, where it goes to pin 17 of the S1001 card. On the S1001 card (figure 14) the phase change pulse is used to control the phase shift circuit.

The phase shift circuit reverses the phase of the uncorrected phase signal. This signal has a frequency of 10 kilohertz, so a 50-microsecond shift will effectively reverse its phase. This is done in the modified receiver by breaking the connection between the third and fourth stages of the divide by ten counter in card location B7. This is shown on figures 8 and 12. The output of the third stage (20 kilohertz) of the counter is sent to the S1001 card where it is normally gated right back to the fourth stage. When the shift is performed, the pulse from the ADACS unit is used to set the left flip-flop of U2 on card S1001. The next positive-going transition

of the 20 kilohertz signal will transfer the set state to the right-hand section of U2. The set (high) output of the right-hand section of U2 is applied to the other gate input of U1 through which the 20 kilohertz signal passes back to the receiver, disabling the 20 kilohertz signal path. The output of the right-hand section of U2 is also applied to the dc reset input of the left-hand section of U2, resetting this section immediately. The right-hand section of U2 will then resume the clear (low) state on the next positive-going transition of the 20 kilohertz signal. The result is that the right-hand section of U2 is set for exactly one whole 20 kilohertz cycle, and disables the 20 kilohertz path through U1 back to the receiver for exactly 50 microseconds.

3.3 TRACKING

The phase difference is also used by the computer program to determine the tracking rate for the receiver. The computer sends 4 bits defining the tracking rate to the ADACS unit, where the 4 bits are decoded and signals sent to the receiver to operate relays on the Tracking Rate card, S2001. These relays connect the proper amount of resistance and capacitance into the two integrators in the receiver. The resistors are mounted on the S2001 card, while the capacitors are those already mounted in the receiver.

The phase difference is sent to the computer as described in 3.2. The computer-generated Tracking bits are sent to the Gain-Tracking-Phase card in the ADACS unit. This is shown on figure 27. The decoder circuitry on the Gain-Tracking-Phase card is shown on figure 32. This circuitry decodes the 4 bits and drives lines to operate the proper relays on card S2001 in the receiver. (The chart showing which relays are operated and the resulting tracking rate is on figure 30.) The lines to the receiver are shown on figure 27 as they leave the ADACS unit. The tracking relay lines are shown entering the receiver on figure 6, where they go to the Tracking Rate card, S2001, shown on figure 15. The S2001 card uses relays K1 through K5 and K12 through K15 to select the proper resistors, while relays K6 and K16 are used to connect the capacitors. The S2001 card is connected to the receiver circuitry as shown on figure 10.

Switching between manual operation and automatic (computer-controlled) operation is performed by relays K7, K8, K9, and K10 on card S2001. In automatic operation, the Servo switch on the front of the receiver is disabled by relays K8 and K9, and the receiver made to operate as if the Servo switch were in the "TRACK" position. Relays K7 and K10 are used to transfer control from the Tracking Rate switch on the front panel of the receiver to control by the S2001 card. In manual operation, the front panel switches control the receiver.

3.4 BLANKING

The receiver has, as an output signal, an on-off voltage which indicates when the input signal is being blanked (signal gain reduced to zero). This signal is sent to the ADACS unit where an analog circuit converts the on-off pulses into an analog voltage that is proportional to the percent of the time that the receiver is blanked. This analog voltage is sent to the computer. The computer program uses this signal to determine the proper blanking level for the receiver. The computer sends 6 bits to the ADACS unit defining the proper blanking level voltage. The ADACS unit uses a digital-to-analog converter and a non-linear network to produce the blanking level voltage for the receiver. This voltage is sent to the receiver, where it is used by the receiver if it is in automatic operation.

The routing of the blanking signals is shown on figure 1 and the cabling for the blanking signals is shown on figure 2. The blanking pulses output from the receiver is shown on the bottom of figure 4, the RF-IF Amplifier Module schematic. The signal is routed as shown at the top of figure 5, the RF-IF Amplifier Module cable diagram. The blanking pulses signal enters the ADACS unit as shown at the top of figure 28, where it goes to the Blanking Level card, S4001, which is on figure 33.

The blanking pulses signal is at zero volts when the receiver is blanked and at minus 11 volts when operation is normal. A saturated DTL inverter using Q1 and associated components produces pulses at the collector of Q1 of the same period as those at the input, but of known -15 volt amplitude. These pulses are then averaged in the active low-pass filter consisting of AR2, filter capacitor C2, feedback resistor R18 and R18A, and input resistor R14 and R16 in series. Variation of R18A allows a small control of full-scale output (volts per percent blanked). A capacitor C8 from the junction of R14 and R16 to ground removes the components of the square wave that are beyond the limits of the amplifier in the active filter. A small offset is caused by R17 to result in zero output voltage with the input (pin X) open. (This is compensation for the finite saturation voltage of Q1.) A value of about 22 megohms will compensate for the 150 millivolts to be expected. If the small offset can be tolerated, this resistor may be left out. With input pin X connected to ground, set R18A for the desired 100 percent blanking output voltage, 10 volts.

The percent blanking signal leaves the ADACS unit as shown on figure 28. The computer program uses it to determine the proper blanking level and sends 6 bits defining this level back to the ADACS unit. The bits enter the ADACS unit as shown on figure 28 and go to the Blanking Level card, S4001, as shown on figure 33. The 6 bits are converted to an analog voltage with a non-linear relationship. The bits are applied to the digital-to-analog converter, which produces a zero to +10 volt output according to the bits. This

analog voltage is then modified by passing through the non-linear amplifier stage consisting of AR1, C1, CR1, CR2, CR3, and R1 through R10. The result is an output in the zero to -10 volt range at output pin V. The non-linear conversion takes place in the input "resistors" of the operational inverter stage containing AR1. This "resistor" actually is composed of four different circuits, which progressively come into action as the output of U6 increases. For small values of output of U6, the input "resistor" is, in fact, R7. As the voltage increases, CR3 becomes forward biased and the input "resistor" involves R5, R6, R7 and CR3. The result is a lower equivalent input "resistance" with a higher resulting gain for the inverter. Further increase in the output of U6 will bring in the circuit containing CR1, and finally that including CR2. The result is an increase in gain of the inverter as the output of U6 increases. The change in gain is about 2-to-1 at each knee. Thus, much finer adjustments in the blanking voltage are possible as it becomes nearer to zero.

The blanking level output from the S4001 card leaves the ADACS unit as shown on figure 28, and enters the receiver as shown on figure 5. In the receiver it goes to the S3001 card, as shown on figure 16. On the S3001 card it is connected to the receiver blanking level input if relay K15 is in the automatic (computer-controlled) position. (Otherwise, the Blanking level control on the front panel of the receiver supplies the blanking level.) The blanking level selected by relay K15 leaves the S3001 card on pin C and is connected to the blanking level circuit of the receiver as shown on figure 4.

3.5 FREQUENCY

The computer program monitors the frequency of the receiver as indicated by the setting of the Channel Select switches on the front panel of the receiver.

The settings of the Channel Select switches are detected as shown on figure 9. The outputs go to card S1001 shown on figure 13, where the switch settings are latched in integrated circuits U3 and U4. The signal for setting the latches is a negative-going 2 microsecond pulse from the logic shown on figure 9. This pulse occurs at a 100 hertz rate. On card S1001 it is inverted by one section of U1 into a positive-going pulse. Two more sections of U1 are used as a one-shot multivibrator to produce a 1 microsecond pulse to load the switch-position signals into the latches (U3 and U4) during the receiver switch sensing pulse.

Since all of the digital integrated circuits on this card operate below ground (their normal +6 volt supply terminal is grounded),level changers must be used to get to positive TTL levels to connect to the computer. This is accomplished in FET's Q4 through Q13. These FETs must conduct 5 milliamperes with less than 0.4 volt drop when they a are zero biased; and less than 10 microamperes when they have -6 volts bias. Since some 2N4092 FETs will not meet these requirements,it is necessary to select them for use in this circuit.

The frequency bit outputs leave the receiver as shown on figure 6, and are passed through the ADACS unit as shown on figure 29 to the computer.

3.6 INE AND INTERRUPT

INE (Invalid Data Equipment sensed) is used by the computer program to indicate that the receiver is inoperative. Several conditions are monitored by circuitry in the receiver and if any of them indicates that the receiver is inoperative, the INE signal is sent to the ADACS unit. If the ADACS unit receives an INE signal from the receiver or detects such a condition in the ADACS unit, it sends an INE indication to the computer. The ADACS unit will also send an interrupt signal to the computer if there is a change in the INE status or in the status of either of the switches on the ADACS front panel, MAINTENANCE and MANUAL. The interrupts from all of the ADACS units are "daisy-chained" so that only one interrupt is needed to the computer.

The INE circuitry in the receiver is on the S1001 card shown on figure 13. As long as current flows out of pin 15 (P2/J41) into the base of NPN transistor on card S4001 in the ADACS unit, the receiver is presumed to be in operating condition. This current comes from the +12 volt supply through R1. If the +12 volt supply falls appreciably, the current to the -12 volt supply will divert the output current and indicate INE. The same situation will occur if the -12 volt supply voltage rises substantially. The opposite conditions of +12 volts too high or -12 volts too low will cause Q3 to conduct, diverting the output current and causing INE.

If the receiver senses that the frequency synthesizer is not operating properly, the receiver TUNING lamp will be energized and the voltage applied to input pin 12 of the S1001 card will change from -18 volts to zero volt . (See figure 9.) Thus FET Q1 will conduct strongly, diverting the current from the output and INE will be sensed.

In manual operation if either the RF signal level drops too low for the servo to operate or the Servo switch is moved from the TRACK position, an INE signal is generated. See figure 10. The indication of the RF signal being too low enters the S2001 card (figure 15) on pin 11 and the status of the Servo switch enters on pin 3. The INE output is on pin 4 and goes to pin 16 of the S1001, where it causes Q2 to saturate, diverting current from the output and causing INE to be sensed.

The INE output from the S1001 card leaves the receiver, as shown on figure 6. The INE from the receiver enters the ADACS unit as shown on figure 28. The INE circuitry on the S4001 card is shown on figure 34.

Normally, a current of about 300 microamperes is supplied to input pin 5 by the INE line from the receiver, indicating the absence of any INE conditions. This keeps Q2 saturated and the INE voltage to the computer (output pin E) low. If this current fails or is diverted from the base of Q2 (due to a receiver INE), then Q2 becomes an open circuit. The voltage at pin E will then rise due to R27 and CR11 or the current supplied into pin E from the computer interface. If the +5 volt supply for Q2 is not present, CR11 prevents the internal circuit from loading pin E and the computer will still read Q2 as an open circuit. When the +5 volt supply fails, the -15 volt supply pulls down the base drive to Q2 through CR7, turning Q2 off. CR9 prevents the base voltage of Q2 from going too negative for safety. In like manner, failure of the +15 volt supply will cause the base drive to Q2 to be diverted through CR8, turning Q2 off. If the -15 volt supply fails, neither of the above systems will work, but the FET Q3 will have zero gate bias and will then have low drain-source resistance diverting the base drive from Q2, causing an INE indication. The INE system will also indicate an INE when the MAINTENANCE switch on the front panel of the ADACS unit is in the MAINTENANCE position. This action opens the circuit from input pin A to ground, resulting in one section of U2 diverting the base current from Q2.

The INE output from the S4001 card leaves the ADACS unit and is sent to the computer as shown on figure 28 and on the system cable diagram, figure 2.

In addition to generating INE for the computer, the INE system also has provisions for generating an interrupt to the computer when there is any change in the INE, MAINTENANCE or MANUAL conditions. The state of these three digital variables are continuously being compared in U4 on the S4001 card (figure 34) with a set of conditions previously stored in latch U3. If they differ, the A=B output of U4 will change from high to low, triggering the one-shot multivibrator, U5. The one microsecond output pulse from U5 is used to transfer the new information into latch U3, so that the A and B inputs to U4 will again be the same and the A=B output will rise. The output pulse of U5 is also amplified in a section of the power inverter U2 and is used to cause a computer interrupt by pulling the "daisy-chained" line connected to output pin 4 to ground. The line is shown going to the ADACS unit output on figure 28 (bottom of the page) and on the system cable diagram, figure 2. Back on S4001, a free-running pulse generator consisting of Q4 and Q5 and their associated components is used to retrigger the one-shot, U5, in the case that the contents of latch U3 do not equal the present state of the variables, yet U5 has already generated its one pulse per trigger. The circuit would hang-up if a retrigger means were not provided.

3.7 MANUAL/AUTOMATIC SWITCH

The MANUAL/AUTOMATIC switch on the front panel of the ADACS unit is used to switch the associated receiver from automatic operation (computer-controlled) to manual operation (operator-controlled). The switch is shown on figure 26, where it is used both to light the MANUAL lamp and to supply lines from the switch to other parts of the ADACS unit. The line labelled Manual is sent via the wiring shown on figure 29 to the computer. The line labelled Automatic is sent both to card S4001 (figures 28 and 34) for use by the INE circuitry in generating computer interrupts and to the wiring shown on figure 27 to be sent as the line labelled Automatic to the receiver. (See also the system cable diagram, figure 2, for system usage of the Manual and Automatic lines.)

The Automatic line to the receiver is shown entering the receiver on figure 6 (to the Local Oscillator and Servo Module) and on figure 5 (to the RF-IF Amplifier Module). In the former, Automatic goes to pin 16 of the S2001 card (figure 15); in the latter, Automatic goes to pin H of the S3001 card (figure 16). In both cases, it is used to operate Manual/Automatic relays.

3.8 MAINTENANCE/NORMAL SWITCH

The MAINTENANCE/NORMAL switch on the front panel of the ADACS unit is used to inform the computer program that the associated receiver is being serviced. The switch is shown on figure 26, where it is used both to light the MAINTENANCE lamp and to supply lines from the switch to other parts of the ADACS unit. The line labelled Maintenance is sent via the wiring shown on figure 29 to the computer. The line labelled Normal is sent: a) to card S4001 (figures 28 and 34) for use by the INE circuitry both to generate INE and a computer interrupt; and b) to the wiring shown on figure 27 where it goes to pin Z on J1, which is a dead-end, as this signal is not used by the receiver.

4. RECEIVER MODIFICATIONS

4.1 MECHANICAL

Mechanical modifications to the receiver are needed to install the S3001 card and to add three connectors to the rear panel. Cards S1001 and S2001 do not require mechanical modifications to the chassis, as they slide into spare card guide slots and use cable plugs to connect to the receiver wiring.

4.1.1 S3001 CARD

Two each of two types of custom-made brackets are required to hold the S3001 card in the RF-IF Amplifier Module. These brackets and the holes to be drilled in the frame of the module are shown on figure 17. The card is installed using the brackets, as shown on figure 18. The card pins should be nearest the front panel of the module, and the card components should be facing the open side of the chassis.

4.1.2 REAR PANEL CONNECTORS

Three new connectors, J30, J31 and J32, must be added to the rear panel of the main chassis of the receiver. The drilling and cutting needed are shown on figure 19.

4.2 MAIN CHASSIS

Wiring must be added to the main chassis of the receiver to connect the modules within the receiver to the connectors to the ADACS Interface Chassis and to the computer. The general layout of the added wiring is shown on figure 2. The detailed wiring from the back of the receiver to the RF-IF Amplifier Module is shown on figure 5 and from the back of the receiver to the Local Oscillator and Servo Module on figure 6. Where possible the added wiring is cabled. Color coding is used to assist in servicing.

A plastic sleeve of 1/2 inch length of PVC plastic tubing, Alpha Wire #13 (PVC-105/13) MIL-1-631D/F/U should be slipped over each wire (or pair of wires) to be attached to J15, J19, J20, J21 and the wire to the center terminal of J22, J26, J27 and J31.

1) Cut 10" lengths of #22 Teflon insulated stranded wire of the following colors -

2 ea black	1 ea yellow
1 ea brown	1 ea green
1 ea orange	1 ea blue
1 ea gray	1 ea purple
2 ea red	1 ea white

2) Crimp a connector contact (ELCO #000-60 8017 06 13) on one end of each of the above wires.

3) Following the wiring shown on figure 6, solder one end of each of these wires to the correct terminal of J19 (use plastic sleeve) and insert the other end of each wire in the correct position in J30. Do this one wire at a time to avoid confusion between the like-colored wires.

4) Use Tie-Wraps to form a cable from the above wires.

5) Cut two 13" lengths of RG-174/U cable. Connect the center conductor of one from J19-2 to the center of J26. Use plastic sleeves. Connect the center conductor of the other from J19-9 to the center of J31. Use plastic sleeves. Connect one end of both shields to J19-1. Connect the other end of both shields to the ground lug between J25 and J26. (See figure 6).

6) Cut the following 7" pieces of #22 Teflon insulated stranded wires -

2 ea black	2 ea green
3 ea brown	3 ea blue
1 ea red	4 ea purple
1 ea orange	3 ea gray
2 ea yellow	1 ea white

7) Crimp a connector contact (ELCO #000-60 8017 06 13) on one end of each of these wires.

8) Connect a 9" piece of #22 red wire from the center of J23 to J15-8, before soldering the J15 end, also insert the 7" red wire cut above into J15-8 - use a common plastic sleeve over both wires. Now solder them both to J15-8. Insert the free end with the connector terminal into J32-b. (See figure 6.)

9) Connect one of the black 7" wires to the outer terminal of J23 and push its connector end into J32-c. (See figure 5.)

10) Cut an 8" piece of #22 gray wire and connect one end to J21-16. Slip the other end of this piece and one of the 7" gray wires through the same plastic sleeve and solder them both to J20-16. Insert the free connector end into J32-a. (See figures 5 and 6.)

11) Following the Wire List, connect the remaining 7" wires to J20 or J21 and the appropriate location of J32. (See figures 5 and 6.)

12) 12" Green #22 wire from J19-3 to J32Y. (See figure 6.)

13) 13" Coax RG-174/U from J22 to J27 with sleeves. Connect shield to outer terminal on both ends. (See figure 5.)

14) Dress all of the above wires against existing wires and hold them in place with Tie-Wraps.

4.3 RF-IF AMPLIFIER MODULE

This module is modified by the addition of the S3001 card and the added wires to the module's connectors to the main chassis of the receiver. The finished wiring is shown on Figure 4. (The original wiring is shown in the receiver manual.)

A number of wires will be connected to J21A. Slip 1/2 inch of clear plastic tubing, Alpha PVC-105/13, over the wire before soldering and then slip it down over the terminal after the solder has cooled. Unless noted, all wire is #26AWG Teflon insulated.

1) Unsolder the green lead from the tap on the Blanking pot (R2) and connect this wire to J21A-C.

2) Disconnect the shielded cable from the Gain pot (R1) and connect the center conductor to J21A-4 (do not use plastic sleeve).

3) Connect a 4" orange wire to the CW and center terminal of R1 and run it to J21A-5. Also connect the shield of the coax cable (above) to J21A-5 (use no plastic sleeve).

4) Connect a 4" gray wire from the tap on R2 to J21A-B.

5) Connect a 4" green wire from the top of R1 to J21A-D.

6) Connect a 16" piece of RG-174/U coax to P22, center to center, shield to sleeve. Connect the other end tc J21A, center to J21A-1, shield to J21A-A.

7) Connect a 4" black wire from J21A-A to the COMMON terminal on the front edge of the Receiver Amplifier ZA35279.

8) Connect a 13" black wire from the sleeve of J23 to the same COMMON terminal used in step (7).

9) Cut 19" lengths of the following color wires -

1 ea black	3 ea purple
2 ea brown	2 ea gray
2 ea yellow	1 ea white
2 ea green	1 ea red (22" long)
2 ea blue	

10) Cut a 15" piece of 3/8" D shield braid. Pull the wires cut in (9) through this sleeve with 2" protruding at each end.

11) Solder a 2" piece of black wire to one end of the braid.

12) Slip a 15" length of 3/8" D clear plastic tubing over the shield braid.

13) Connect the shield braid ground wire to a small ground lug under the nut attaching the upper end of P21.

14) Connect the red wire in the cable to the center of J23 (use plastic sleeve) and to J21A-20.

15) Connect the green wire in the cable from P21-16 to J21A-H.

16) Being careful to avoid confusion between wires of the same color, connect P21 pins 2 through 15 with the correct terminal among J21A, K through Z. Use an ohmmeter for wire identification.

17) Use cable clamp to hold the cable of (9) - (15) to the top surface of the RF-IF Module.

18) Use cable clamp to hold the RG-174 cable and the black wire from J23 to the top surface of the RF-IF Module.

19) Install the Gain Control card S3001 in J21A with the components toward the open side of the Module (toward the viewer). Install the card guide-clamps to hold the card in place.

4.4 LOCAL OSCILLATOR AND SERVO MODULE

This module is modified by the addition of the S1001 and S2001 cards, the added wiring to the module's connectors to the main chassis, of the receiver, and by minor alterations of other wiring in the module for computer-controlled operation of the receiver. The wiring for the S1001 card is shown on figure 9 and for the S2001 card on figure 10. The wiring to the module's connectors is shown on figure 6. The remaining wiring changes are scattered on figures 8 through 10.

All wiring will be done with #26 AWG Teflon insulated wire. Connections to the rear-panel connectors P15, 16, 19, 20 should have plastic tubing sleeves of 1/2" of clear PVC tubing, size #13. Slip the sleeve over the wire before soldering and then slip it over the connector terminal after the solder has cooled.

1) Four cables should be made prior to wiring inside the unit. These are W1001, W1002, W2001, and W2002. (See figures 20 through 23.) In each case one of these wires carries a connector. Each wire is crimped into a connector contact (Amp #86015-1) and then the connector is pushed into the appropriate hole in the connector block (Amp 86148-4). Keying plugs are installed in the appropriate locations by crimping a contact without a wire and then inserting it in the block. This contact will capture the keying plug (Amp 86286-1) when it is inserted.

12) The other switch on this layer of S2 is section A. Disconnect the green wire from the tap of section A, S2, and tie the free end back. Connect the brown wire of W2002 to the tap of section A of S2. Clip out jumper wire connecting stationary terminals A3 and B3 of Servo switch S2.

13) Section C can be located on the rear layer of S2 since all of its stationary terminals are used. Disconnect and tie back the green wire from the tap on section C of S2. Connect the orange wire of W2002 to the tap of section C of S2.

14) Dress all of the cables and use Tie-Wraps to improve the stability of the wiring. Attach remaining wires of W2002 per cable drawing on figure 23.

4.5 CARD MODIFICATIONS

Three cards in the receiver must be modified for computer-controlled operation. The cards are each shown in their entirety in the manuals supplied with the receiver. The modified portions only are shown on figure 12.

4.5.1 CARD D582-AB

There are several cards of this type in the receiver, but only the one in slot B7 is modified. It should be tagged so that it will not be mixed up with the other cards of the same type.

A jumper on this card is moved to route the signal out through phase shift circuit on card S1001 (figure 14) and back into the card. The jumper which connects from near pin V to near pin Z is removed. Replace it with a bare #22 wire jumper from the old location near pin Z to pin X. Mark this modified card with a label "B7 only" on the visible top edge of its handle.

4.5.2 CARD D586-AB

A resistor is added to this card to ensure that the TUNING lamp output, which is used by the INE circuitry, is pulled high even if the lamp burns out. Connect a 33,000 ohm, 1/4 watt resistor from pin M to pin 6 on this card. The card is used in card location A4 and is shown on figure 9.

4.5.3 CARD D592-AA

A resistor and a capacitor are added to this card to provide an isolated output for the phase difference. The card is used in card location A1 and is shown on figure 8.

Notice that the keying plug is NOT square, it must be inserted with the long dimension of its head parallel with the long dimension of the block.

2) After the cables have been constructed, dress cable W1001 down the side of the central guide toward the left of the front panel and fan out the leads to pick up their terminals on the mother board of the Module. Attach cable per figure 20.

3) Attach the free ends of W1002 to P19, using plastic sleeves.

4) Attach the free ends of W2001 to P15 and P20, using plastic sleeves. NOTE: Use the chassis ground terminal between P15 and P16 for ground connections to pins 1 and 26 of J42.

5) Dress cable W2002 down the side of the central guide to the right of the front panel, and connect the fanned-out wires to the appropriate pins of the mother board. Nine long wires will still await attachment.

6) Disconnect the green wire from the + terminal of Meter M2 (figure 10) and tie back against the side of the black wires to the other terminal of this meter. Then connect the correct green wire of W2002 to the meter terminal.

7) Disconnect the jumper wire from tap of section A of S1 to the tap of section B of S1. Disconnect and tie-back the green wire that formerly connected to this jumper. Connect the yellow wire of W2002 to the tap of section A of S1 (resistor layer). Connect the remaining green wire of W2002 to the tap of section B of S1 (capacitor layer).

8) Disconnect the jumper wire between the tap of section C of S1 and the tap of section D of S1. Also disconnect and tie back the green wire that formerly connected to these jumpered terminals. Connect the blue wire of W2002 to the tap of section C of S1 (resistor layer). Connect the purple wire of W2002 to the tap of section D of S1.

9) Connect the gray wire of W2002 to the jumper which connects positions 1-5 of the B layer of S1.

10) Connect the white wire of W2002 to the jumper which connects positions 1-5 of the D layer of S1.

11) The Mode switch, S2 has two layers, each of which has two single-pole, 5-position switches. Find the section which has connections to only two of the five stationary terminals. This is section B. Disconnect the green wire from the tap of section B, S2, and tie the free end back. Connect the red wire from W2002 to the tap of section B, S2.

Connect a 3600 ohm, 1/4 watt resistor, R33, from the emitter of Q3 to connector pin M. Connect a 2.2 microfarad, 25 volt capacitor, C12, from the circuit common to connector pin M.

4.6 NEW CARDS

Three new cards are needed for computer-controlled operation of the receiver: S1001, S2001 and S3001. The first two are used in the Local Oscillator and Servo Module and the latter in the RF-IF Amplifier Module.

4.6.1 S1001 CARD

4.6.1.1 CONSTRUCTION

This card (figures 13 and 14) contains a number of plated-through holes used for jumping from one side of the card to the other, and holes for some components that were not used in the final design. Thus, there will be many unfilled holes when the card is completed. Be sure that the diodes are mounted in the correct directions and be sure to install the insulated jumper next to CR2. The components may be installed in any order, except for C3 and U1 through U4. C3 should be the last component installed, and U1 through U4 the next to last components installed. To avoid possible static electricity damage, be sure to ground the soldering iron and the circuit ground terminal before installing U1 through U4. There is a mark next to pin 1 of all integrated circuits on both the top and bottom of the board.

4.6.1.2 ADJUSTMENTS

There are four adjustments on the S1001 card which must be made afer it is installed in the receiver. Two of these adjustments compensate for offset in the zero output and two provide full-scale (gain) adjustment. These adjustments will require the use of the Test Unit.

a) Amplitude channel. Switch the receiver to manual control and its Servo Switch to track. Examine the Amplitude output with the digital voltmeter (DVM) of the Test Unit. With the receiver tuned to a moderately strong station, or to the Simulator output, adjust the receiver gain control until the front-panel Signal Strength meter reads exactly "-20 dB". Now adjust R28 on the card for zero Amplitude output as indicated on the Test Unit DVM. Readjust the receiver gain control until its Signal

Strength meter reads exactly "+20 dB". Now adjust R31 of the card until the Test Unit DVM reads +10.00 volts. The Amplitude channel has now been adjusted.

b) Phase channel. With the receiver still on manual control and the Signal Strength meter indicating mid-scale, set the Servo switch to Negative Slew and the Tracking Rate control to 0.3 μs/s. Observe the Phase output of the receiver with the Test Unit DVM. As the value indicated on the DVM approaches zero, adjust R38 on the card to keep the DVM indicating zero. When the phase jumps from 0 to 360° stop turning R38. To confirm that 0° is represented by zero volts, switch to Positive Slew and observe that just after jumping from 360° to 0° the DVM reads essentially zero. The full scale adjustment R41 is made with Positive Slew as the phase approaches 360° in a like manner, keeping the DVM indicating 7.816 volts. This completes the adjustments for the S1001 card.

4.6.1.3 PARTS LIST

Designator	Description	Manufacturer	Part Number
S 1001	Circuit Card	Divelpro	
AR 1 to AR 4	Amplifier, Integrated Circuit 8-pin DIP	Texas Instruments	SN72741P
C 1	Capacitor, 4.7 nF, 80 V, 10%	Sprague	type 192P
C 2	Capacitor, 220 pF, 5%	dipped mica	CM05
C 3	Capacitor, 150 pF, 5%	dipped mica	CM05
C 4	Capacitor, 100 pF, 5%	dipped mica	CM05
C 5	Capacitor, 0.22 µF, 80 V, 10%	Sprague	type 192P
C 6	Capacitor, 100 pF, 5%	dipped mica	CM05
C 7	Capacitor, 0.22 µF, 80 V, 10%	Sprague	type 192P
C 8	Capacitor, 0.22 µF, 80 V, 10%		
CR 1	Diode, signal, 1N3064		
CR 2	Diode, regulating, 4.7V, 5% 1N750A		
CR 3	Diode, regulating, 6.2V, 5% 1N753A		
P 1	Connector terminal Post (25 ea)	AMP, Inc	85931-6
P 2	Connector Terminal Post (24 ea)	AMP, Inc	85931-6
Q 1	Transistor, FET, 2N4092	Motorola, etc.	
Q 2	Transistor, bipolar 2N2222 or 2N2219		
Q 3	Transistor, bipolar 2N2222 or 2N2219		
Q 4 to Q 13	Transistor, FET, 2N4092	Motorola, etc.	
R 1	Resistor, 12 K, 1/4 W, 2% or 5%		
R 2	Resistor, 15 K, 1/4 W, 2% or 5%		
R 3	Resistor, 15 K, 1/4 W, 2% or 5%		

R 4	Resistor, 12 K, 1/4 W, 2% or 5%		
R 5	Resistor, 22 K, 1/4 W, 2% or 5%		
R 6	Resistor, 1000 ohms, 1/4 W, 2% or 5%		
R 7	Resistor, 4.7 K, 1/4 W, 2% or 5%		
R 8	Resistor, 4.7 K, 1/4 W, 2% or 5%		
R 9	Resistor, 24 K, 1/4 W, 2% or 5%		
R 10	Resistor, 7.5 K, 1/4 W, 2% or 5%		
R 11	Resistor, 7.5 K, 1/4 W, 2% or 5%		
R 26	Resistor, 100 K, 1/4 W, 2% or 5%		
R 27	Resistor, 1 M, 1/4 W, 2% or 5%		
R 28	Potentiometer, multiturn, 10 K	Dale	1680
R 29	Resistor, 10 K, 1/4 W, 2% or 5%		
R 30	Resistor, 12 K, 1/4 W, 2% or 5%		
R 31	Potentiometer, multiturn, 10 K	Dale	1680
R 32	Resistor, 4.7 K, 1/4 W, 2% or 5%		
R 33	Resistor, 4.3 K, 1/4 W, 2% or 5%		
R 34	Resistor, 47 K, 1/4 W, 2% or 5%		
R 35	Resistor, 47 ohms, 1/4 W, 2% or 5%		
R 36	Resistor, 15 K, 1/4 W, 2% or 5%		
R 37	Resistor, 150 K, 1/4 W, 2% or 5%		
R 38	Potentiometer, multiturn, 10K	Dale	1680

R 39	Resistor, 10 K, 1/4 W, 2% or 5%		
R 40	Resistor, 5.6 K, 1/4 W, 2% or 5%		
R 41	Potentiometer, multiturn, 10 K		
R 42	Resistor, 24 K, 1/4 W, 2% or 5%		
R 43	Resistor, 4.3 K, 1/4 W, 2% or 5%		
R 44	Resistor, 47 K, 1/4 W, 2% or 5%		
R 45	Resistor, 47 ohms, 1/4 W, 2% or 5%		
R 46	Resistor, 15 ohms, 1/4 W, 2% or 5%		
R 47	Resistor, 330 ohms, 1/4 W, 2% or 5%		
R 48	Resistor, 1000 ohms, 1/4 W, 2% or 5%		
U 1	Integrated Circuit, CMOS, 4X2NOR	RCA	CD 4001 AE
U 2	Integrated Circuit, CMOS, 2X D FF	RCA	CD 4013 AE
U 3 & U 4	Integrated Circuit, CMOS, 4X FF	RCA	CD 4018 AE

4.6.2 S2001 CARD

4.6.2.1 CONSTRUCTION

This card (figure 15) contains 11 dual-inline relays and 4 larger DPDT relays as well as a number of resistors. The connectors P1 and P2 are made up from terminal posts pressed into the circuit board. The posts protrude from the side of the board carrying the SERIAL (the bottom). They are pressed in from the top and then soldered on the TOP side only. The mating connector requires the pins to be "square" with the connector, so be sure that they are aligned before pressing each into place. All other components are mounted on the TOP side of the board and soldered on the bottom side only.

The dual-inline relays are mounted in locations marked K1 to K6, K12 to K16. Be sure to place the end with the notch toward the little mark on the board next to pin 1 of each relay. This is toward the edge of the board with P1 for K3 to K5 and K12 to K15. The others are reversed.

The larger relays K7 to K10 are mounted with their coil ends toward P1. The marking on the top of these relays is unreliable. The coil terminals are round, not square wire. Check with an ohmmeter to confirm the pin connections. The resistors are mounted in the identified locations.

4.6.2.2 PARTS LIST

Designator	Description	Manufacturer	Part Number
S 2001	Circuit Card	Divelpro	
CR 1	Diode, Signal, 1N3064		
K 1 to K 6	Relay, SPST, NO, 10 mA	Grigsby-Barton	GB 821A-4E
K 7 to K 10	Relay, DPDT, 140 ohms	Hathaway	65627-4
K 11	Not Used		
K 12 to K 16	Relay, SPST, NO, 10 mA	Grigsby-Barton	GB 821A-4E
P 1	Connector Terminal Post (21 ea)	AMP, Inc.	85931-6
P 2	Connector Terminal Post (24 ea)	AMP, Inc.	85931-6
R 1	Resistor, 47 K, 1/4 W, 2% or 5%		
R 2	Resistor, 47 K, 1/4 W, 2% or 5%		
R 3	Resistor, 18 K, 1/4 W, 2% or 5%		
R 4	Resistor, 8.2 K, 1/4 W, 2% or 5%		
R 5	Resistor, 91 K, 1/4 W, 2% or 5%		
R 6	Resistor, 15 K, 1/4 W, 2% or 5%		
R 7	Resistor, 4.7 K, 1/4 W, 2% or 5%		

4.6.3 S3001 CARD

4.6.3.1 CONSTRUCTION

This card (figure 16) contains 14 dual-inline relays and one larger DPDT relay in addition to a number of resistors. All parts are mounted on the side of the board carrying the SERIAL.

The dual-inline relays are mounted so that the end with the notch is away from the board edge-connector. In the case of K 1 and K 2, the notch is next to the edge of the board. The DPDT relay K 15 is mounted with the coil end away from the edge-connector. Unfortunately, the top marking of this relay is unreliable. The coil terminals are round, not rectangular, and should be verified using an ohmmeter. The resistors should be mounted in the identified locations. The lower or only resistors should normally be the one nearest the associated relay.

Carefully solder all terminals on the bottom of the board. All holes are plated-through, so soldering on the bottom is sufficient.

4.6.3.2 PARTS LIST

Designator	Description	Manufacturer	Part Number
S 3001	Circuit Board	Divelpro	
K 1 to K 14	Relay, SPST, NO, 10 mA	Grigsby-Barton	GS 821A-4E
K 15	Relay, DPDT, 140 ohms	Hathaway	65627-4
R1 a	Resistor, 2.7 ohms, 1/2 W, 5% or 2%		
R1 b	Resistor, 12 ohms, 1/4 W, 5% or 2%		
R2 a	Resistor, 13 ohms, 1/4 W, 5% or 2%		
R2 b	Resistor, 13 ohms, 1/4 W. 5% or 2%		
R3	Resistor, 16 ohms, 1/4 W, 5% or 2%		
R4	Resistor, 33 ohms, 1/4 W, 5% or 2%		
R5	Resistor, 68 ohms, 1/4 W, 5% or 2%		
R6 a	Resistor, 150 ohms, 1/4 W, 5% or 2%		
R6 b	Resistor, 1.8 K, 1/4 W, 5% or 2%		
R7 a	Resistor, 300 ohms, 1/4 W, 5% or 2%		
R7 b	Resistor, 4.3 K, 1/4 W, 5% or 2%		
R8	Resistor, 560 ohms, 1/4 W, 5% or 2%		
R9	Resistor, 1.1 K, 1/4 W, 5% or 2%		
R10	Resistor, 2.2 K, 1/4 W, 5% or 2%		
R11 a	Resistor, 4.7 K, 1/4 W, 5% or 2%		
R11 b	Resistor, 110 K, 1/4 W, 5% or 2%		

R12 a	Resistor, 18 K, 1/4 W, 5% or 2%
R12 b	Resistor, 18 K, 1/4 W, 5% or 2%
R13	Resistor, 18 K, 1/4 W, 5% or 2%

5. ADACS INTERFACE CHASSIS CONSTRUCTION

5.1 GAIN-TRACKING-PHASE CARD

5.1.1 CONSTRUCTION

This card uses TTL integrated circuits and the components may be installed in any order. The circuitry of the card is shown on figures 31 and 32.

5.1.2 PARTS LIST

Designator	Quantity	Description	Manufacturer	Part Number
Gain-Tracking-Phase	1	Circuit Card	Divelpro	------
A, B and C	3	Binary to 1 of 16 decoder, TTL levels	Motorola	MC 8311P
D, E, H and J	4	Triple 3-Input Positive NAND Gates, TTL	Texas Instruments	SN 7410N
F and G	2	Quad 2-Input Positive NAND Gates, TTL	Texas Instruments	SN 7400N
M, N and S	3	Hex Inverter, Open Collector, TTL	Texas Instruments	SN 7405N
R	1	Hex Inverter, Open Collector, High Current, TTL	Texas Instruments	SN 7406N
L	1	8-Input Positive NAND Gate, TTL	Texas Instruments	SN 7430N
K and P	2	One shot	Fairchild	F 9601
R1 and R2	2	Resistor, 1500 ohms 1/4 watt, ±2 percent, tin oxide film	------	------
R3 and R4	2	Resistor, 3900 ohms, 1/4 watt, ±2 percent, tin oxide film	------	------
C1, C2 and C3	3	Capacitor, .001 microfarad, ±10 percent	Sprague	Pacer Filmite

5.2 BLANKING & INE CARD (S4001)

5.2.1 CONSTRUCTION

This card (figures 33 and 34) contains a wide variety of components. Their locations are labeled on the bottom of the board with one exception, R21, which is located between the edge connector and R22. Be sure to observe the polarity of the electrolytic capacitors and the diodes. There is a mark on the bottom of the board near pin 1 of all integrated circuits. The components may be inserted in the board in any order with the exception that U1 should not be installed until all other components are installed and soldered. Be sure to ground the soldering iron and circuit board ground terminal before installing or changing U1. This device is of MOS construction (though it does have protective diodes), so static electricity could damage the device unless these precautions are taken. (Once installed, circuit impedances offer sufficient protection.)

5.2.2 ADJUSTMENT

The circuit on this card for converting the Blanking Pulses into an analog Percent Blanking voltage has both a zero setting and a full scale setting. The zero setting uses a fixed resistor and the full scale setting uses an adjustable pot.

Remove the cable to J6, connect a coax cable from J7 to the External input connector on the front panel of the Test Unit, and set the Function switch of the Test Unit to External. The voltage indicated on the DVM (digital voltmeter) in the Test Unit should be zero, plus or minus 50 millivolts. If not, a new value for R17 is needed. Use a higher value of resistance if the voltage is negative.

With the cable to J6 still disconnected, connect a shorting cap to J6. The DVM voltage should be adjusted with R18A on the card to give a reading of + 10.00 volts.

5.2.3 PARTS LIST

Designator	Description	Manufacturer	Part Number
S 4001	Circuit Card	Divelpro	
AR 1	Amplifier, Integrated Circuit (8-pin DIP)	Texas Instruments	SN72741P
AR 2	Amplifier, Integrated Circuit (8-pin DIP)	Texas Instruments	SN72741P
C 1	Capacitor, 1 nF, 200 V, 10%	Sprague	type 192P
C 2	Capacitor, Tantalum Electrolytic, 10 µF, 20V		CS13BE106M
C 3	Capacitor, dipped mica, 390 pF		CM05
C 4	Capacitor, Tantalum Electrolytic, 47µF, 20V		CS13BE476M
C 5	Capacitor, Tantalum Electrolytic, 47 µF, 20V		CS13BE476M
C 6	Capacitor, Tantalum Electrolytic, 47 µF, 20V		CS13BE476M
C 7	Capacitor, 1nF, 200 V, 10%	Sprague	type 192P
C 8	Capacitor, 1nF, 200V, 10%	Sprague	type 192P
CR 1 to CR 5	Diode, Signal, 1N3064		
CR 6	Diode, regulating, 7.5 V, 5%, 1N755A		
CR 7 to CR 9	Diode, Signal, 1N3064		
CR 10	Diode, Power, 1N4005		
CR 11	Diode, Signal, 1N3064		
Q 1	Transistor, PNP, Silicon, 2N2905 or 2N2907		
Q 2	Transistor, NPN, Silicon, 2N2222 or 2N2219		
Q 3	Transistor, FET, n Chan, 2N4092		
Q 4	Transistor, PNP, Silicon, 2N2905 or 2N2907		
Q 5	Transistor, NPN, Silicon, 2N2222 or 2N2219		

R 1	Resistor, 33 K, 1/4 W, 2% or 5%
R 2	Resistor, 100 K, 1/4 W, 2% or 5%
R 3	Resistor, 22 K, 1/4 W, 2% or 5%
R 4	Resistor, 43 K, 1/4 W, 2% or 5%
R 5	Resistor, 100 K, 1/4 W, 2% or 5%
R 6	Resistor, 750 K, 1/4 W, 2% or 5%
R 7	Resistor, 300 K, 1/4 W, 2% or 5%
R 8	Resistor, 47K, 1/4 W, 2% or 5%
R 9	Resistor, 47 ohms, 1/4 W, 2% or 5%
R 10	Resistor, 47 K, 1/4 W, 2% or 5%
R 11	Resistor, 75 K, 1/4 W, 2% or 5%
R 12	Resistor, 100 K, 1/4 W, 2% or 5%
R 13	Resistor, 3.3 K, 1/4 W, 2% or 5%
R 14	Reistor, 130 K, 1/4 W, 2% or 5%
R 15	not used
R 16	Resistor, 200 K, 1/4 W, 2% or 5%
R 17	Resistor, chosen for zero output with pin X open
R 18	Resistor, 220 K, 1/4 W, 2% or 5%
R 18A	Potentiometer, multiturn, 10 K
R 19	Resistor, 47 ohms, 1/4 W, 2% or 5%
R 20	Resistor, 110 K, 1/4 W, 2% or 5%

R 21	Resistor, 15 K, 1/4 W, 2% or 5%		
R 22	Resistor, 15 K, 1/4 W, 2% or 5%		
R 23	Resistor, 10 K, 1/4 W, 2% or 5%		
R 24	Resistor, 10 K, 1/4 W, 2% or 5%		
R 25	Resistor, 6.8 ohms, 1/2 W, 5%		
R 26	Resistor, 10 K, 1/4 W, 2% or 5%		
R 27	Resistor, 6.8 K, 1/4 W, 2% or 5%		
R 28	Resistor, 1000 ohms, 1/4 W, 2% or 5%		
R 29	Resistor, 5.6 K, 1/4 W, 2% or 5%		
R 30	Resistor, 6.8 K, 1/4 W, 2% or 5%		
R 31	Resistor, 6.8 K, 1/4 W, 2% or 5%		
R 32	Resistor, 6.8 K, 1/4 W, 2% or 5%		
R 33	Resistor, 6.8 K, 1/4 W, 2% or 5%		
R 34	Resistor, 1.8 K, 1/4 W, 2% or 5%		
R 35	Resistor, 100 K, 1/4 W, 2% or 5%		
R 36	Resistor, 680 ohms, 1/4 W, 2% or 5%		
R 37	Resistor, 430 ohms, 1/4 W, 2% or 5%		
U 1	Integrated ckt, CMOS, 6X BUF	RCA	CD 4010 AE
U 2	Integrated ckt, TTL, 4X2NAND(PWR)	Sprague	UHP408
U 3	Integrated ckt, TTL, 4X LATCH	Texas Instruments	SN7475N

U 4	Integrated ckt, Magnitude Compare	Texas Instruments	SN74L85N
U 5	Integrated ckt, One-Shot MV	Texas Instruments	SN74L122N
U 6	Assembly, Digital-to-Analog Converter	Datel DAC	198B or 298B

5.3 CHASSIS

5.3.1 CONSTRUCTION

The basic chassis for the ADACS unit is shown on figure 41. The front panel is drilled and engraved as shown on figure 42 and the back panel is drilled, cut-out and engraved as shown on figure 43. The floor of the unit is drilled and cut-out as shown on figure 44.

The components on the front and back panels are installed next, as shown on figure 45. Install the bulbs in the incandescent lamps and the fuse in the fuse holder. Check each of the multi-pin cable connectors for a well-secured nut in the center to hold the plug, as some have been delivered with a loose nut that later becomes a nuisance.

Connect all of the wires to the two power supplies with the power supplies on the work bench positioned as they will be in the chassis, except for the three output wires on the plus and minus 15 volt power supply. (It is quite difficult to tighten the screws to the terminal strip on the 5 volt power supply when it is mounted in the chassis.) The wiring is shown on figure 26 through 29.

Mount the power supplies using the correct spacers for each supply, as shown on figure 46. Both power supplies use 3/4 inch long spacers, but one uses spacers with number 6 holes for its 6-32 screws and the other uses number 8 holes for its 8-32 screws. It is easier to mount the supplies if the chassis is placed on its side so that one's hand can go through the rectangular ventilation hole to hold the spacers in place. Do not tighten the screws until all screws have been started.

Put each of the card sockets in a bench vise and solder the wires to each of the pins, observing the color code. (It is much neater to make up the cable harnesses this way than when the sockets are already mounted.) Use shrink tubing over the pins. (1/8 inch is good.) Use excess length for the wires, which will later be cut back to the appropriate length when the sockets are mounted. It is more convenient to use cable ties to group wires going to the connectors on the back panel.

Mount the card sockets, scraping off the anodizing around where the ground lug will go, as a good ground is desirable. Be sure to use a washer with teeth on this screw. Position the ground lug and the two terminal strips so as to clear the socket pins. Install the two resistors and the capacitor without soldering. Position them to clear the mounting screws.

Dress each group of wires going from adjacent card socket pins to a particular back panel connector for a neat, equal length appearance and cut to appropriate length. There is no need to seek minimum length, as there are no electrical problems. Attach the crimp pins and insert into the appropriate slots of the connectors. The remaining wires may be cut to length and soldered. Additional wires on the wiring diagram that are not yet installed should be installed now. (For example, J3 to J5, J1 to front panel.) The a.c. power wiring should be installed with shrink tubing over component contacts to reduce the chance of accidental electrical shock.

The black ground wires should be installed with special care, as it is important to make good electrical contact to the ground lug with each and the space on the lug is rather limited.

The coax from the BNC connectors should be soldered very carefully, as the amount of heat needed to attach the ground straps can easily melt the insulator and cause a short. Use cable ties as needed.

Before turning on a.c. power, check out the a.c. power path visually. Then test with a.c. power, but without the cards. Check for the correct voltage at the card pins. Adjust the d.c. level with the power supply adjustment pots, if necessary. Check the operation of the MAINTENANCE and MANUAL lamps with the toggle switches.

It is desirable to check out the wiring from the cards to the back panel using an ohmmeter, as there are likely to be some wiring errors.

Mount the cards in the chassis using the 1/2 inch spacers to keep the ends of the cards off the bottom of the chassis. (They also serve to keep the cards tight in the sockets for a dependable connection.)

The ADACS unit is now ready to be tested with the Test Unit.

5.3.2 PARTS LIST

Quantity	Manufacturer	Part No.	Description
1	Divelpro	DIV 472	Chassis with front and rear panels drilled and silk-screened
1	Lambda	LXD-3-152	±15 volt 400 mA power supply
1	Lambda	LXS-A-5-OV	5-volt 4-amp power supply
1	J-B-T	ST22N	Toggle switch (for rear panel)
2	Microswitch	23AT11	Toggle switches (for rear panel)
1	Drake	Postlite 105-025	Neon lamp assembly (Power On)
3	Dialco	184-9830-1871-604-Red	Lamp assembly (other front panel lamps)
3	G.E.	328	Bulb T-1-3/4 6-volt 0.2-amp.
1	Amphenol	160-5-N	Flush motor plug (AC power)
5	Amphenol	31-221	BNC connectors
1	Amphenol	126-010	5-pin socket (J4)
2	Amphenol	225-22221-101	44-pin card socket
1	Belden	17461	Extension cord
4	Herman H. Smith	1476	Angles
3	Herman H. Smith	2112	Spacers 1/2" high, hole for No. 6 screw
4	Herman H. Smith	2113	Spacers 3/4" high, hole for No. 6 screw
4	Herman H. Smith	2118	Spacers 3/4" high, hole for No. 8 screw

Quantity	Manufacturer	Part No.	Description
1	Elco	00-8016-056-000-001	Connector, 56-pin (J1)
3	Elco	00-8016-020-000-707	Connector, 20-pin (J2, J3 & J5)
72	Elco	60-8017-0313	Contacts for connector
1	Sprague	Pacer Filmite	.47 uF capacitor
1	-----	-----	27 ohm 2 percent 1/2 watt resistor
1	-----	-----	3300 ohm 2 percent 1/2 watt resistor
1	Vernitron	14301	feed through lug from terminal used as ground lug for ADACS
1	Littlefuse	342012A	3AG fuse extractor post
1	Littlefuse	313.500	1/2 ampere slow blow 3AG fuse
2	H. H. Smith	863	tie down terminal, 2 terminals

Quantity	Thread	Description
12	2-56	5/8 inch long fillister head brass machine screw
12	2	washer, cadmium plated steel, internal teeth
12	2-56	brass hexagon nut
4	4-40	1/2 inch long fillister head brass machine screw
4	4-40	1/2 inch long round head brass machine screw
4	4	washer, cadmium plated steel, round flat
8	4	washer, cadmium plated steel, internal teeth
8	4-40	brass hexagon nut
7	6-32	one inch long flat head brass machine screw
4	6-32	3/8 inch long flat head brass machine screw
3	6	washer, cadmium plated steel, round flat
7	6	washer, cadmium plated steel, internal teeth
7	6-32	brass hexagon nut
4	8-32	one inch long flat head brass machine screw

6. COMPUTER INTERFACE SPECIFICATIONS

The interface between the computer and the ADACS/receiver has the following characteristics:

6.1 ANALOG LINES TO THE COMPUTER:

Receiver J26 (Phase), BNC connector, 0 to +10 volts into at least 10,000 ohms.

Receiver J31 (Amplitude), BNC connector, 0 to +47.816 volts into at least 10,000 ohms.

ADACS J7 (Percent Blanked), BNC connector, 0 to +10. volts into at least 10,000 ohms.

6.2 ANALOG LINES FROM THE COMPUTER:

None.

6.3 DIGITAL LINES TO THE COMPUTER (TTL LEVELS):

ADACS J5 (Frequency and Cardioid bits, etc.). ELCO connector number 00-8016-020-000-707. Pin assignments are on figure 29. Each line will sink 4.8 milliamperes (3 TTL inputs). Pull-up resistors are required for bit lines.

ADACS J9 (Interrupt), one per computer system, BNC connector. Pulled to ground for about 2 microseconds by an ADACS/receiver when its status changes. This output is pulled up in ADACS and will drive at least 1 TTL input.

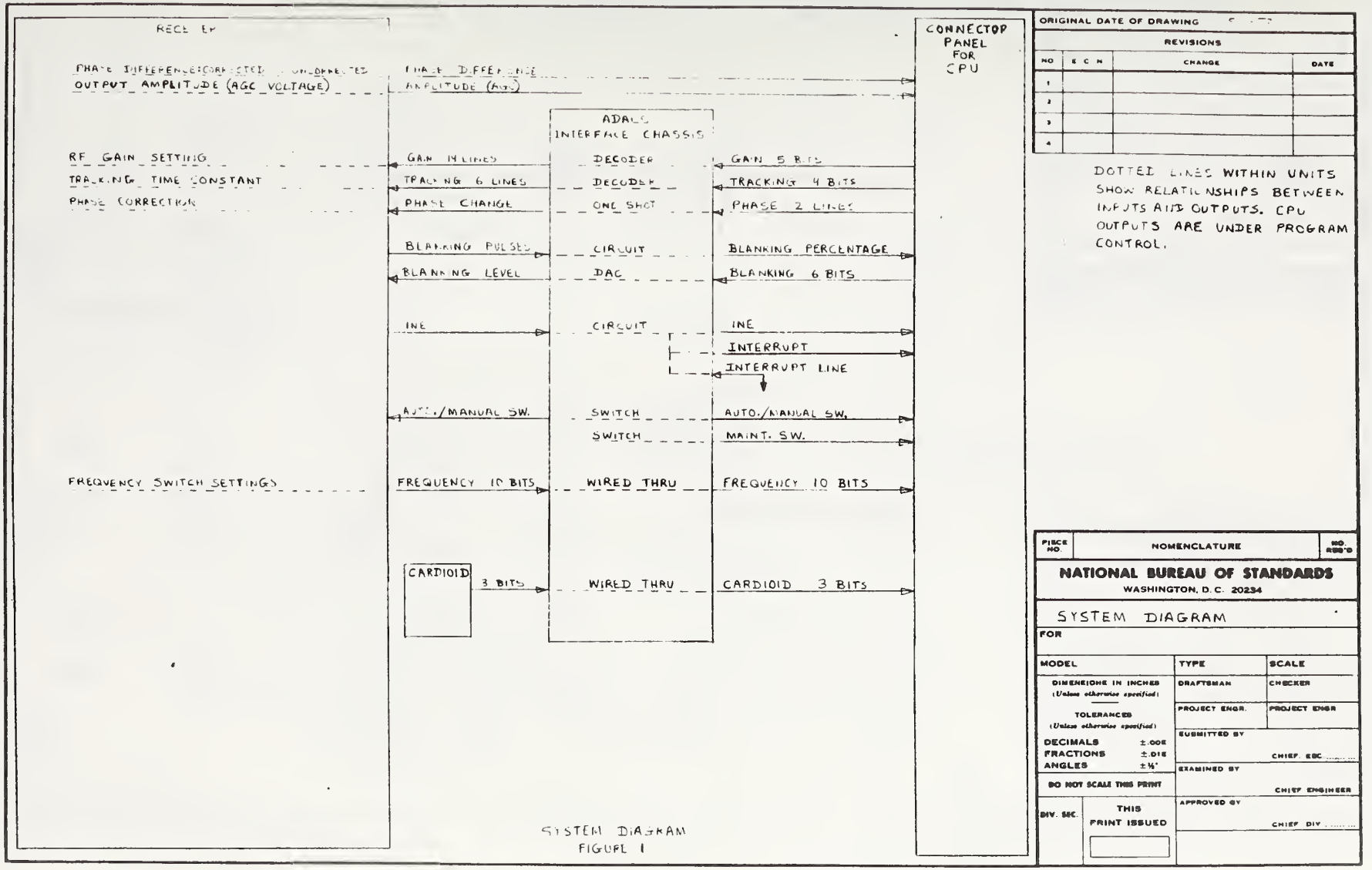
6.4 DIGITAL LINES FROM THE COMPUTER (TTL LEVELS):

ADACS J2 (Gain, Tracking, Phase and Blanking bits). ELCO connector number 00-8016-020-000-707. Pin assignments are on figures 27 and 28. Each bit must be able to sink at least 10. milliamperes (6 TTL inputs). The control word must always be present, since it is used directly without latching. One positive pulse of 10 to 150 microseconds duration must occur just after each time the control word is updated.

7. INSTALLATION

The Receiver and its ADACS unit should be mounted adjacent to each other in a 19-inch equipment rack. The receiver occupies 7 inches of panel space and the ADACS occupies 5-1/4 inches. It is suggested that a blank panel of 1-3/4 inch be placed between the Receiver and ADACS and also on the other side of the Receiver to allow cooling air passage. Following these suggestions, the total panel space occupied by one Receiving Subsystem is 15-3/4 inches.

Certain commercial equipment and materials are identified in this paper in order to adequately specify the components used. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.



SYSTEM DIAGRAM
FIGURE 1

ORIGINAL DATE OF DRAWING

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

DOTTED LINES WITHIN UNITS SHOW RELATIONSHIPS BETWEEN INPUTS AND OUTPUTS. CPU OUTPUTS ARE UNDER PROGRAM CONTROL.

PIECE NO.	NOMENCLATURE	NO. REQ'D

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SYSTEM DIAGRAM

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.00E FRACTIONS ±.01E ANGLES ±½°	SUBMITTED BY CHIEF, EEC	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF DIV

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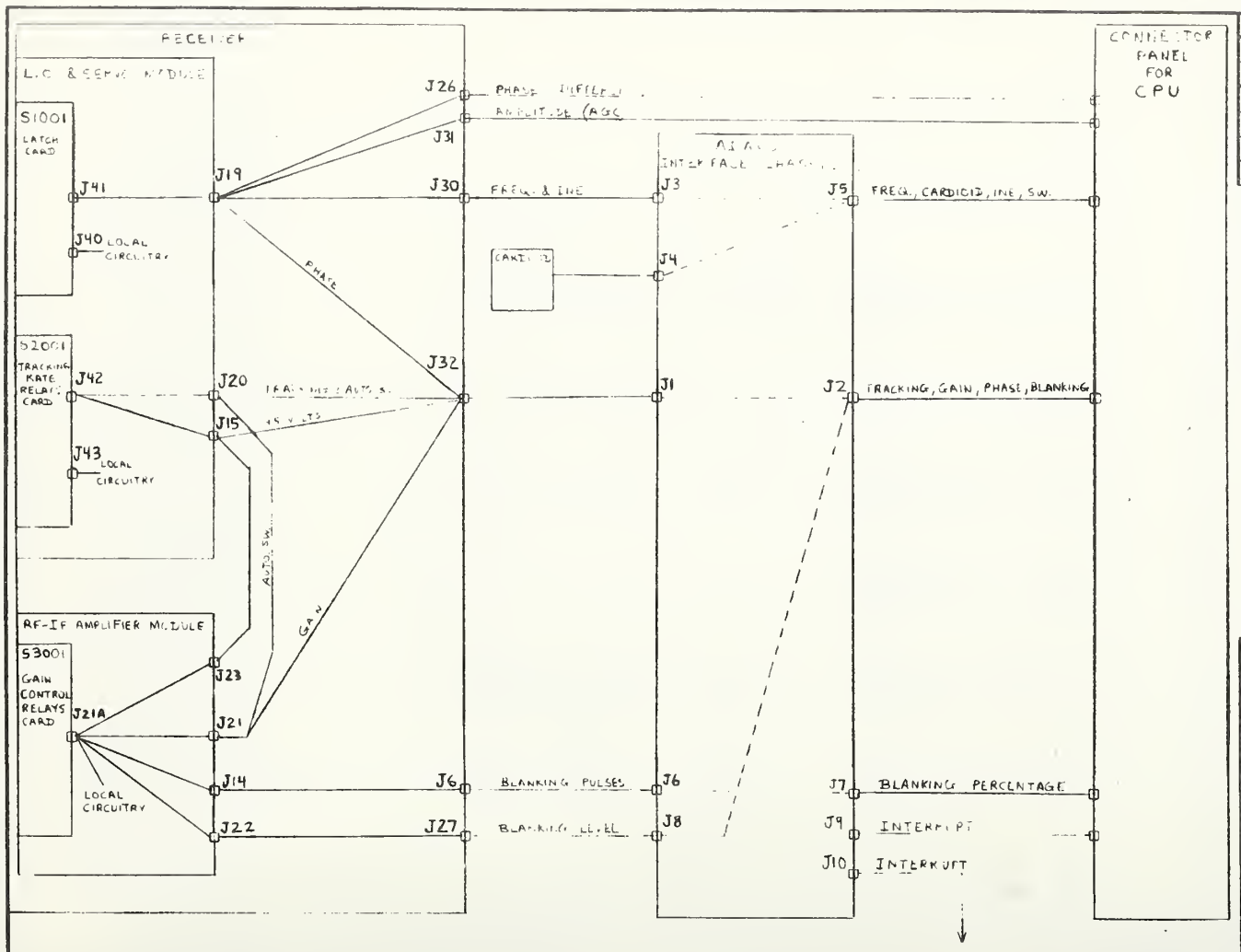

SYSTEM CABLE DIAGRAM
FIGURE 2

ORIGINAL DATE OF DRAWING 7?

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
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4			

PIECE NO	NOMENCLATURE	NO REQ'D

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SYSTEM CABLE DIAGRAM

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.00E FRACTIONS ±.01E ANGLES ±½°	SUBMITTED BY CHIEF, EEC.	
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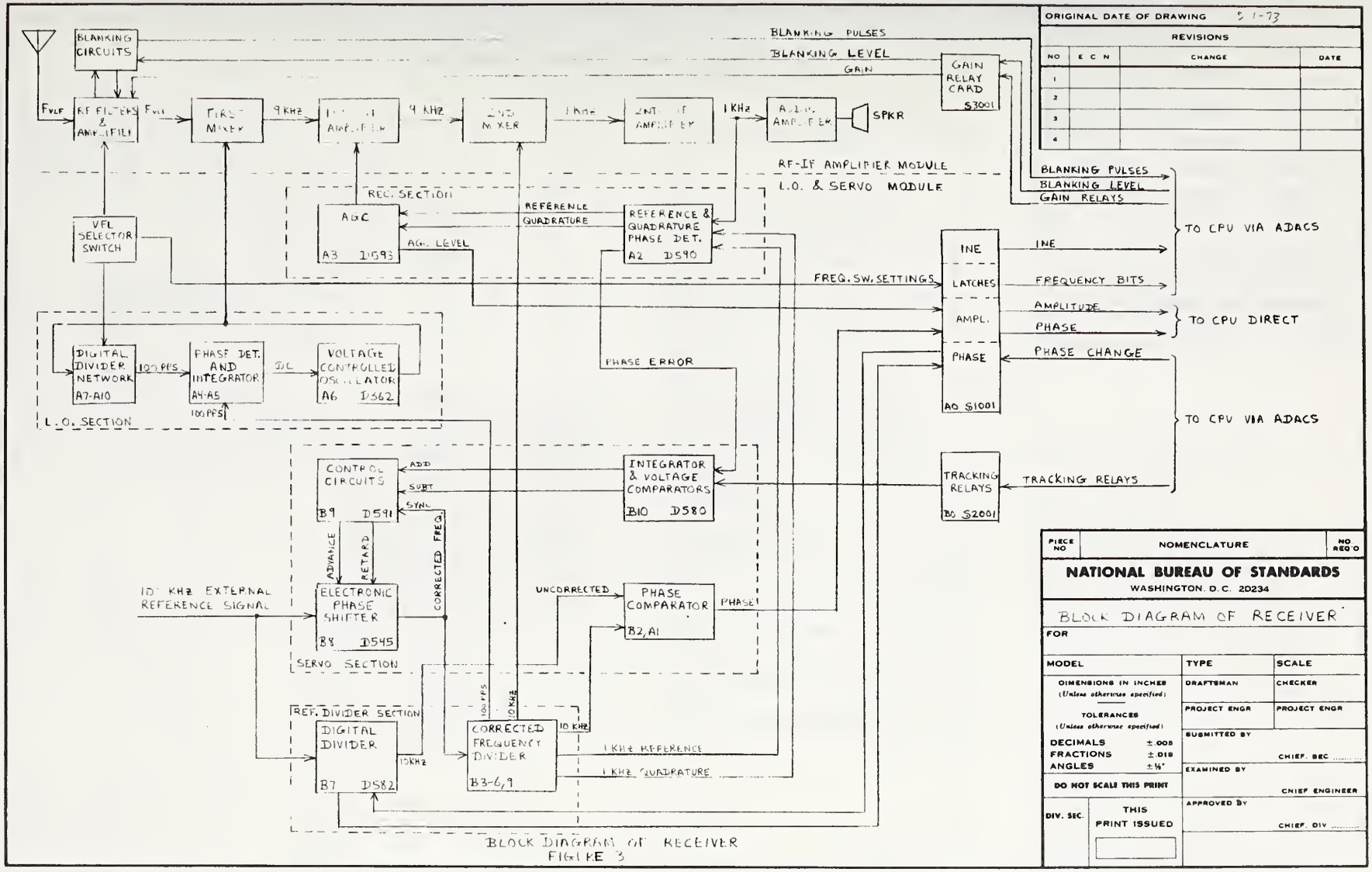

BLOCK DIAGRAM OF RECEIVER
FIGURE 3

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

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BLOCK DIAGRAM OF RECEIVER

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
DO NOT SCALE THIS PRINT		CHIEF ENGINEER
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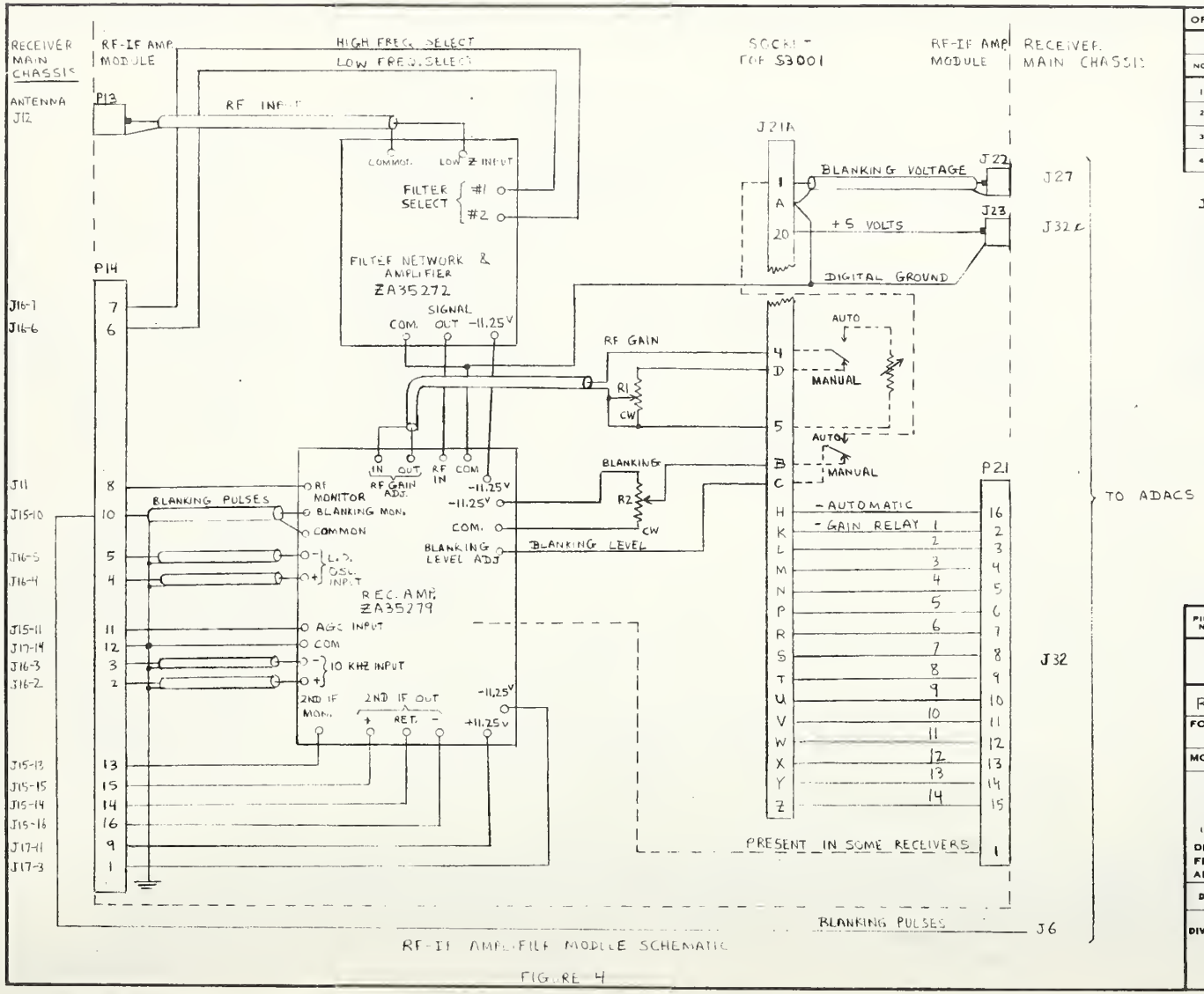

RF-IF AMPLIFIER MODULE SCHEMATIC

FIGURE 4

ORIGINAL DATE OF DRAWING 5-77			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
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4			

DOTTED WIRING IS ON S3001 CARD (J21A)

PIECE NO	NOMENCLATURE	NO. REQ'D

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RF-IF AMPLIFIER MODULE SCHEMATIC

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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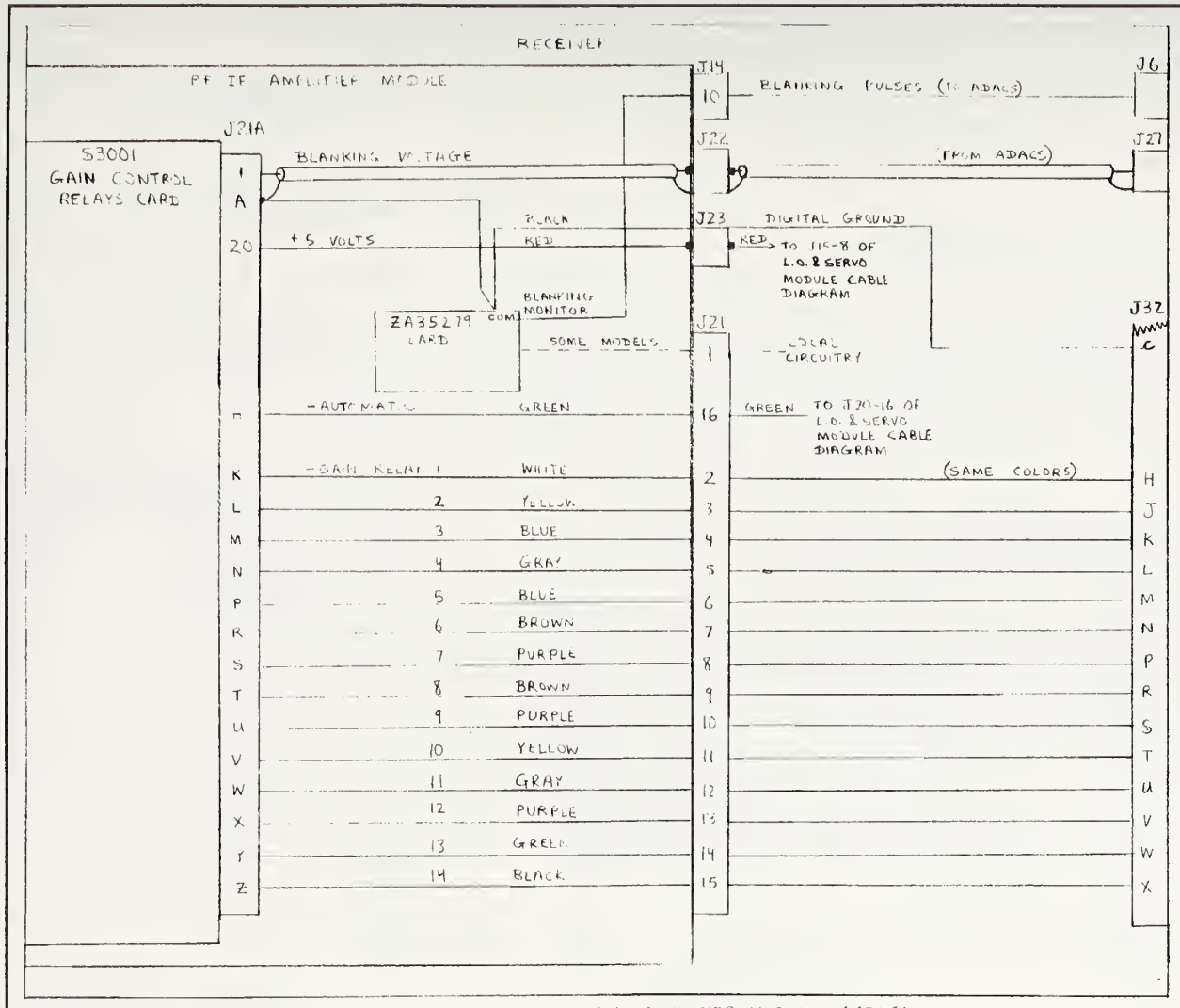

RF-IF AMPLIFIER MODULE CABLES

FIGURE 5

ORIGINAL DATE OF DRAWING	6-7

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO. REQ'D

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RF-IF AMPLIFIER MODULE CABLES

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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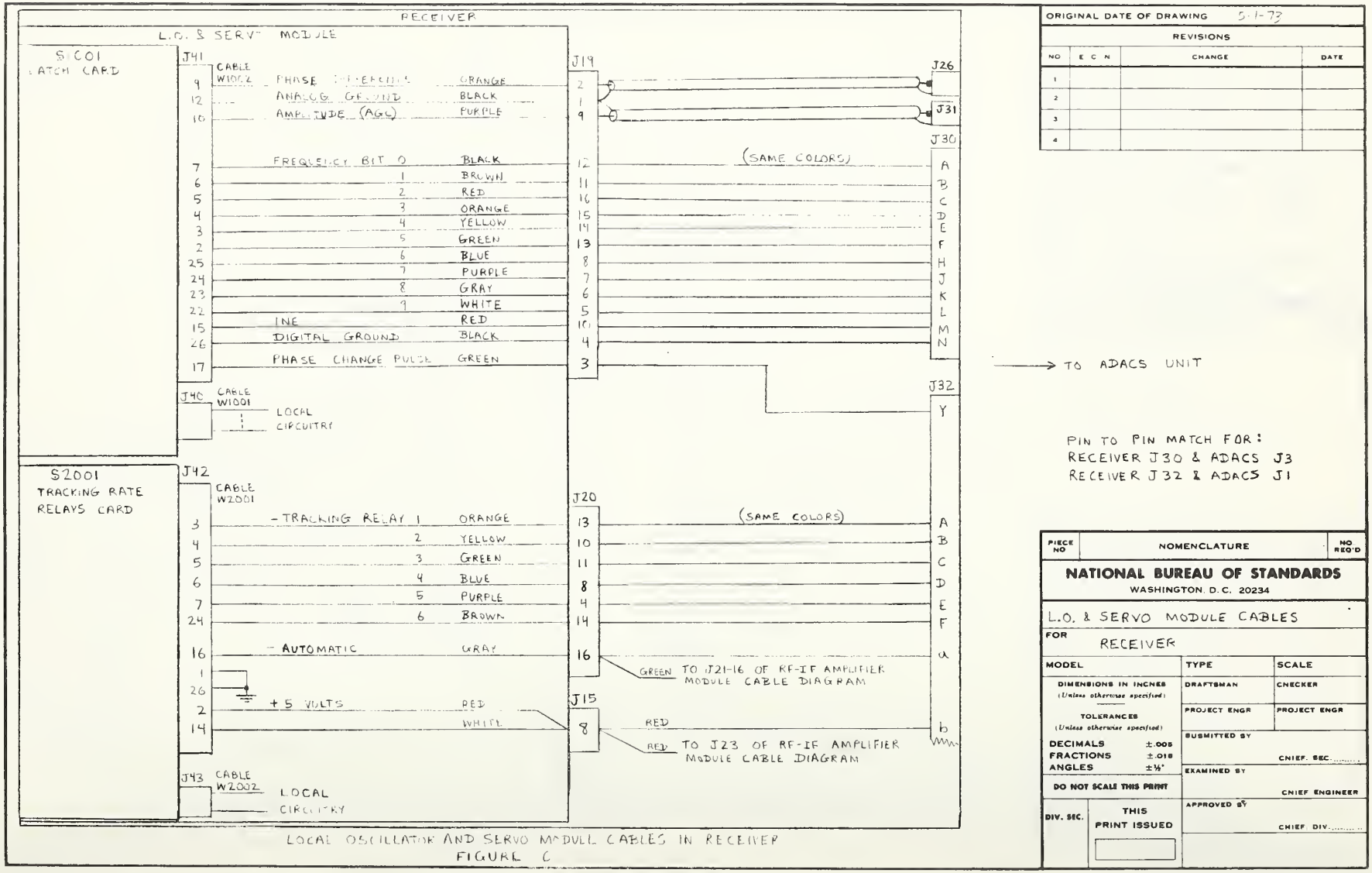

LOCAL OSCILLATOR AND SERVO MODULE CABLES IN RECEIVER
FIGURE C

ORIGINAL DATE OF DRAWING 5-1-73

REVISIONS

NO	E C N	CHANGE	DATE
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3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

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L.O. & SERVO MODULE CABLES
FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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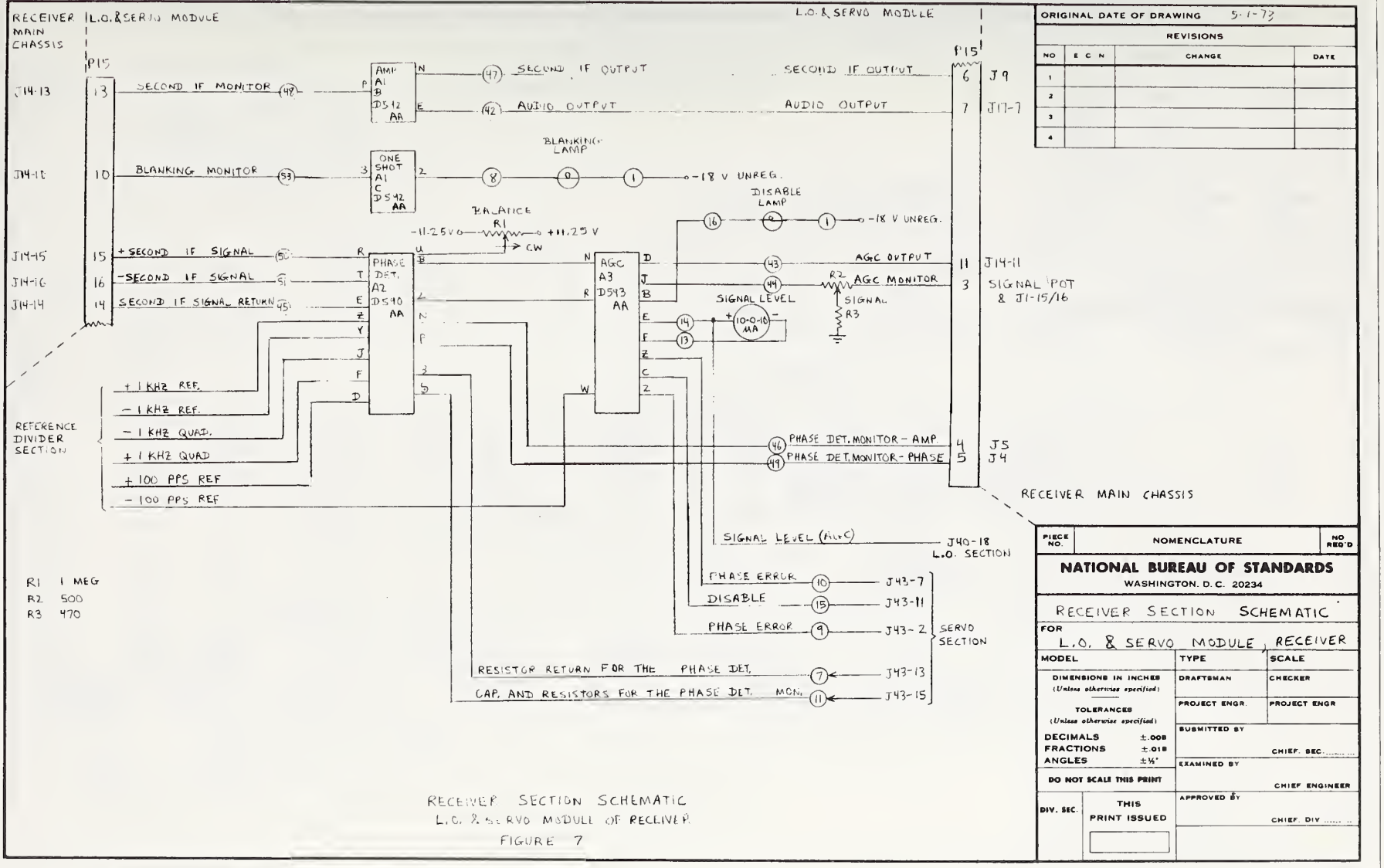

RECEIVER SECTION SCHEMATIC
L.O. & SERVO MODULE OF RECEIVER
FIGURE 7

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
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4			

PIECE NO.	NOMENCLATURE	NO REQ'D

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RECEIVER SECTION SCHEMATIC

FOR L.O. & SERVO MODULE RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.008 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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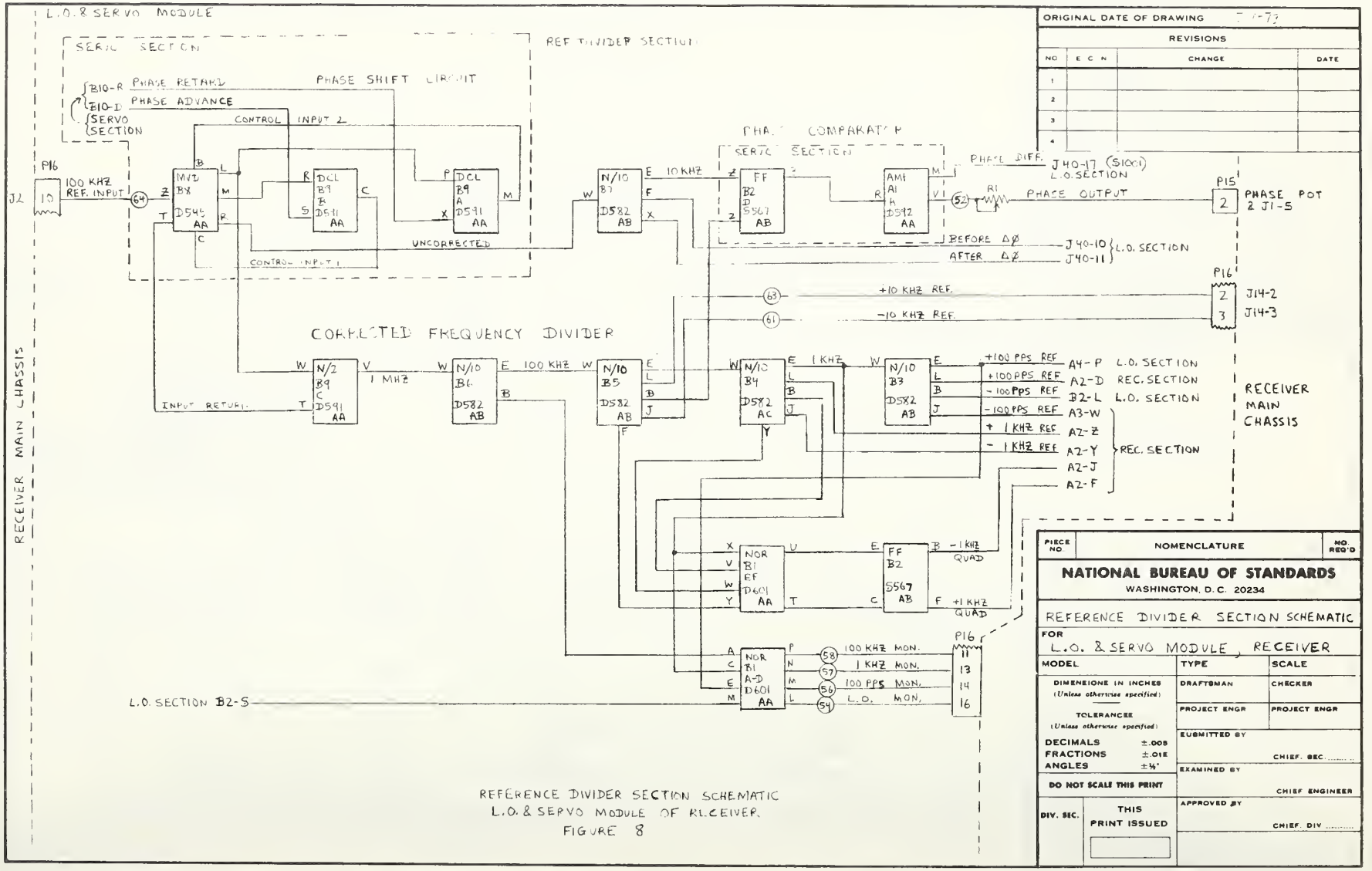

REFERENCE DIVIDER SECTION SCHEMATIC
L.O. & SERVO MODULE OF RECEIVER
FIGURE 8

ORIGINAL DATE OF DRAWING	7-7?

REVISIONS

NO	E C N	CHANGE	DATE
1			
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PIECE NO.	NOMENCLATURE	NO. REQ'D

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REFERENCE DIVIDER SECTION SCHEMATIC

FOR L.O. & SERVO MODULE, RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.01E ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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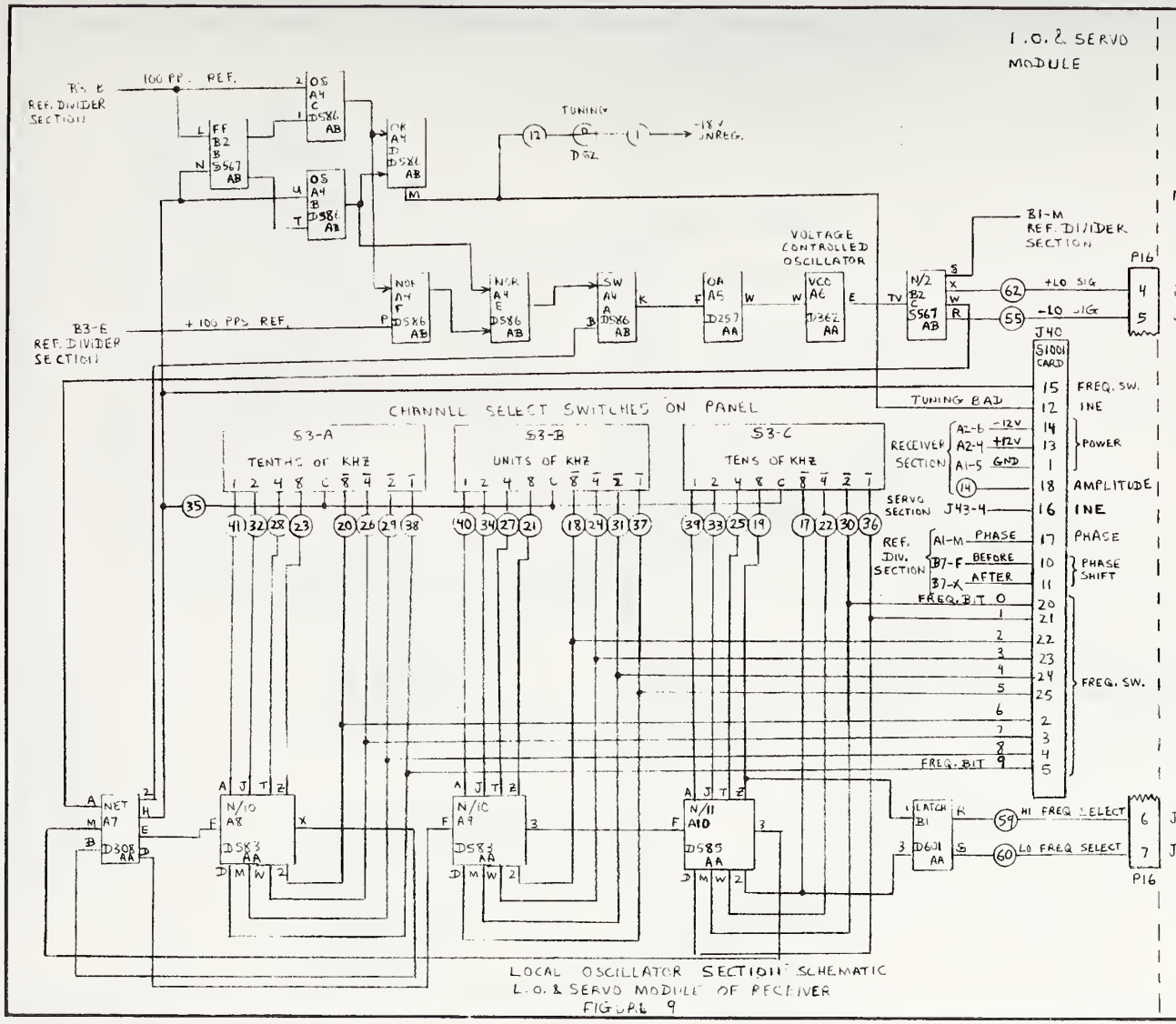

LOCAL OSCILLATOR SECTION SCHEMATIC
L.O. & SERVO MODULE OF RECEIVER
FIGURE 9

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
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4			

MAIN RECEIVER CHASSIS

PIECE NO.	NOMENCLATURE	NO REQ'D

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LOCAL OSC. SECTION SCHEMATIC
FOR
L.O. & SERVO MODULE, RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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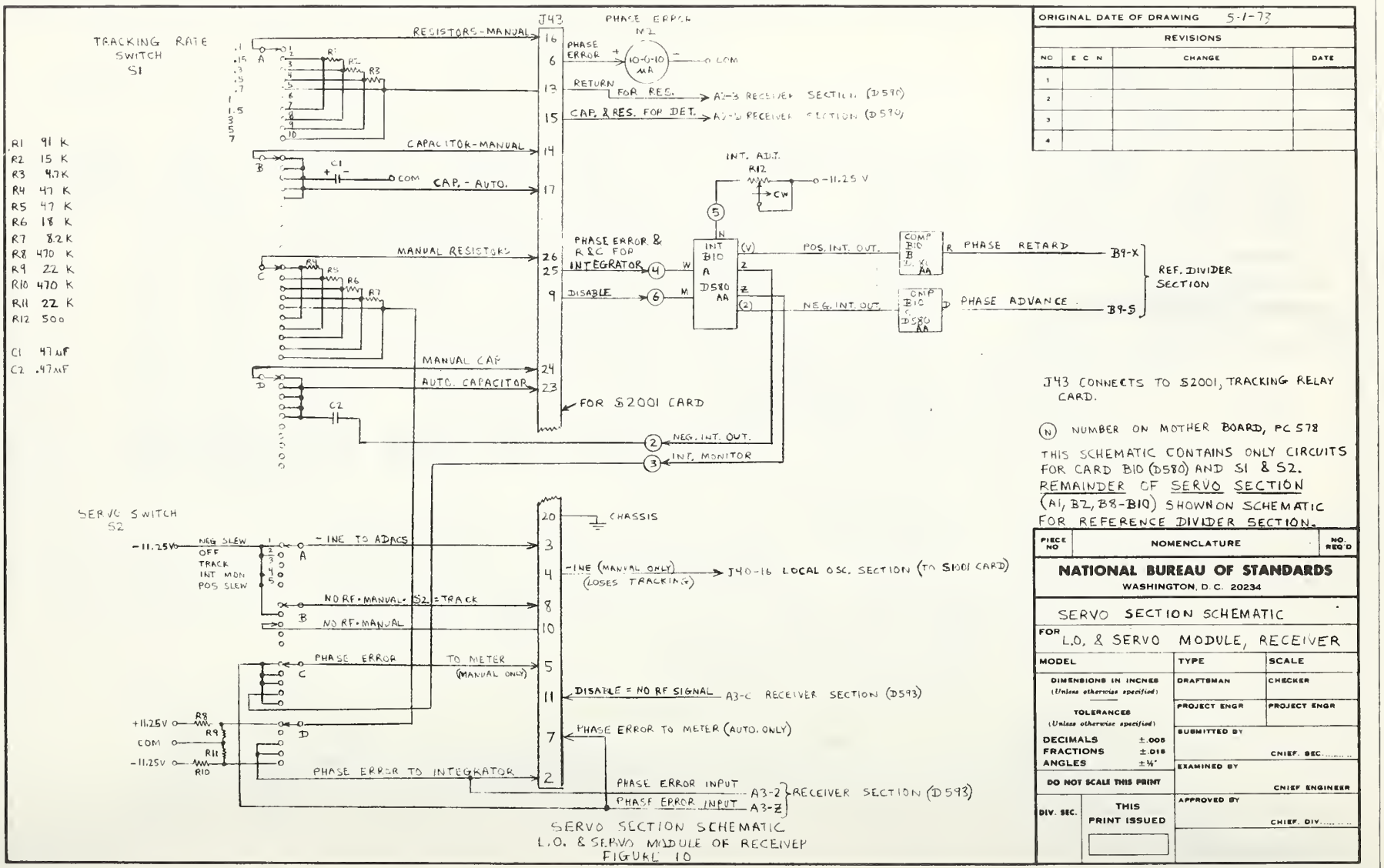

SERVO SECTION SCHEMATIC
L.O. & SERVO MODULE OF RECEIVER
FIGURE 10

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

J43 CONNECTS TO S2001, TRACKING RELAY CARD.

(N) NUMBER ON MOTHER BOARD, PC 578

THIS SCHEMATIC CONTAINS ONLY CIRCUITS FOR CARD B10 (D580) AND S1 & S2. REMAINDER OF SERVO SECTION (A1, B2, B8-B10) SHOWN ON SCHEMATIC FOR REFERENCE DIVIDER SECTION.

PIECE NO	NOMENCLATURE	NO. REQ'D

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SERVO SECTION SCHEMATIC

FOR L.O. & SERVO MODULE, RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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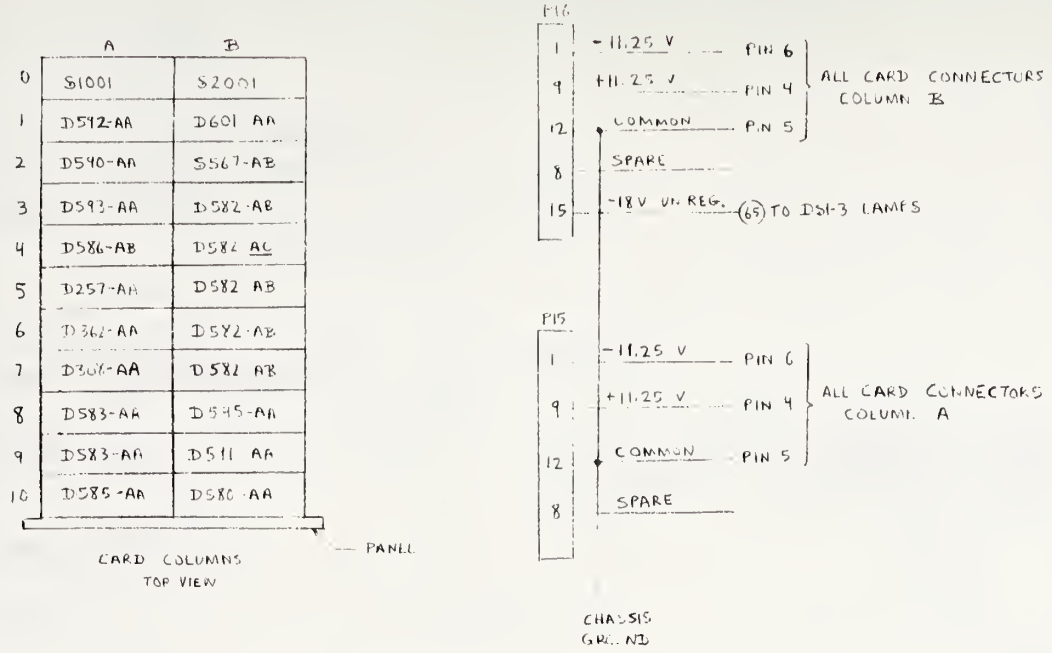

CARD LOCATIONS AND POWER CONNECTIONS
L.O. & SERVO MODULE OF RECEIVER
FIGURE 11

ORIGINAL DATE OF DRAWING 5-1-13			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO.	NOMENCLATURE	NO REQ'D

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POWER CONNECTIONS & CARD LOCATIONS
FOR L.O. & SERVO MODULE, RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC	
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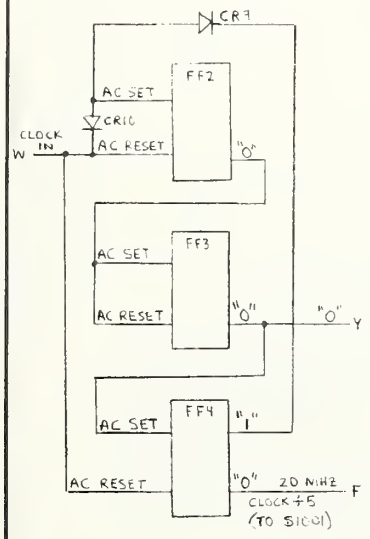
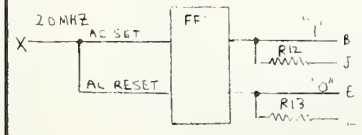
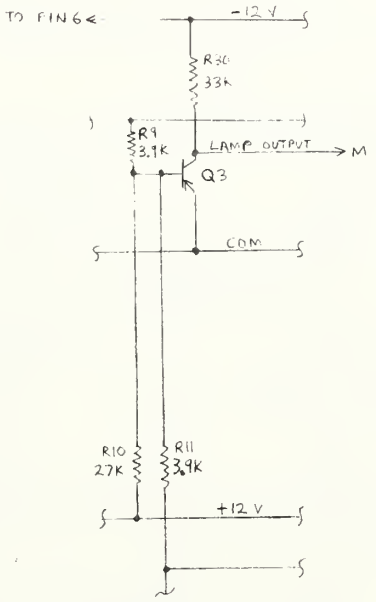
D582-AE CARD
RECEIVER SOCKET B ONLY
(CARD MARKED FOR B1 TO PREVENT USE IN OTHER LOCATIONS)





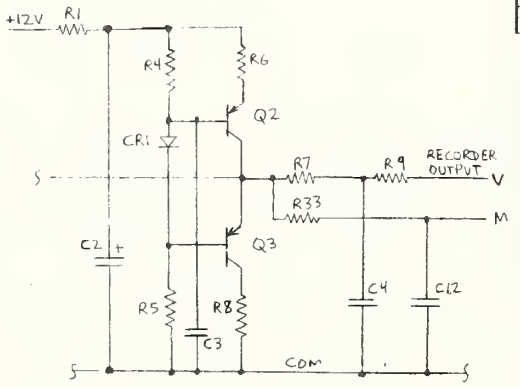
(FORMERLY, FF4 "0" WAS INTERNALLY JUMPERED TO FF1 AC SET/RESET.)

D586 AB CARD
RECEIVER SOCKET A4



(FORMERLY, SAME CIRCUIT BUT WITHOUT R33)

D592-AA CARD
RECEIVER SOCKET A1



(FORMERLY, SAME CIRCUIT BUT WITHOUT R33, C12 AND PIN M.)

ORIGINAL DATE OF DRAWING 5-1-72			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

THE CARD CIRCUITS SHOWN HAVE BEEN MODIFIED TO PERMIT COMPUTER CONTROL OF THE RECEIVER. SEE RECEIVER MANUAL FOR UNMODIFIED CIRCUITS ON CARDS.

CARD MODIFICATIONS IN RECEIVER
FIGURE 12

PIECE NO	NOMENCLATURE	NO. REQ'D

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CARD MODIFICATIONS

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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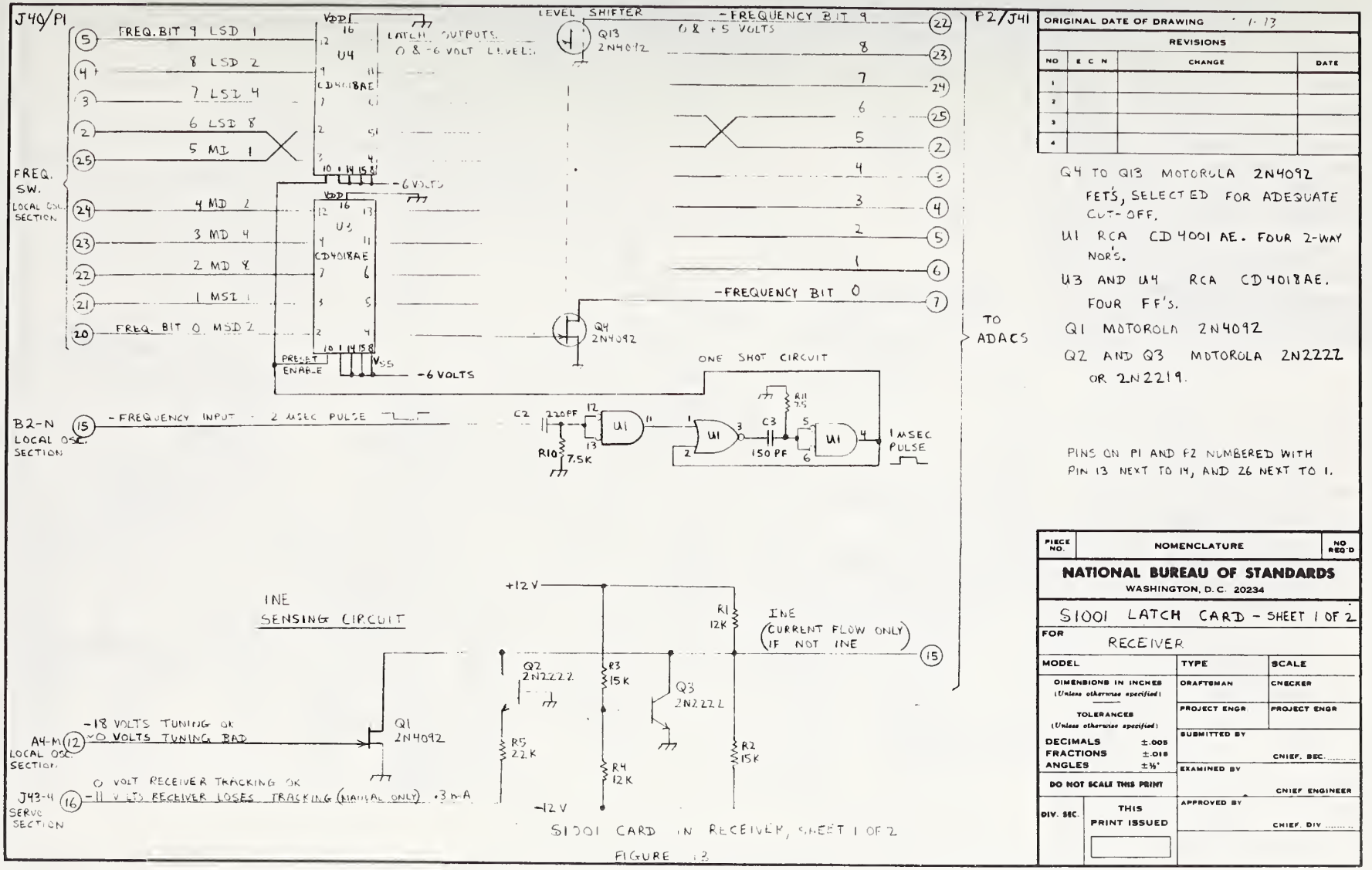

S1001 CARD IN RECEIVER, SHEET 1 OF 2

FIGURE 13

ORIGINAL DATE OF DRAWING	1-13

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

Q4 TO Q13 MOTOROLA 2N4092 FET'S, SELECTED FOR ADEQUATE CUT-OFF.

U1 RCA CD4001AE. FOUR 2-WAY NOR'S.

U3 AND U4 RCA CD4018AE. FOUR FF'S.

Q1 MOTOROLA 2N4092

Q2 AND Q3 MOTOROLA 2N2222 OR 2N2219.

PINS ON P1 AND P2 NUMBERED WITH PIN 13 NEXT TO 14, AND 26 NEXT TO 1.

PIECE NO.	NOMENCLATURE	NO REQ'D

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S1001 LATCH CARD - SHEET 1 OF 2

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY ..... CHIEF, SEC.	
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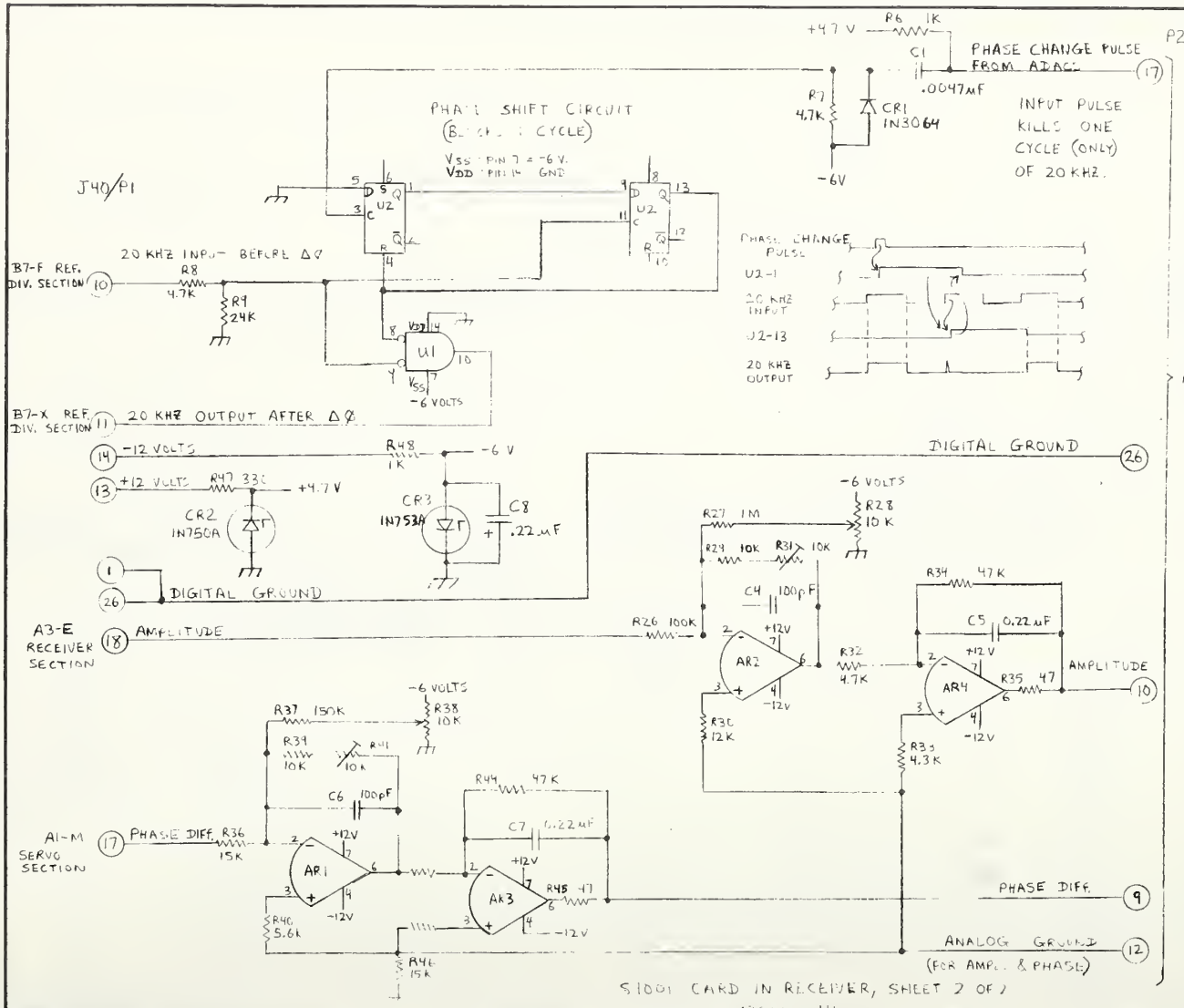

S1001 CARD IN RECEIVER, SHEET 2 OF 2

FIGURE 14

ORIGINAL DATE OF DRAWING			'73
REVISIONS			
NO.	E C N	CHANGE	DATE
1			
2			
3			
4			

U1 RCA CD4001AE, FOUR 2-WAY NOR'S.

U2 RCA CD4013AE, TWO D FF's.

AR1 THRU AR4 TEXAS INSTRUMENTS SN72741P 8-PIN INTEGRATED AMPLIFIER.

CR1 IN3064 SIGNAL DIODE

CR2 IN750A 4.7 VOLT 5% REGULATING DIODE

CR3 IN753A 6.2 VOLT 5% REGULATING DIODE

RESISTORS IN OHMS. FIXED RESISTORS ¼ WATT 2% OR 5%

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

S1001 LATCH CARD - SHEET 2 OF 2

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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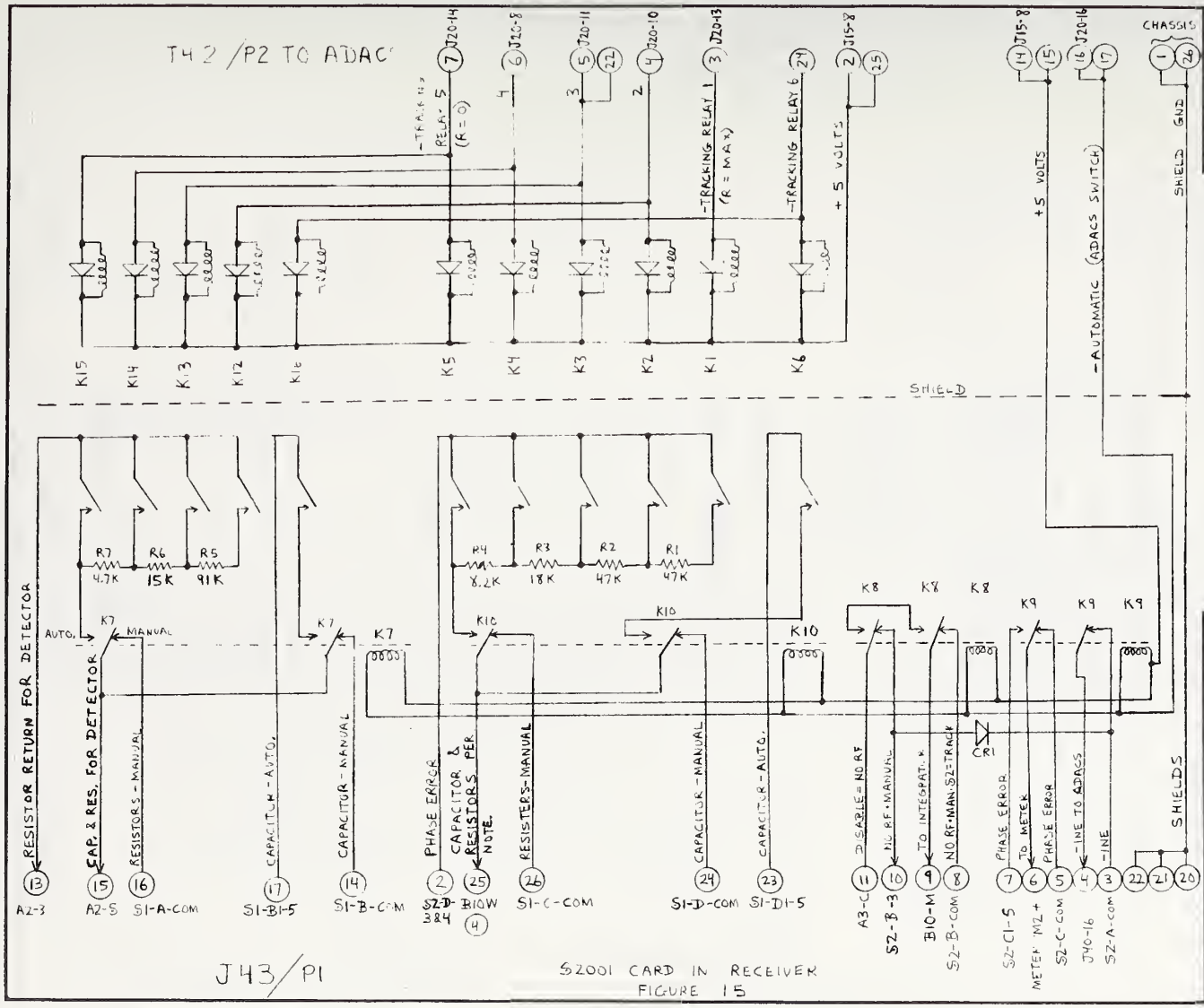

J43/P1

S2001 CARD IN RECEIVER
FIGURE 15

ORIGINAL DATE OF DRAWING 5-7-?

REVISIONS

NO	E C N	CHANGE	DATE
1			
4			
4			
4			

RELAYS K7-K10: OFF = MANUAL
ON = AUTOMATIC (COMPUTER CONTROL)

PIN 25 OF P1/J43 TO INTEGRATOR:
CAPACITOR IF MANUAL & S1-D1-5
OR AUTOMATIC & K6 ON.
RESISTOR IF MANUAL & S1-C1-5
OR AUTOMATIC & (K1+K2+K3+K4+K5)

K1-K6, K12-K16 SPST, NO, 10 mA RELAYS
GRIGSBY-BARTON GB-821A-4E

K7-K10 DPDT 140 OHMS RELAY
HATHAWAY 65627-4

ALL RESISTORS 1/4 WATT 5% OR 2%

CR1 IS IN3064

P1 AMP 85931-6

P2 AMP 85931-6

PINS NUMBERED WITH PIN 13 NEXT 14, AND PIN 26 NEXT 1.

PIECE NO.	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

S2001 TRACKING RATE CARD

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR.
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
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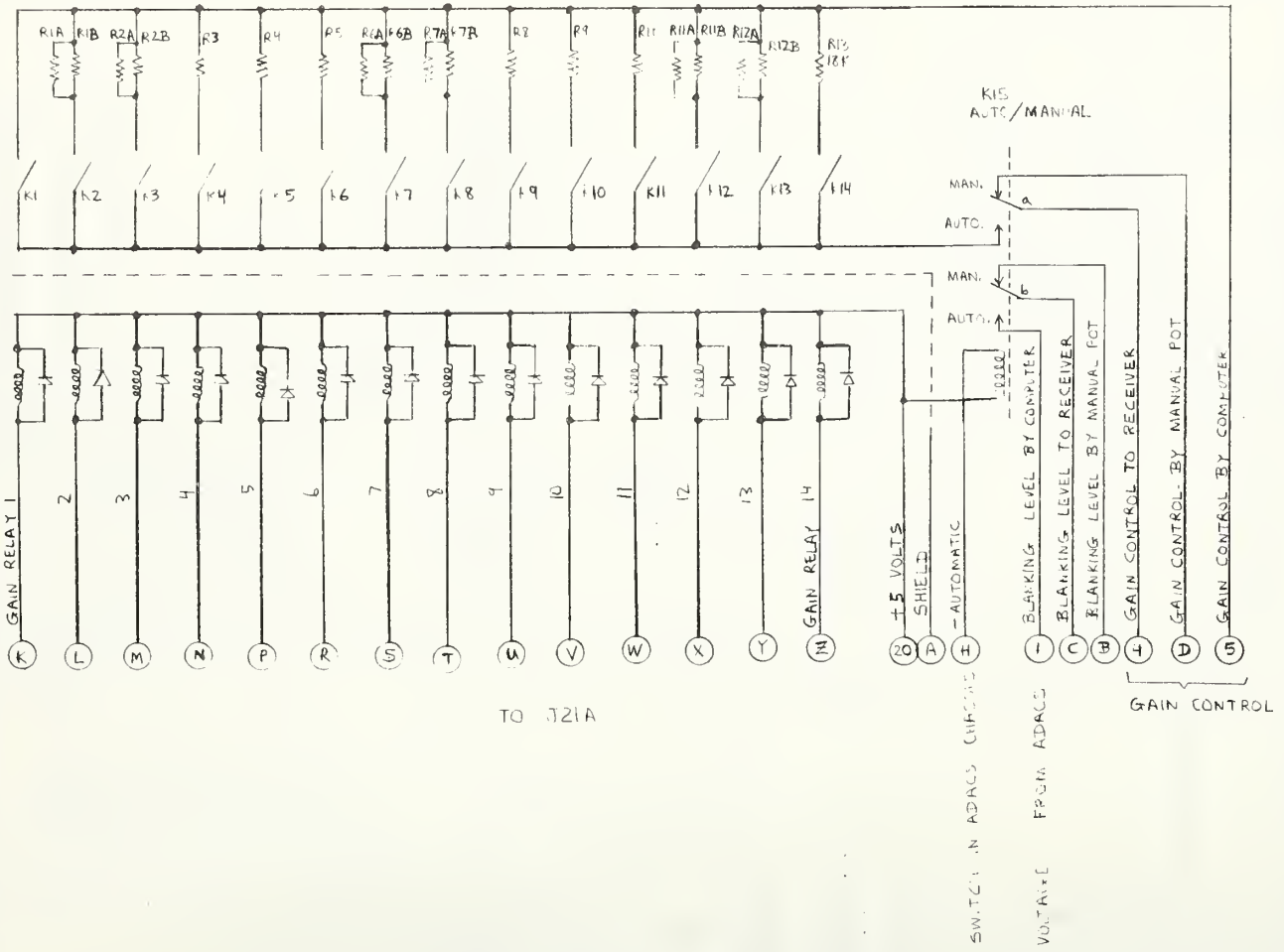

S3001 CARD IN RECEIVER

FIGURE 16

ORIGINAL DATE OF DRAWING	

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

RESISTANCE IN OHMS

R1A	2.7	R8	560.
R1B	12.	R9	1100.
R2A	13.	R10	2200.
R2B	13.	R11A	4700.
R3	16.	R11B	110K
R4	33.	R12A	18K
R5	68.	R12B	18K
R6A	150.	R13	18K
R6B	1800.		
R7A	300.		
R7B	4300.		

ALL RESISTORS $\frac{1}{4}$ WATT 5% OR 2% EXCEPT R1A WHICH IS $\frac{1}{2}$ WATT

K1 TO K14 SPST NO 10 mA RELAYS
GRIGSBY-BARTON GB 821A-4E

K15 DPDT 140 OHMS RELAY
HATHAWAY 65627-4

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D. C. 20234

S3001 GAIN CONTROL CARD

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.008 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC
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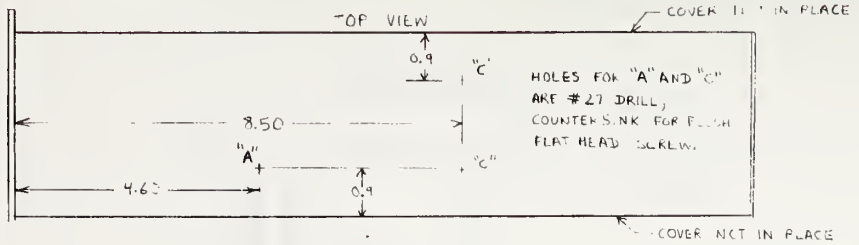
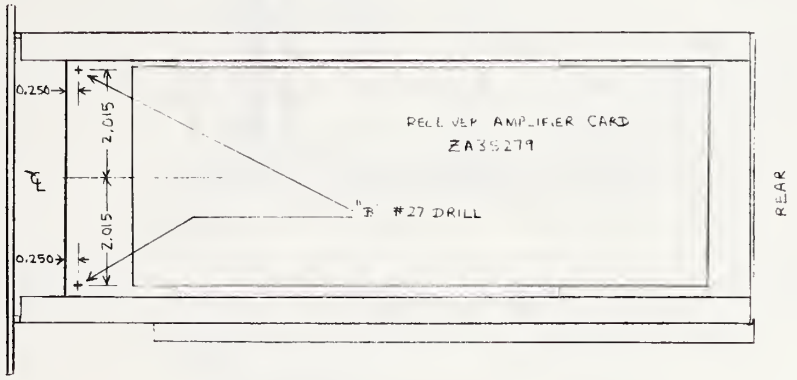
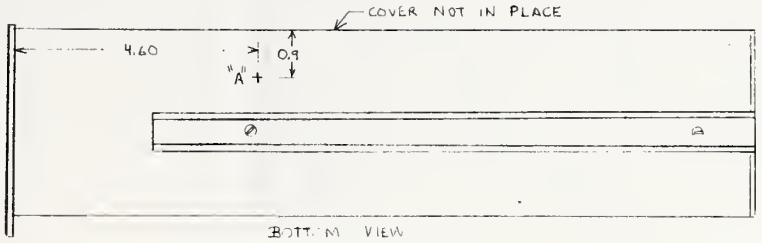
NBS 348

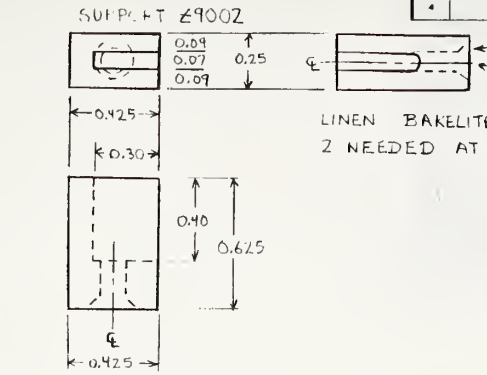
RF-IF AMPLIFIER MODULE







DIMENSIONS ARE AT REAR OF PANEL



MOUNTING HARDWARE FOR S3001 CARD IN RECEIVER

FIGURE 17

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

S3001 CARD, MOUNTING HARDWARE

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.015 ~~.0000~~	SUBMITTED BY	
FRACTIONS ±.018		CHIEF, SEC.
ANGLES ±½°	EXAMINED BY	
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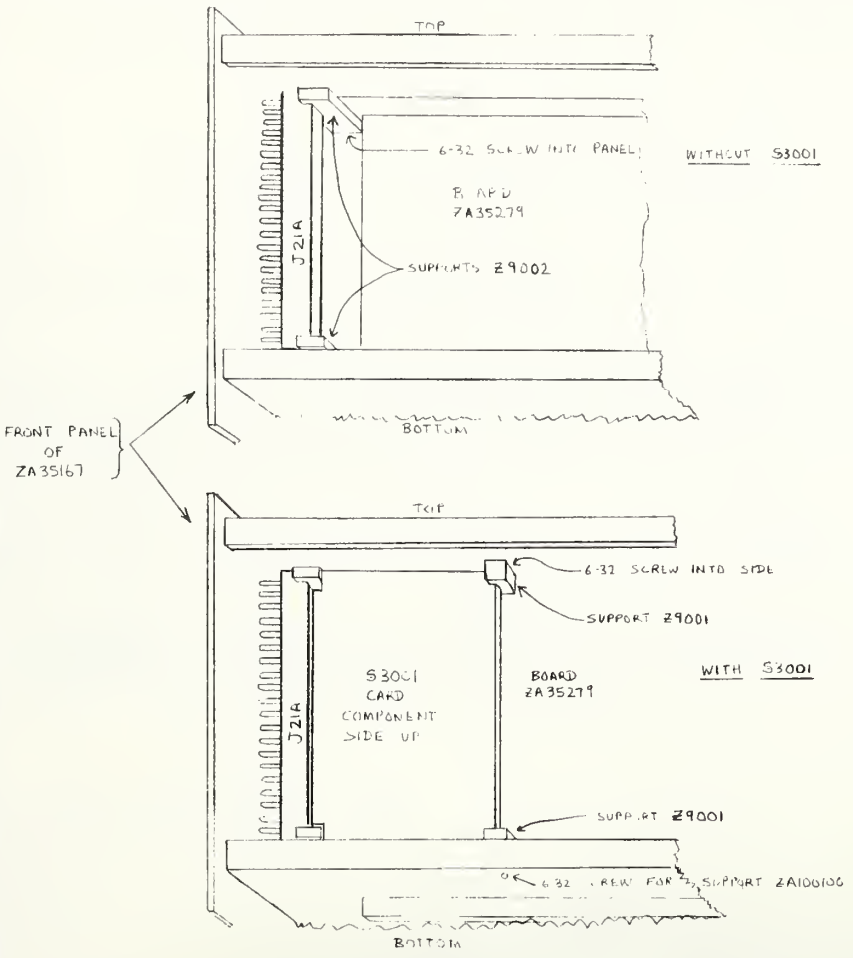
U.S. GOVERNMENT PRINTING OFFICE 1964—O-717-709

NBS 348

RF-IF AMPLIFIER MODULE



MECHANICAL MOUNTING OF S3001 CARD IN RECEIVER

FIGURE 18

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

ASSEMBLY OF S3001 CARD INTO RECEIVER'S RF-IF AMPLIFIER MODULE USING TWO Z9001 AND TWO Z9002 SUPPORTS.

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D. C. 20234

S3001 CARD, MECHANICAL MOUNTING

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.008 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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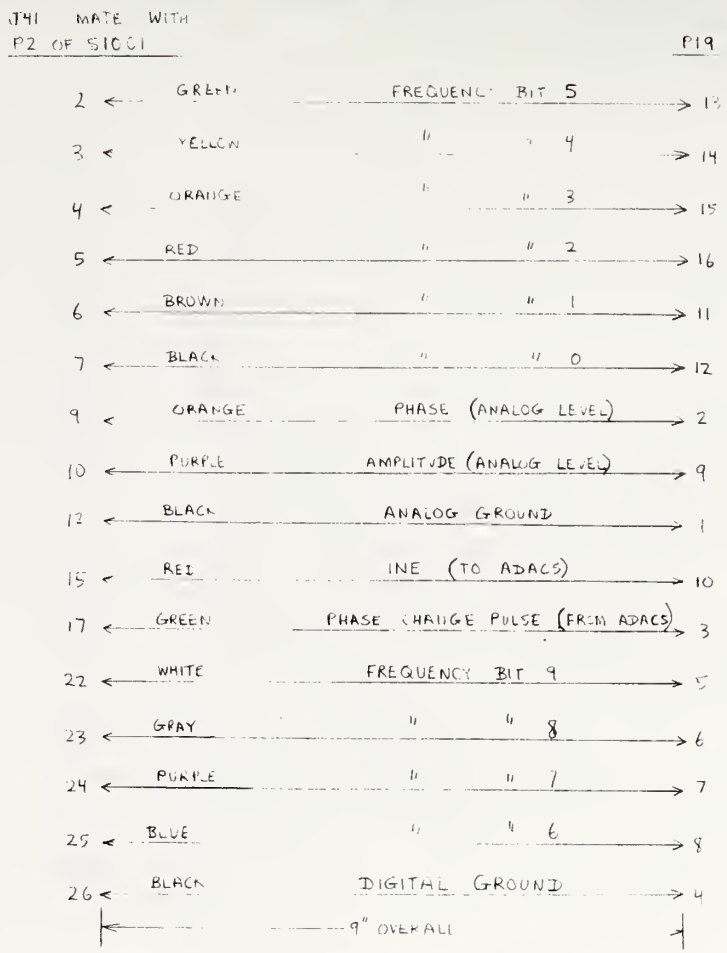

CABLE W1002 IN RECEIVER
FIGURE 21

ORIGINAL DATE OF DRAWING 5-72				
REVISIONS				
NO	E C N		CHANGE	DATE
4				
4				
4				
4				

KEYS IN PINS 1 AND 13 OF J41

#26 WIRE, STRANDED, TEFLON INSULATED

J41 BLOCK — AMP # 86148-4
CONTACTS — AMP # 86015-1
KEYING PIN — AMP # 86286-1

PIECE NO.	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

CABLE W1002 — J41 (S1001) TO P19

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ± .005	SUBMITTED BY	CHIEF, SEC.
FRACTIONS ± 1/16		
ANGLES ± 1/2°	EXAMINED BY	CHIEF ENGINEER
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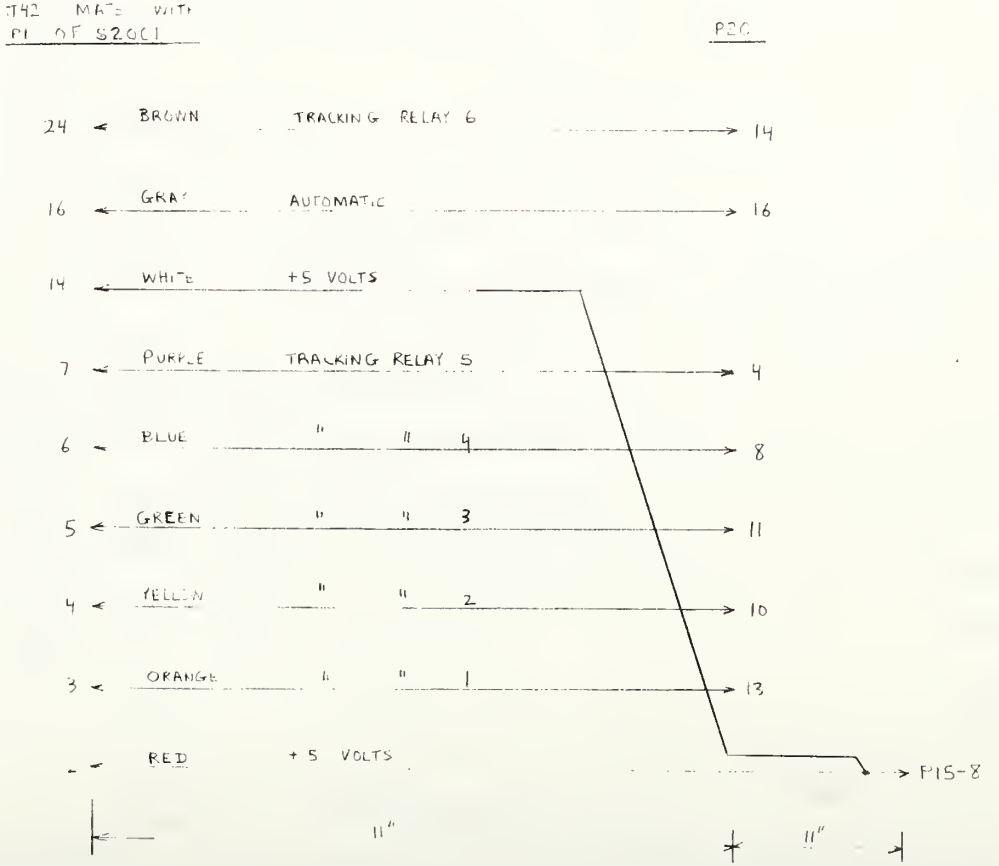
ORIGINAL DATE OF DRAWING 2-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

KEYS IN PINS 9, 18, 20, 21, 23 OF J42



CABLE W2001 IN RECEIVER

FIGURE 22

PIECE NO.	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

CABLE W2001-J42(S2001) TO P20

FOR RECEIVER

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.018 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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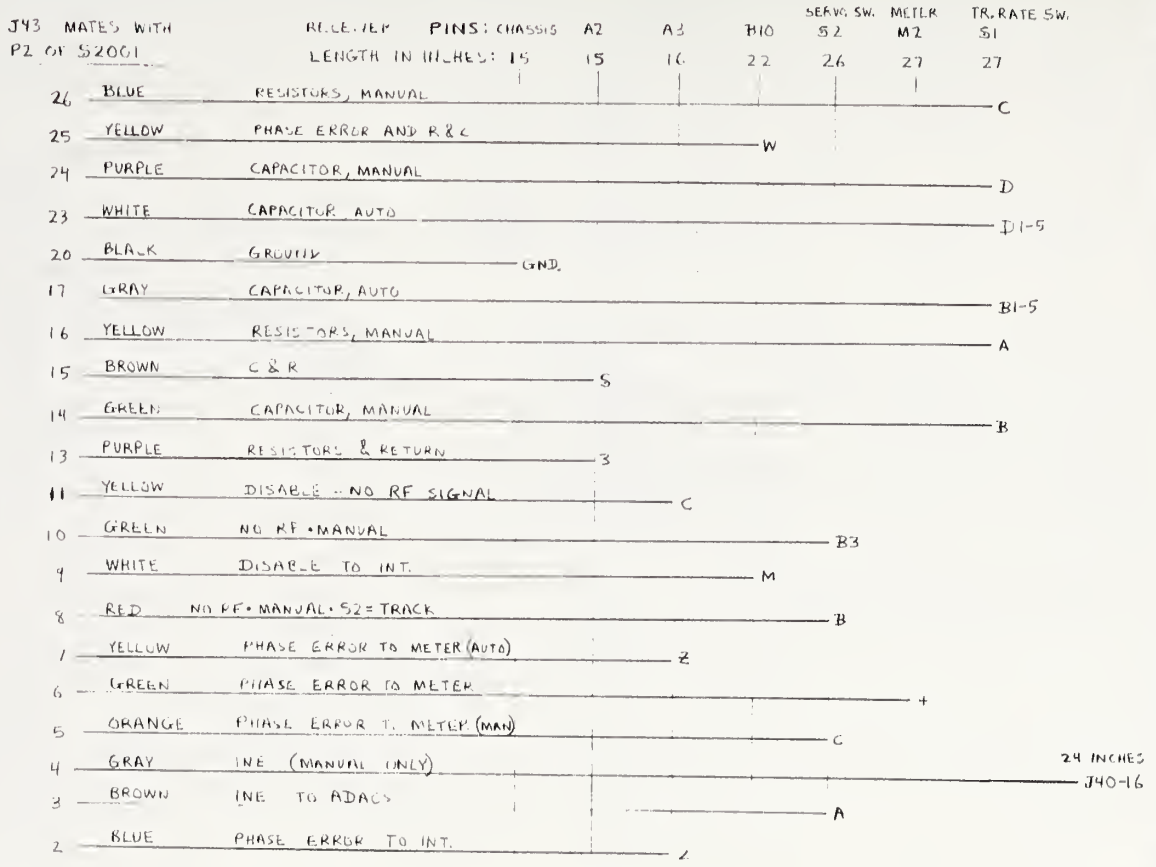
NBS 548

ORIGINAL DATE OF DRAWING 5-1-72			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

KEYS IN PINS 1 AND 12 OF J43



CABLE W2002 IN RECEIVER

FIGURE 23

PIECE NO	NOMENCLATURE	NO. REQ'D
	NATIONAL BUREAU OF STANDARDS WASHINGTON, D. C. 20234	
	CABLE W2002 - J43 (S2001) TO CARDS	
	FOR RECEIVER	

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.00E FRACTIONS ±.01E ANGLES ±½°	SUBMITTED BY	CHIEF, SEC
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RECEIVER J32 PIN #	WIRE COLOR	ADACS J1 PIN #	DESCRIPTION
A	WHITE-BROWN	A	TRACKING RATE RELAY 1
B	WHITE-BLACK-GREEN	B	" " " 2
C	WHITE-BLACK-YELLOW	C	" " " 3
D	WHITE-BLACK-ORANGE	D	" " " 4
E	WHITE	E	" " " 5
F	WHITE-BLUE	F	" " " 6
H	YELLOW	H	GAIN RELAY 1
J	BLACK	J	" " 2
K	RED	K	" " 3
L	WHITE-VIOLET	L	" " 4
M	WHITE-ORANGE	M	" " 5
N	WHITE-GRAY	N	" " 6
P	WHITE-GREEN	P	" " 7
R	WHITE-YELLOW	R	" " 8
S	VIOLET	S	" " 9
T	BLUE	T	" " 10
U	GREEN	U	" " 11
V	WHITE-BROWN-BLACK	V	" " 12
W	WHITE-RED	W	" " 13
X	GRAY	X	" " 14
Y	ORANGE	Y	PHASE CHANGE PULSE
Z	WHITE-VIOLET-BLACK	Z	MAINT./NORMAL
a	WHITE-BLACK	a	AUTO./MANUAL
b	WHITE-BLACK-RED	b	+5 VOLTS
c	SHIELD	c	DIGITAL GROUND
d	WHITE-BLACK-GRAY	d	——
e	BROWN	e	——
f	WHITE-BLUE-BLACK	f	——

RECEIVER J31 PIN #	WIRE COLOR	ADACS J3 PIN #	DESCRIPTION
A	BLUE-BLACK	A	FREQUENCY BIT 0
B	BLUE-RED	B	" " 1
C	RED-GREEN	C	" " 2
D	GREEN	D	" " 3
E	BLACK-WHITE	E	" " 4
F	WHITE	F	" " 5
H	ORANGE-BLACK	H	" " 6
J	RED	J	" " 7
K	ORANGE	K	" " 8
L	ORANGE-RED	L	" " 9
M	RED-WHITE	M	LINE
N	SHIELD	N	DIGITAL GROUND
P	WHITE-BLACK	P	——
R	BLUE	R	——
S	WHITE-RED	S	——
T	GREEN-BLACK	T	——
U	RED-BLACK	U	——
V	BLUE-WHITE	V	——
W	GREEN-WHITE	W	——
X	SHIELD	X	DIGITAL GROUND

SOLDER TWO WIRES TO SHIELD

ADACS J4 PIN #	CARDIOID	DESCRIPTION
A	H	CARDIOID BIT 10
B	A	" " 11
D	B	" " 12
E	D	GROUND
H	E	+5 VOLTS

RECEIVER	ADACS	DESCRIPTION	COAX
J6	J6	BLANKING PULSES (FROM RECEIVER)	
J27	J8	BLANKING LEVEL (FROM ADACS)	

RECEIVER	COMPUTER	DESCRIPTION	COAX
J26	—	PHASE	
J31		AMPLITUDE (AGC)	

SYSTEM CABLES
FIGURE 24

ORIGINAL DATE OF DRAWING 5-73

REVISIONS

NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D. C. 20234

CABLES: RECEIVER TO ADACS; MISC.

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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ADACS J5 PIN #	WIRE COLOR	CPU PIN #	BIT NUMBER	DESCRIPTION
A	BLUE-BLACK	A	0	FREQUENCY BIT 0*
B	BLUE-RED	B	1	" " 1
C	RED-GREEN	C	2	" " 2
D	GREEN	D	3	" " 3
E	BLACK-WHITE	E	4	" " 4
F	WHITE	F	5	" " 5
H	ORANGE-BLACK	H	6	" " 6
J	RED	J	7	" " 7
K	ORANGE	K	8	" " 8
L	ORANGE-RED	L	9	" " 9
M	RED-WHITE	M	10	CARDINAL 2^0
N	RED-BLACK	N	11	" 2^1
P	WHITE-BLACK	P	12	" 2^2
R	BLUE	R	13	LINE
S	WHITE-RED	S	14	MAINT./NORMAL
T	GREEN-BLACK	T	15	AUTO./MANUAL
U	BLACK-SHIELD	U		GROUND
V	BLUE-WHITE	V		—
W	GREEN-WHITE	W		—
X	BLACK-SHIELD	X	COMMON	GROUND

*MOST SIG. BIT

ADACS J2 PIN #	WIRE COLOR	CPU PIN #	BIT NUMBER	DESCRIPTION
A	BLUE-BLACK	A	3	TRACKING RATE
B	BLUE-RED	B	2	" "
C	RED-GREEN	C	1	" "
D	GREEN	D	0	" "
E	BLACK-WHITE	E	4	RF GAIN
F	WHITE	F	3	" "
H	ORANGE-BLACK	H	2	" "
J	RED	J	1	" "
K	ORANGE	K	0	" "
L	ORANGE-RED	L	5	BLANKING LEVEL
M	RED-WHITE	M	4	" "
N	RED-BLACK	N	3	" "
P	WHITE-BLACK	P	2	" "
R	BLUE	R	1	" "
S	WHITE-RED	S	0	" "
T	GREEN-BLACK	T	—	PHASE CHANGE BIT
U	COAX	W		FLAG PULSE
V	GREEN-WHITE	U		—
W	SHIELD	V		—
X	SHIELD	X		GROUND

SOLDER TWO BLACK WIRES TO SHIELD.

ADACS	COAX TO:	DESCRIPTION
J7	COMPUTER	PERCENT BLANKING
J9	COMPUTER/ADACS N+1	LINE INTERRUPT
J10	ADACS N-1	LINE INTERRUPT

SYSTEM CABLES
FIGURE 25

ORIGINAL DATE OF DRAWING 5/73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

CABLES FOR ADACS TO COMPUTER

FOR

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.00E FRACTIONS ±.01S ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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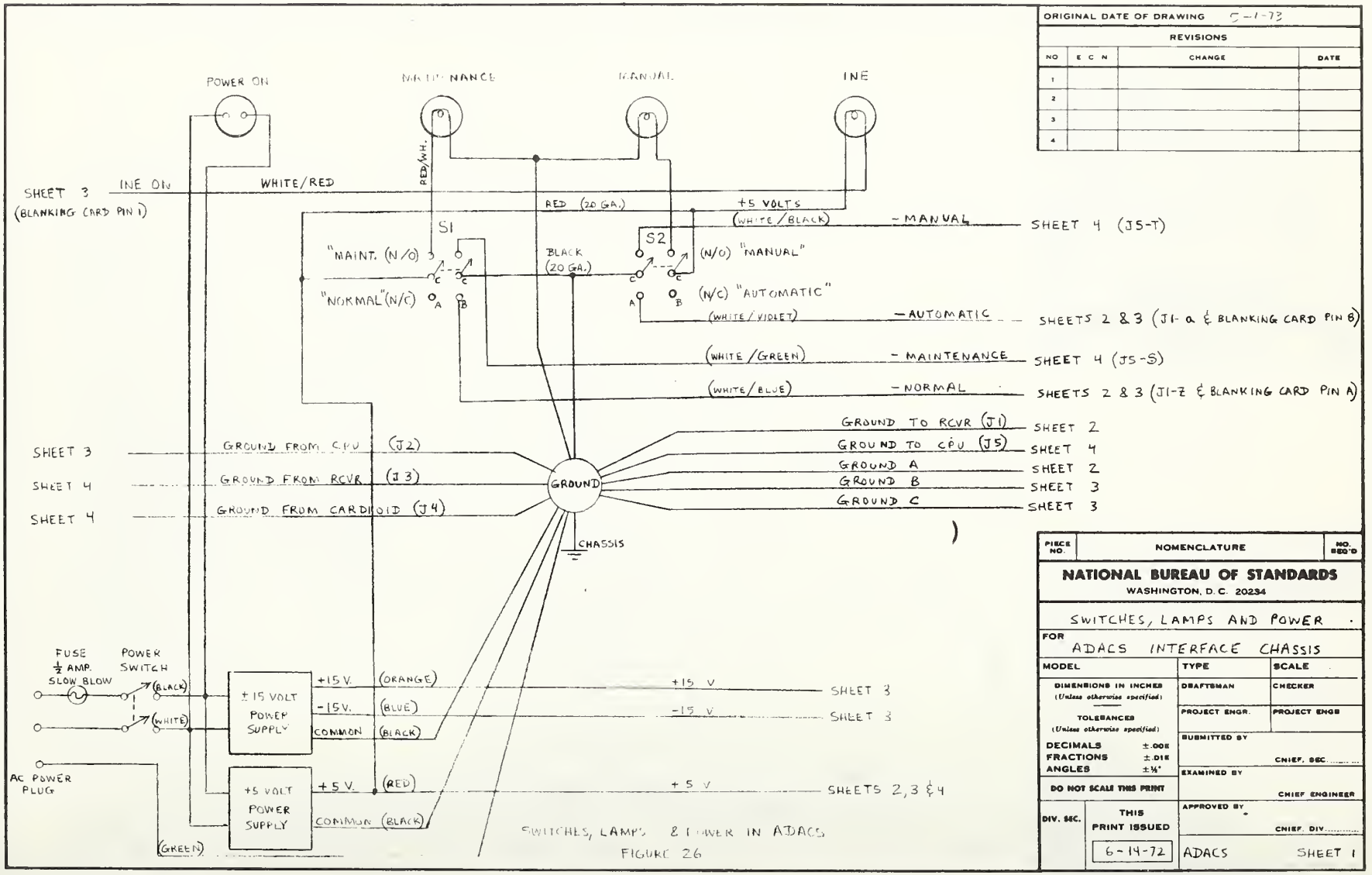

SWITCHES, LAMPS & POWER IN ADACS

FIGURE 26

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D. C. 20234

SWITCHES, LAMPS AND POWER

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.00E FRACTIONS ±.01E ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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NO. 413-2301-ADACS-1

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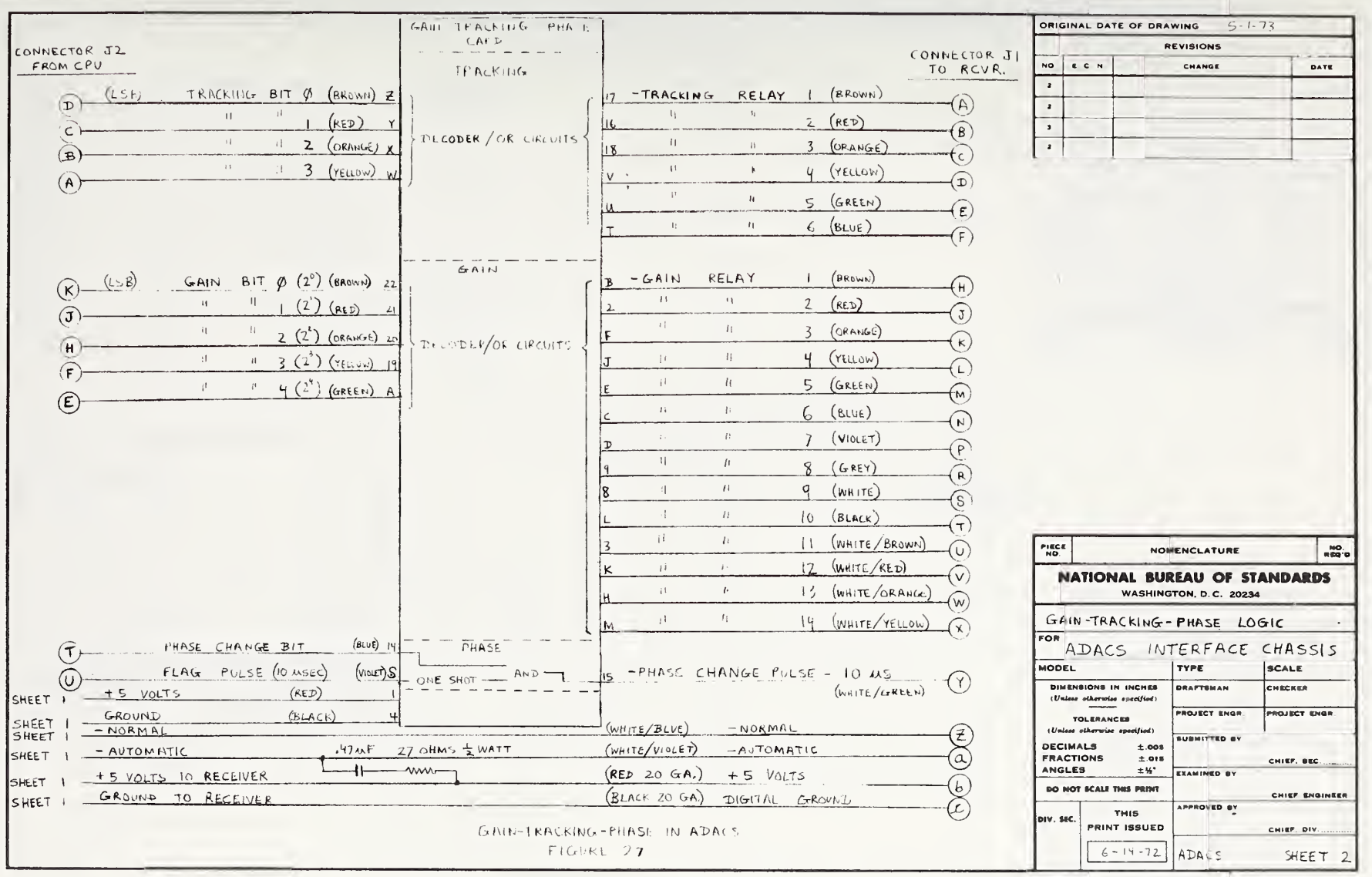
NBS 348



GAIN-TRACKING-PHASE IN ADACS
FIGURE 27

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
2			
2			
3			
2			

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

GAIN-TRACKING-PHASE LOGIC

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
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	ADACS	SHEET 2

DRAWING NO. 413-2301-ADACS-1

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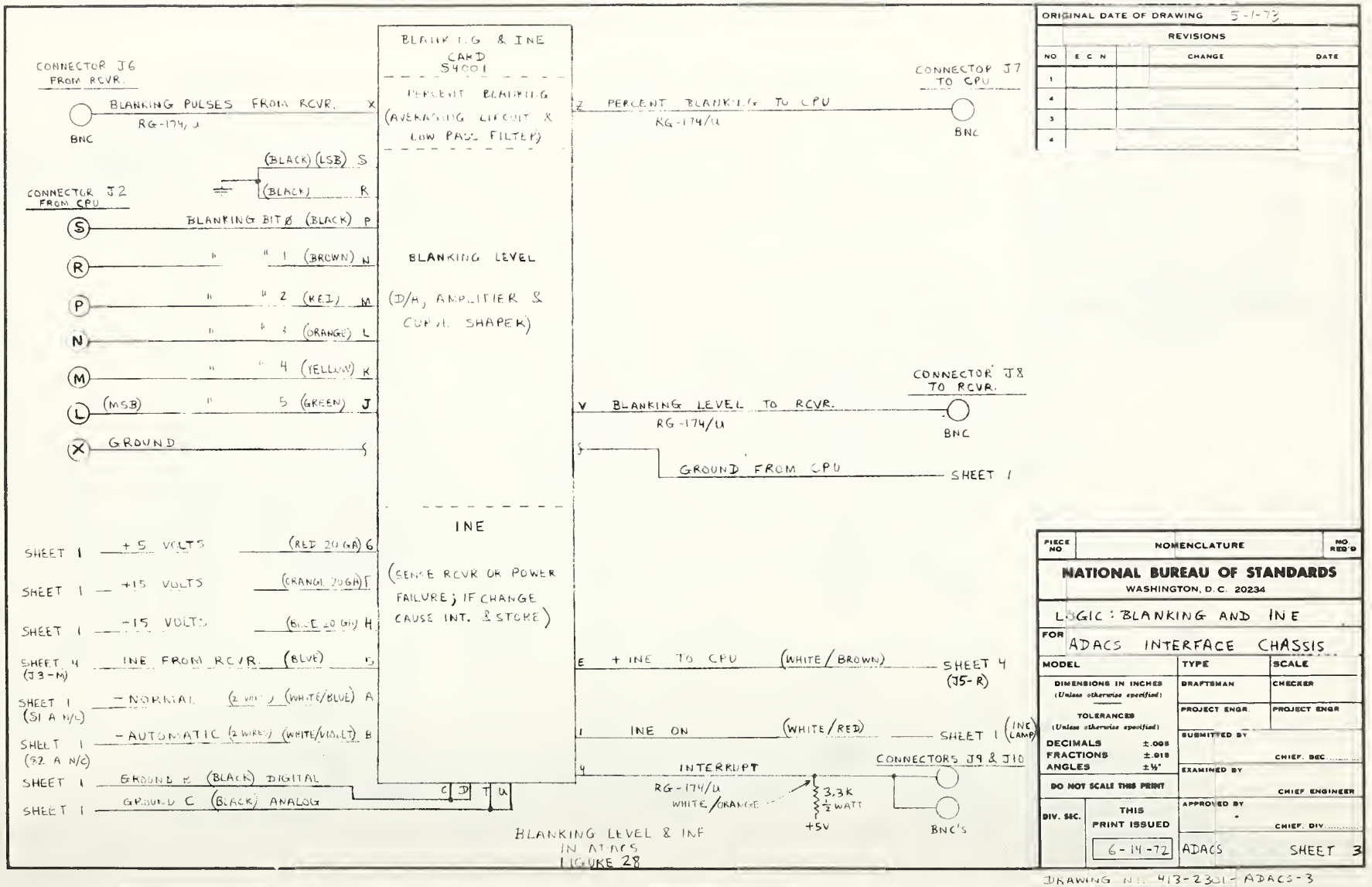


BLANKING LEVEL & INE IN ADACS
FIGURE 28

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

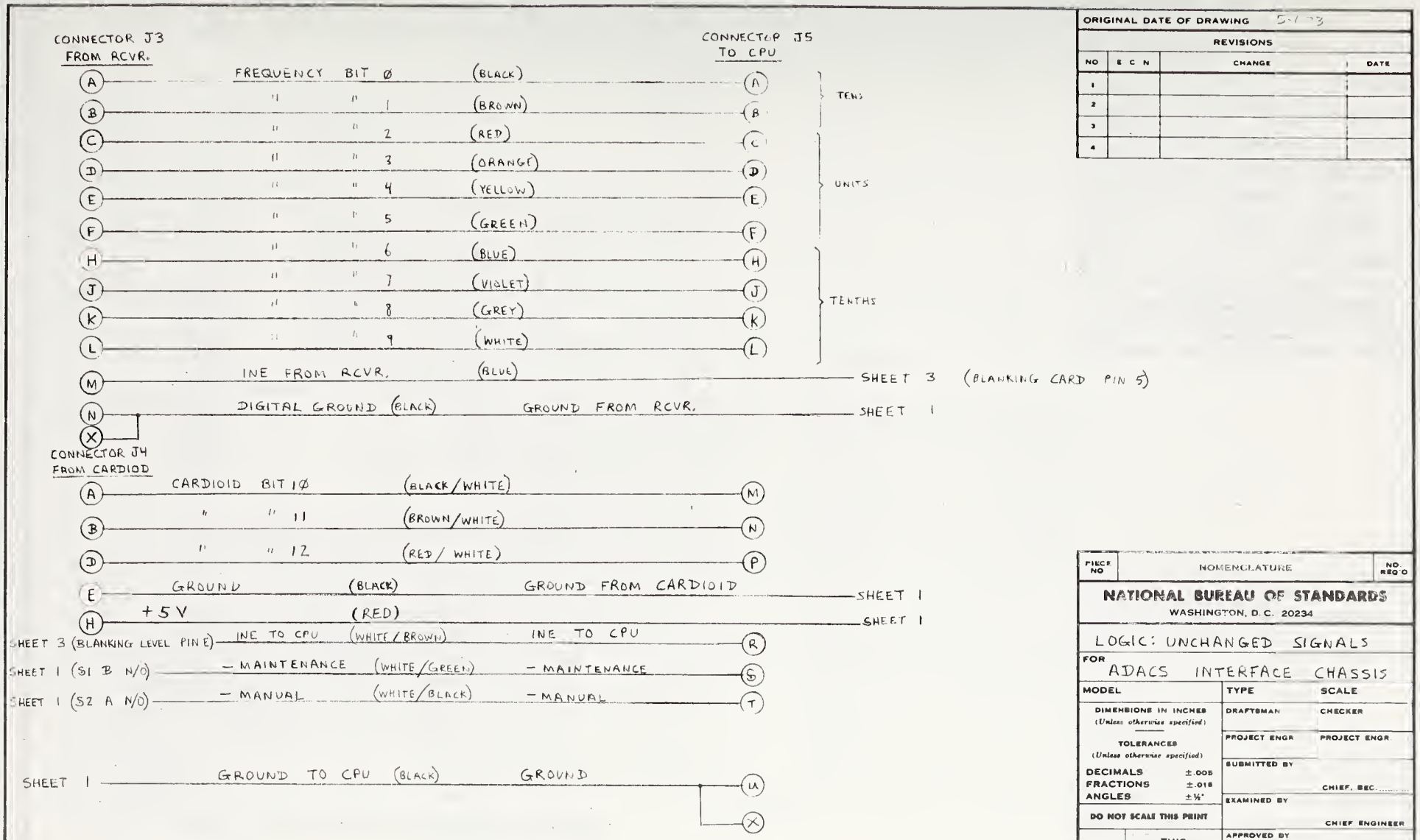
LOGIC: BLANKING AND INE

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF, SEC	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC. THIS PRINT ISSUED 6-14-72	APPROVED BY CHIEF, DIV.	
	ADACS SHEET 3	

DRAWING NO. 413-2301-ADACS-3

U.S. GOVERNMENT PRINTING OFFICE 1964—O-717-709



UNCHANGED LINES PASSED THROUGH ADACS

FIGURE 29.

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

LOGIC: UNCHANGED SIGNALS
FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY CHIEF, SEC.	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
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ADACS SHEET 4

DRAWING NO. 413-2301-ADACS-4

U.S. GOVERNMENT PRINTING OFFICE 1964—O-717-700

TRACKING

STEP	CODE	RELAYS	TRACKING
1	0000	1 & 6	0.1
2	0001	2 & 6	0.15
3	0010	3 & 6	0.3
4	0011	4 & 6	0.5
5	0100	5 & 6	0.7
6	0101	1	1.0
7	0110	2	1.5
8	0111	3	3.0
9	1000	4	5.0
10	1001	5	7.0

GAIN

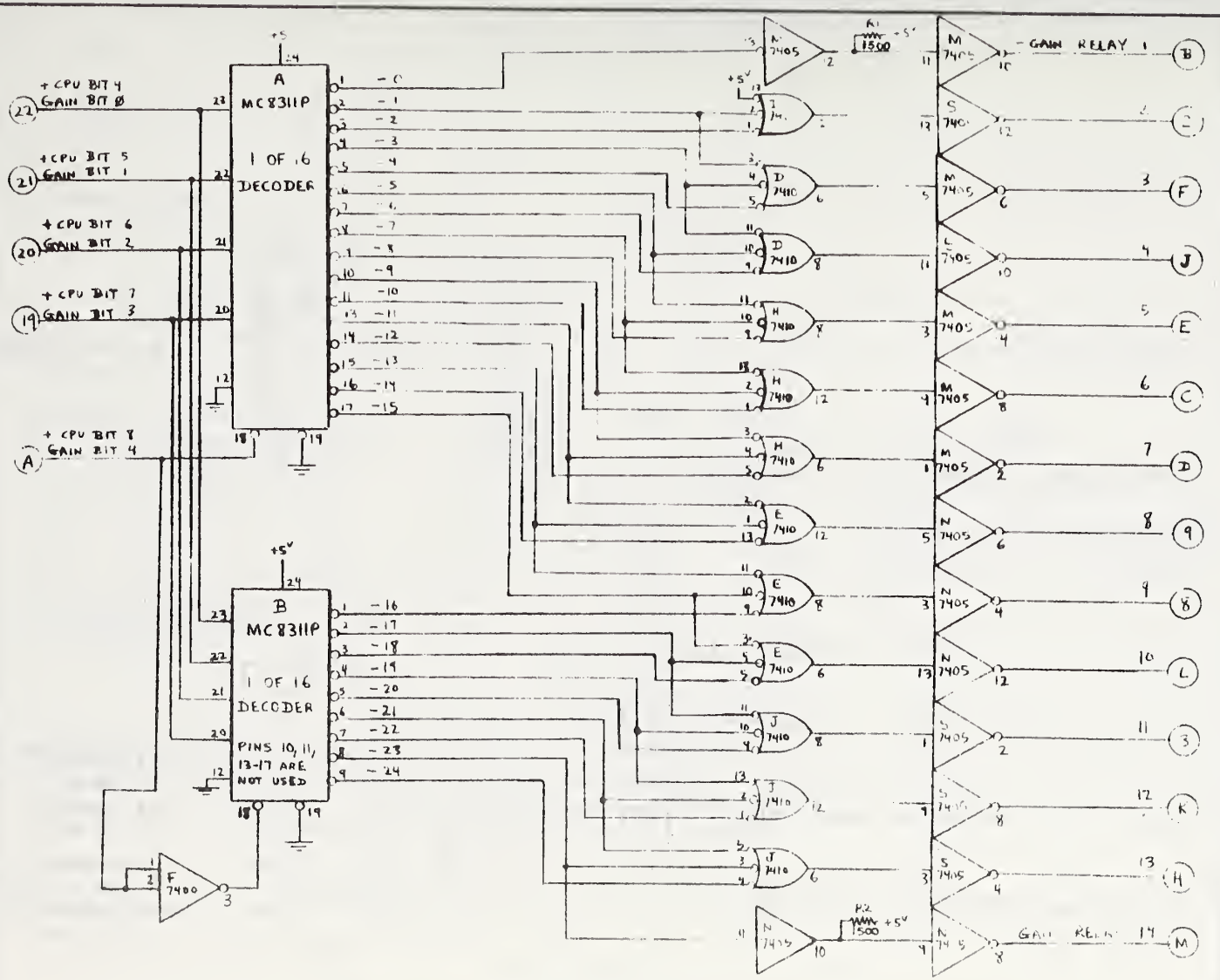
STEP	CODE	RELAYS	dB GAIN
1	00000	1	0
2	00001	2 & 3	5.
3	00010	2	6.
4	00011	3 & 4	11.
5	00100	3	12.
6	00101	4 & 5	15.
7	00110	4	18.
8	00111	5 & 6	21
9	01000	5	24
10	01001	6 & 7	27.
11	01010	6	30.
12	01011	7 & 8	33.
13	01100	7	36.
14	01101	8 & 9	39.
15	01110	8	42.
16	01111	9 & 10	45.
17	10000	9	48
18	10001	10 & 11	51.
19	10010	10	54.
20	10011	11 & 12	57.
21	10100	11	60.
22	10101	12 & 13	63.
23	10110	12	66.
24	10111	13 & 14	69.
25	11000	13	72.

TRACKING AND GAIN CHART
ADACS
FIGURE

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO. REQ'D
NATIONAL BUREAU OF STANDARDS WASHINGTON, D.C. 20234		
LOGIC TRACKING AND GAIN CHART		
FOR ADACS INTERFACE CHASSIS		
MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified) TOLERANCES (Unless otherwise specified) DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	DRAFTSMAN	CHECKED
	PROJECT ENGR	PROJECT ENGR
	SUBMITTED BY CHIEF SEC.	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED 6-14-72	APPROVED BY CHIEF DIV.
		ADACS SHEET 5

DRAWING NO. 413-23 ALA-5



GAIN TRACKING-PHASE CARD IN ADACS
SHEET 1 OF 2
FIGURE 31

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

GAIN-TRACKING-PHASE CARD 1 OF 2

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF SEC	
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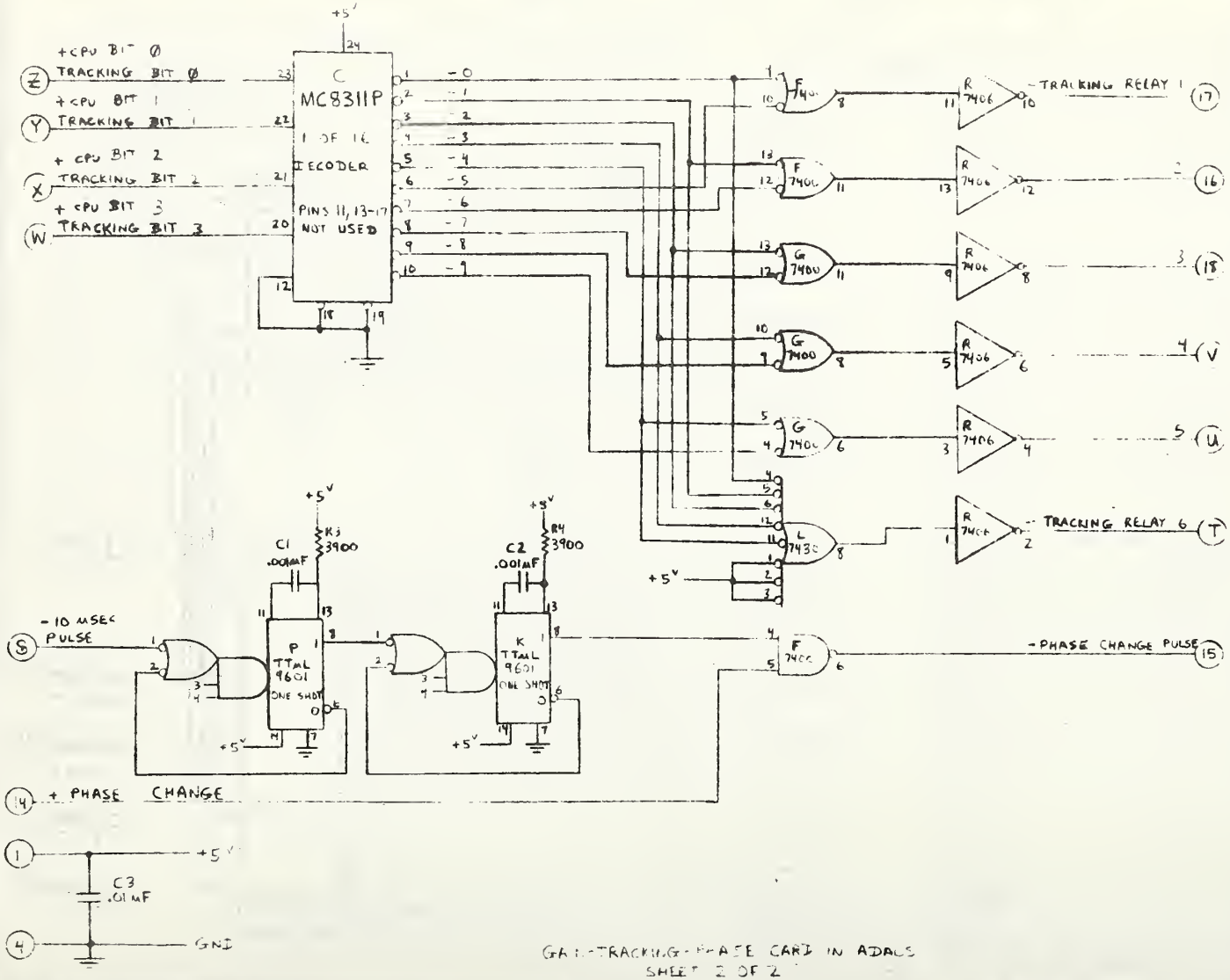


GAIN-TRACKING-PHASE CARD IN ADACS
SHEET 2 OF 2
FIGURE 32

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

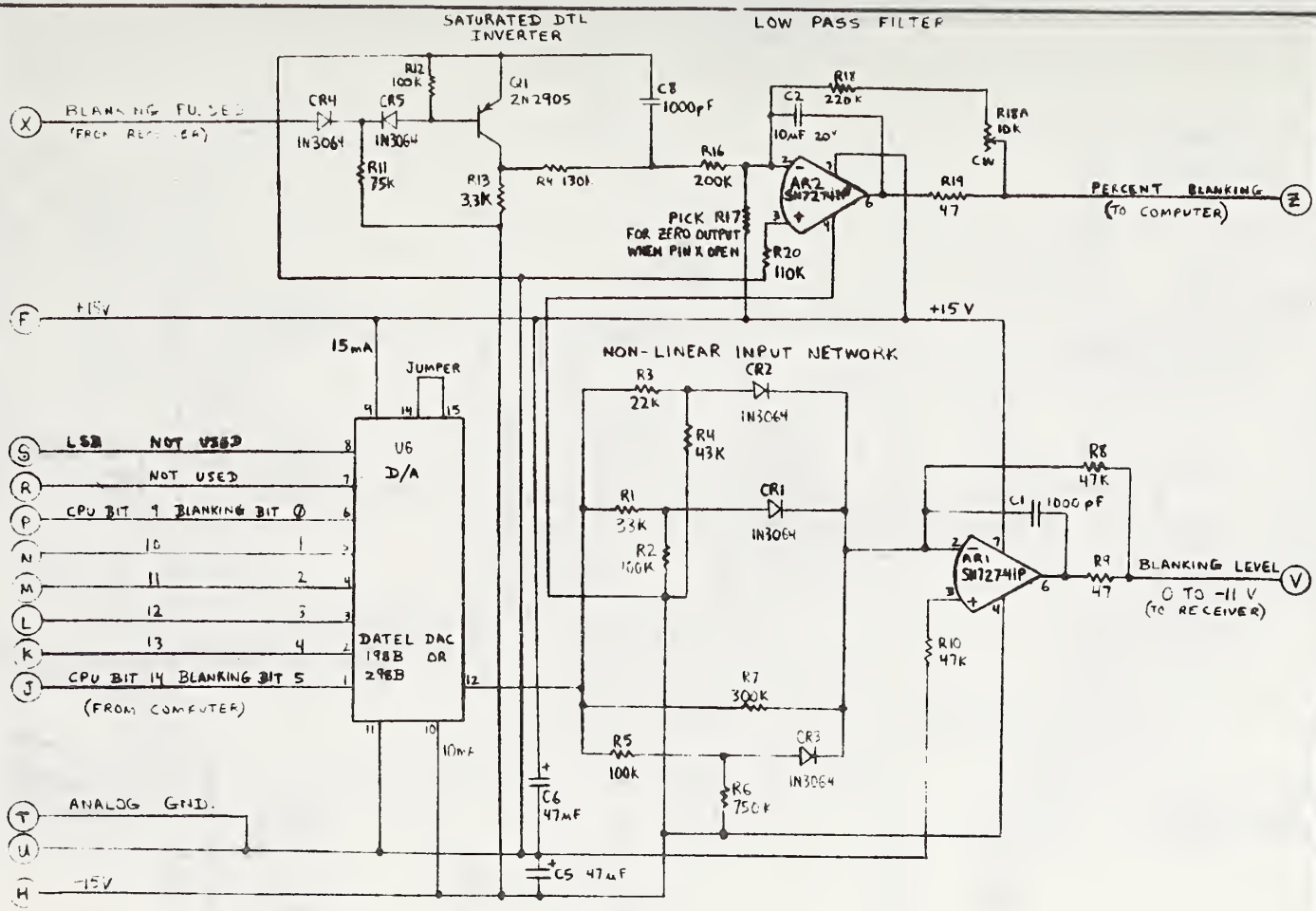
PIECE NO	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

GAIN-TRACKING-PHASE CARD 2 OF 2

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF SEC	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF DIV



S4000.
BLANKING & INE CARD IN ADACS
SHEET 1 OF 2
FIGURE 33

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

TRANSISTOR PINS:

BOTTOM VIEW

SN72741P PINS

TOP VIEW

2N2907 MAY BE USED INSTEAD OF 2N2905

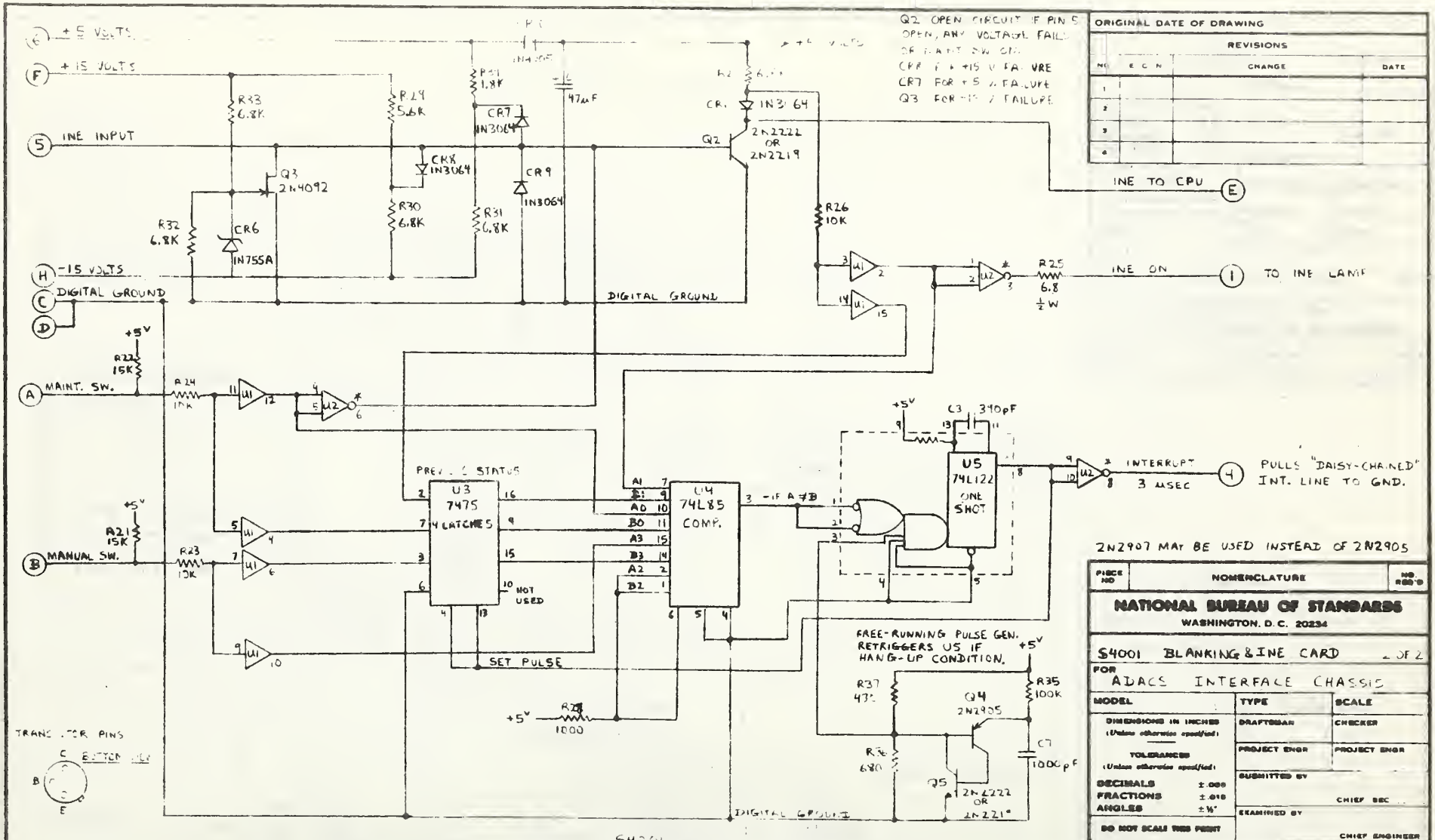
PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

S4001 BLANKING & INE CARD 1 OF 2

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
DO NOT SCALE THIS PRINT	EXAMINED BY	CHIEF ENGINEER
DIV. SEC. THIS PRINT ISSUED	APPROVED BY	CHIEF, DIV



Q2 OPEN CIRCUIT IF PIN 5 OPEN, ANY VOLTAGE FAILS OR PLANT SW. ON.
CR8 FOR +15 V FAILURE
CR7 FOR +5 V FAILURE
Q3 FOR -15 V FAILURE

2N2907 MAY BE USED INSTEAD OF 2N2905

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO.	E.C.N.	CHANGE	DATE
1			
2			
3			
4			

PIECE NO.	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D.C. 20234

S4001 BLANKING & INE CARD 2 OF 2

FOR AIDACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.016 ANGLES ±½°	SUBMITTED BY	CHIEF SEC.
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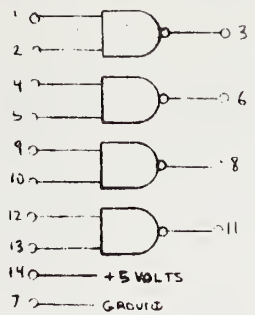
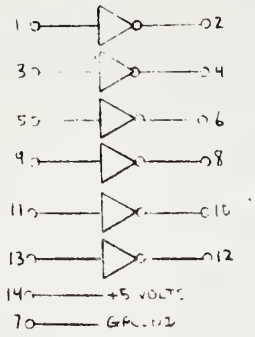
ENG. SEC. THIS PRINT ISSUED	APPROVED BY	CHIEF DIV.

S4001
BLANKING & INE CARD IN AIDACS
SHEET 2 OF 2
FIGURE 34

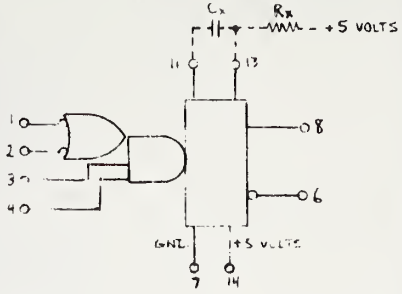
7400 QUAD 2-INPUT NAND GATE
COMPONENT LOCATIONS F & G



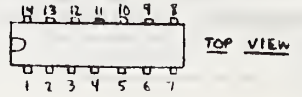
7406 HEX INVERTER BUFFER
OPEN COLLECTOR
HIGH VOLTAGE OUTPUTS
COMPONENT LOCATION P



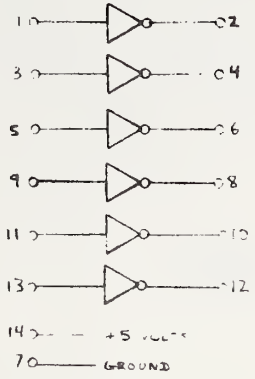
74121 MONOSTABLE MULTIVIBRATOR
FAIRCHILD
COMPONENT LOCATIONS K & P



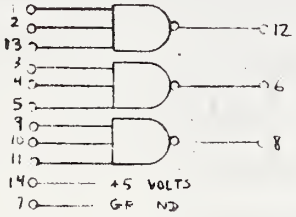
DUAL IN LINE INTEGRATED CIRCUITS
14 PINS
TTL LEVELS
TEXAS INSTRUMENTS (EXCEPT TTL 9601)



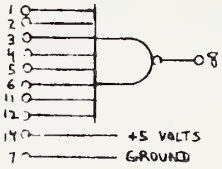
7405 HEX INVERTER
OPEN COLLECTOR
COMPONENT LOCATIONS M, N & S



7410 TRIPLE 3-INPUT NAND GATE
COMPONENT LOCATIONS D, E, H & J



7430 SINGLE 8-INPUT NAND GATE
COMPONENT LOCATION L.

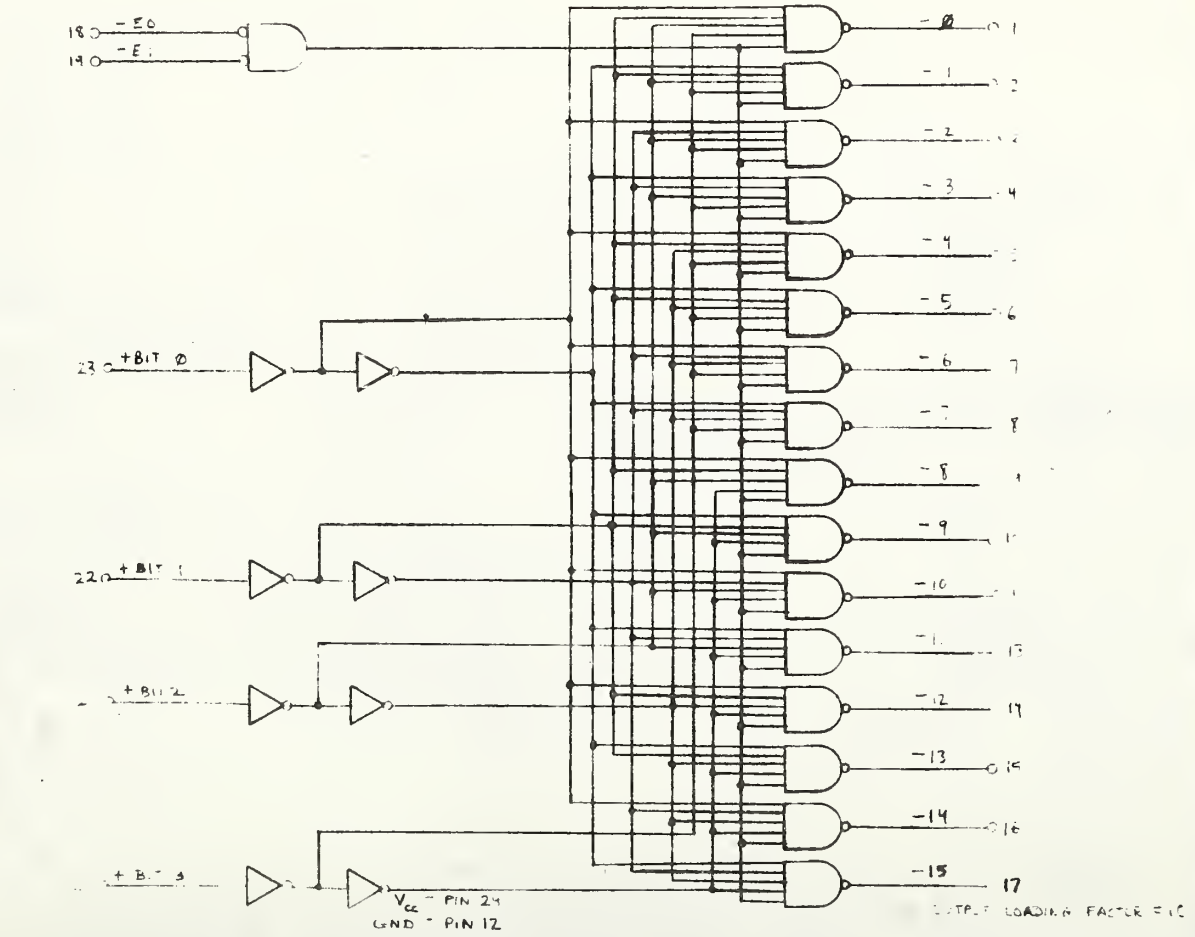


IC'S ON GAIN-TRACKING-PHASE CARD
IN AIACS
FIGURE 35

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

PIECE NO	NOMENCLATURE	NO. REQ'D
	NATIONAL BUREAU OF STANDARDS WASHINGTON, D. C. 20234	
	IC'S ON GAIN-TRACKING-PHASE CARD	
	FOR AIACS INTERFACE CHASSIS	

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.000 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF SEC	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF DIV



MC8311P ON GAIN-TRACKING-PHASE CARD IN ADACS
SHEET 1 OF 2
FIGURE 36

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

MOTOROLA MC8311P
TTL LEVELS
175 MW. POWER DISSIPATION

GAIN-TRACKING-PHASE CARD
COMPONENT LOCATIONS A, B & C.

PIECE NO	NOMENCLATURE	NO. REQ'D
NATIONAL BUREAU OF STANDARDS WASHINGTON, D.C. 20234		
MC8311P ON GAIN-TRACKING-PHASE CARD		
FOR ADACS INTERFACE CHASSIS		

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKED
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF SEC.
DO NOT SCALE THIS PRINT	EXAMINED BY	CHIEF ENGINEER
DIV. SEC. THIS PRINT ISSUED	APPROVED BY	CHIEF DIV

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

INPUT					OUTPUT														
EI	D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0 = GROUND

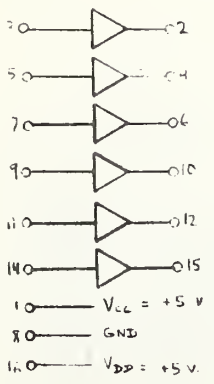
1 = +V

MC 8311P ON GAIN-TRACKING PHASE CARD
SHEET 2 OF 2

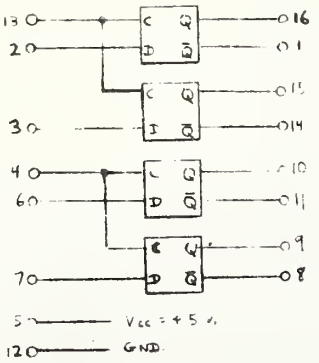
FIGURE 37

PIECE NO	NOMENCLATURE	NO. REQ'D
NATIONAL BUREAU OF STANDARDS WASHINGTON, D.C. 20234		
MC 8311P ON GAIN-TRACKING-PHASE CARD		
FOR ADACS INTERFACE CHASSIS		
MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified) TOLERANCES (Unless otherwise specified) DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	DRAFTSMAN	CHECKER
	PROJECT ENGR	PROJECT ENGR
DO NOT SCALE THIS PRINT	SUBMITTED BY CHIEF, SEC.	
	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF, DIV.

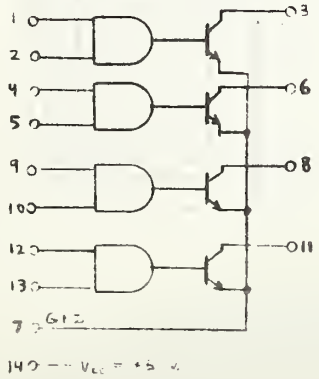
U1 COS/MOS BUFFERS
RCA CD4010AE
NON-INVERTING
16 PIN DUAL IN LINE



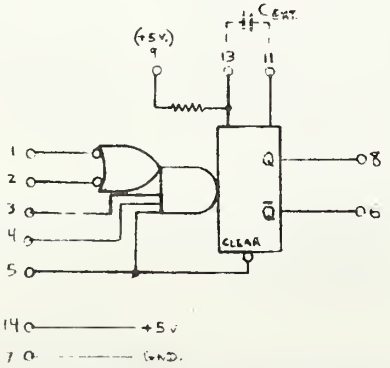
U3 FOUR LATCHES
TEXAS INSTRUMENTS SN7475
4 LATCHES
16 PIN DUAL IN LINE



U2 TWO-INPUT NAND POWER DRIVERS
SPRAGUE UHP408
INVERTING
OPEN COLLECTOR
TTL/DTL INPUT
14 PIN DUAL IN LINE



U5 RETRIGGERABLE ONE SHOT WITH CLEAR
TEXAS INSTRUMENTS SN74L122
TTL LEVELS
14 PIN DUAL IN LINE



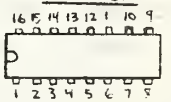
IC'S ON SHOT CARD IN ADACS

FIGURE 38

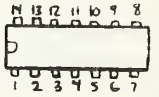
ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

TOP VIEW

U1 & U3
16 PIN



U2 & U5
14 PIN

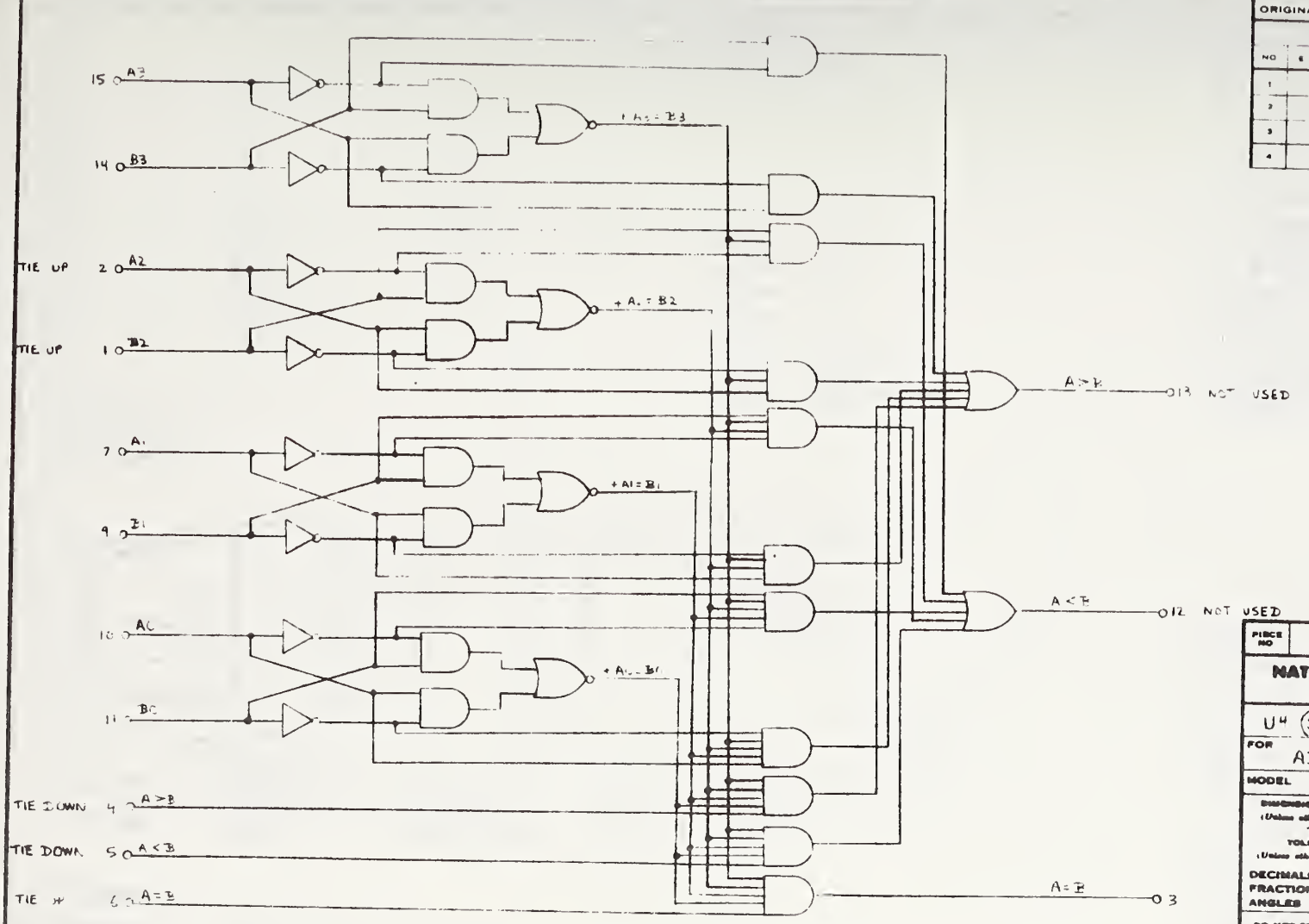


PIECE NO	NOMENCLATURE	NO. REQ'D

NATIONAL BUREAU OF STANDARDS
WASHINGTON, D. C. 20234

IC'S FOR BLANKING LEVEL CARD
FOR
ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.000 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY CHIEF SEC.	
DO NOT SCALE THIS PRINT	EXAMINED BY CHIEF ENGINEER	
DIV. SEC.	THIS PRINT ISSUED	APPROVED BY CHIEF, DIV.

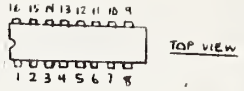


U4 (SN74L85) IN SN54L01, BLANKING LEVEL CARD

FIGURE 34

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
1			
2			
3			
4			

U4 MAGNITUDE COMPARATOR
TEXAS INSTRUMENTS SN74L85
16 PIN DUAL IN LINE
A=B PORTION USED



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WASHINGTON, D.C. 20234

U4 (SN74L85) ON BLANKING LEVEL CARD FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005 FRACTIONS ±.015 ANGLES ±½°	SUBMITTED BY	CHIEF, SEC.
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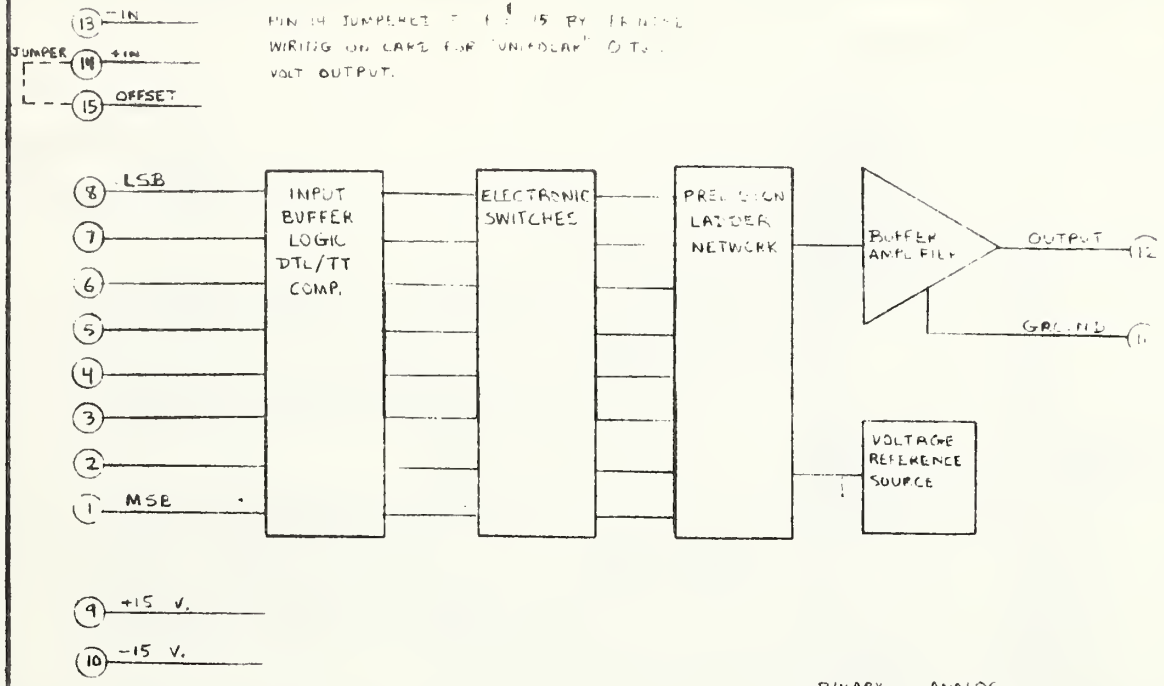

BINARY INPUT	ANALOG OUTPUT
1111 1111	+9.96 VOLTS
1110 0000	+8.7
1100 0000	+7.5
1000 0000	+5.0
0100 0000	+2.5
0010 0000	+1.2
0000 0000	0.0

BOTTOM VIEW

L6 ON 5400 CARD

FIGURE 4C

ORIGINAL DATE OF DRAWING			
REVISIONS			
NO	E C N	CHANGE	DATE
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4			

DIGITAL TO ANALOG CONVERTER - 8 BITS
DATEL DAC 198B OR 298 B BINARY
OUTPUT SETTLING TIME 20 μSEC. TO ±0.2%
DTL/TTL LOGIC LEVELS FOR INPUT
OUTPUT 0 TO 10 VOLTS @ 5 MA
POWER INPUT ±15 VOLTS @ ±20 MA.
SIZE 2" x 2" x 0.4"

PIECE NO	NOMENCLATURE	NO REQ'D
NATIONAL BUREAU OF STANDARDS WASHINGTON, D.C. 20234		
U6 ON BLANKING LEVEL CARD		
FOR ADACS INTERFACE CHASSIS		
MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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REVISIONS			
NO	E C N	CHANGE	DATE
1			
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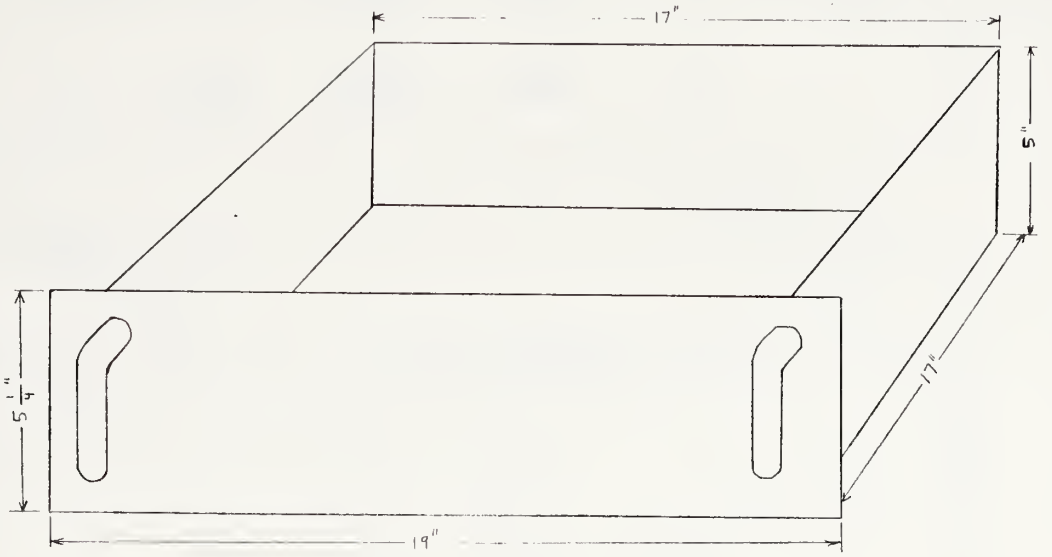
CHASSIS FOR MOUNTING IN 19" RACK. SLIDES ON SIDES AND HANDLES ON FRONT ARE REQUIRED. CHASSIS MUST BE ENCLOSED ON ALL SIDES AND ON BOTTOM.
ALUMINUM

MEASUREMENTS ARE IN INCHES AND ARE APPROXIMATE PER MOUNTING IN 19" RACK.



FRONT VIEW

AIACS BASIC CHASSIS
FIGURE 41

PIECE NO	NOMENCLATURE	NO. REQ'D

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BASIC CHASSIS

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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FRACTIONS ±.015	CHIEF, SEC.	
ANGLES ±½°	EXAMINED BY	
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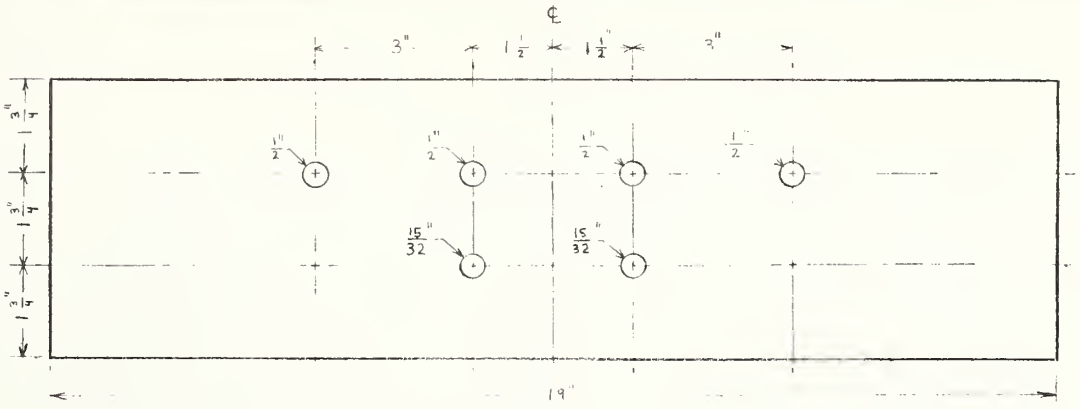
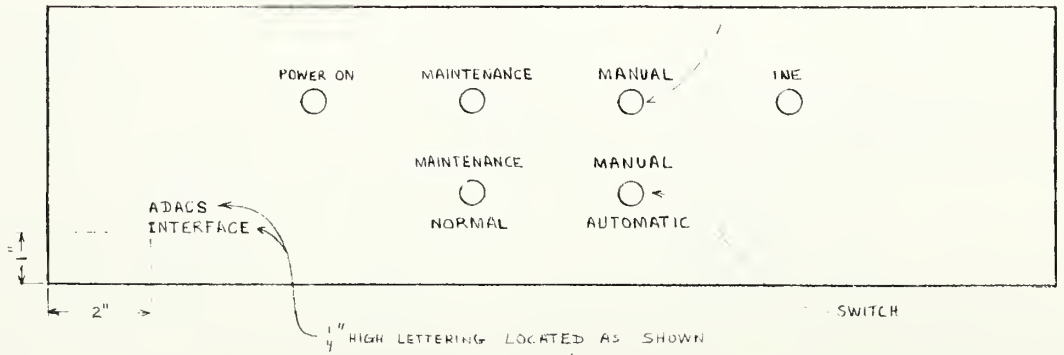


ALL DIMENSIONS IN INCHES



1/4" HIGH LETTERING LOCATED AS SHOWN

ALL OTHER LETTERING 1/8" HIGH AND CENTERED 3/16" ABOVE AND BELOW HOLES.

WHITE LETTERING ON GRAY PANEL

ADACS FRONT PANEL

FIGURE 42.

ORIGINAL DATE OF DRAWING 5-1-72			
REVISIONS			
NO	E C N	CHANGE	DATE
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4			

PIECE NO	NOMENCLATURE	NO. REQ'D

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FRONT PANEL

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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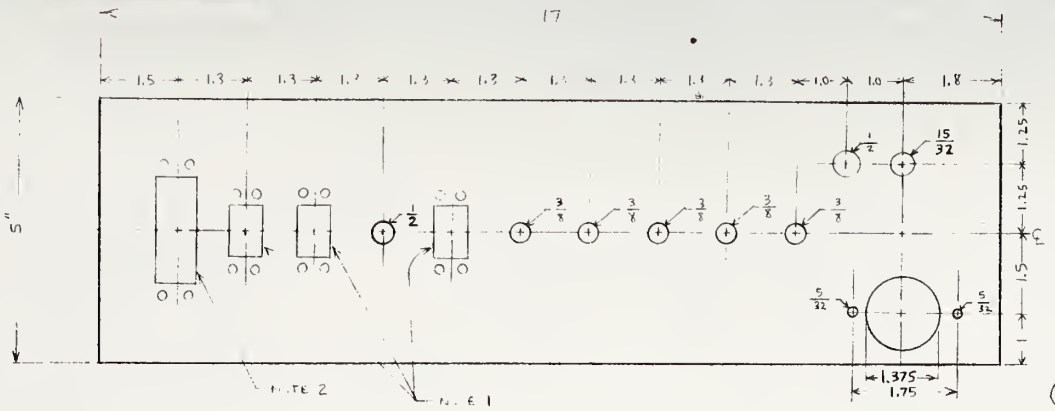
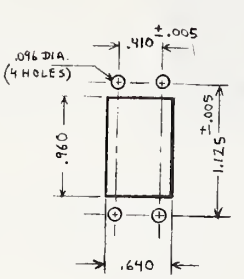
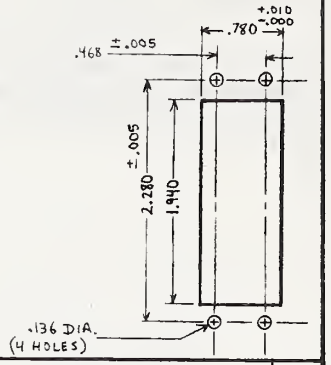
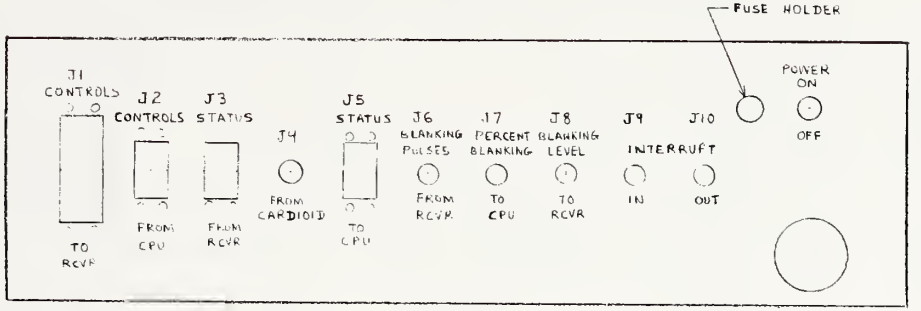


NOTE 1:
ELCO 8016
20 CONTACTS

NOTE 2:
ELCO 8016
56 CONTACTS







ALL LETTERING IN BLACK AND $\frac{1}{8}$" HIGH

LETTERING CENTERED $\frac{3}{16}$" ABOVE AND BELOW CIRCULAR HOLES; $\frac{3}{8}$" FOR RECTANGULAR HOLES

ALL DIMENSIONS IN INCHES

ADACS BACK PANEL
FIGURE 43

ORIGINAL DATE OF DRAWING	

REVISIONS

NO	E C N	CHANGE	DATE
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BACK PANEL

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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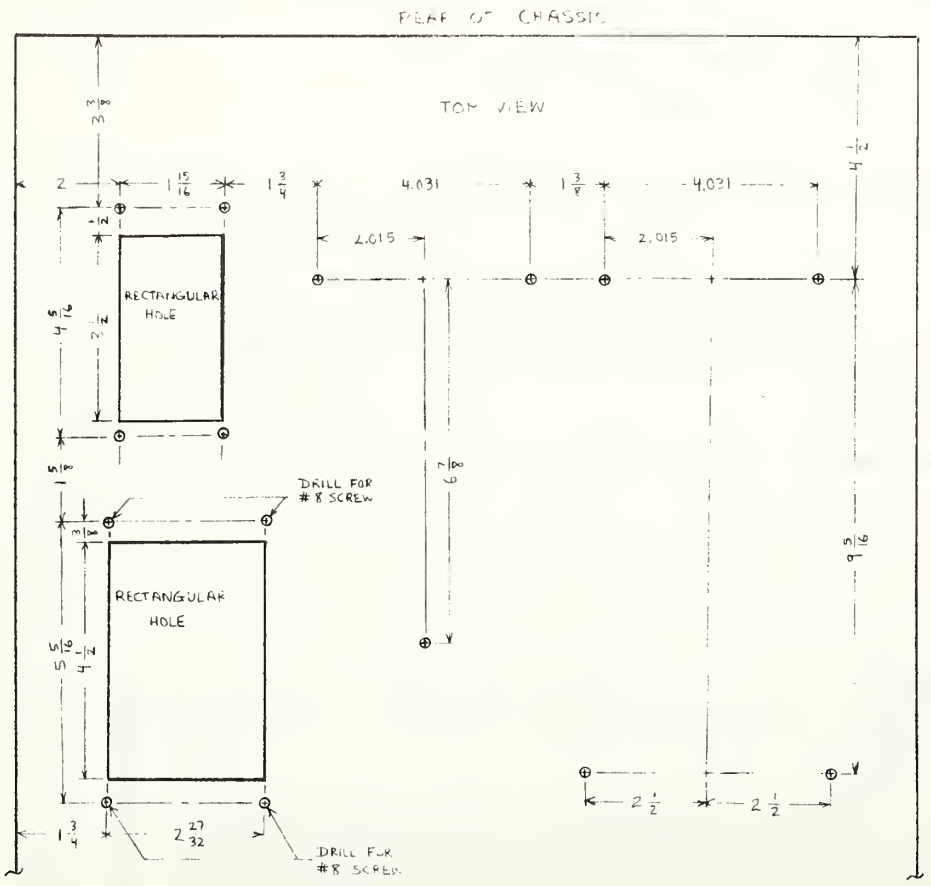

FLOOR OF ADACS CHASSIS
FIGURE 44

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
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HOLES: CUT RECTANGULAR HOLES AS SHOWN
ALL ROUND HOLES DRILLED FOR #6 SCREW, UNLESS OTHERWISE NOTED.
COUNTERSINK ALL ROUND HOLES FOR FLAT HEAD SCREWS.

DIMENSIONS: ALL DIMENSIONS IN INCHES AND MEASURED FROM OUTSIDE OF CHASSIS

CHASSIS HAS DIVELPRO PART NUMBER DIV. 472

PIECE NO.	NOMENCLATURE	NO. REQ'D

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FLOOR OF CHASSIS

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
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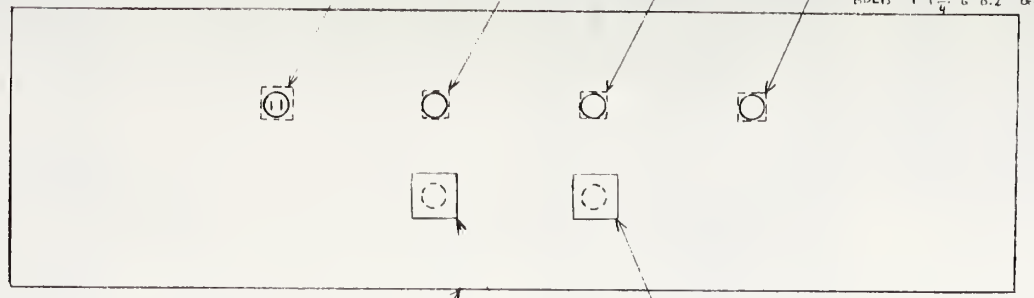
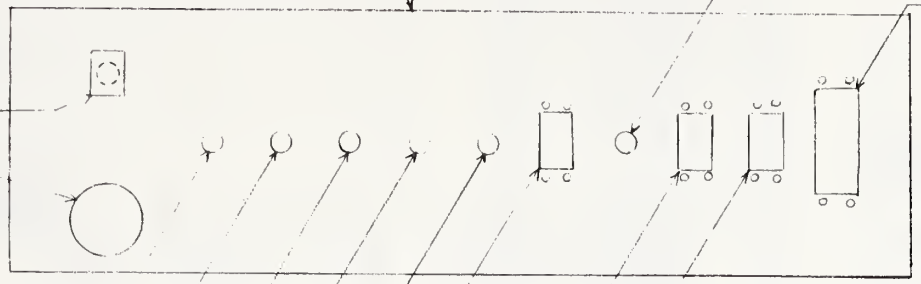
REAR VIEW OF FRONT PANEL:



PART OF CHASSIS
DIVELPRO # DIV472

FRONT (INSIDE) VIEW OF BACK PANEL:



CONTACTS
ELCO # 60-8017-0313
CABLE PLUG
ELCO # 00-8016-020-000-703
20 PIN CONNECTOR
ELCO # 00-8016-020-000-701

ADAC FRONT & BACK PANEL COMPONENTS

FIGURE 45

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
NO	E C N	CHANGE	DATE
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FRONT & BACK PANEL, COMPONENTS

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR.	PROJECT ENGR
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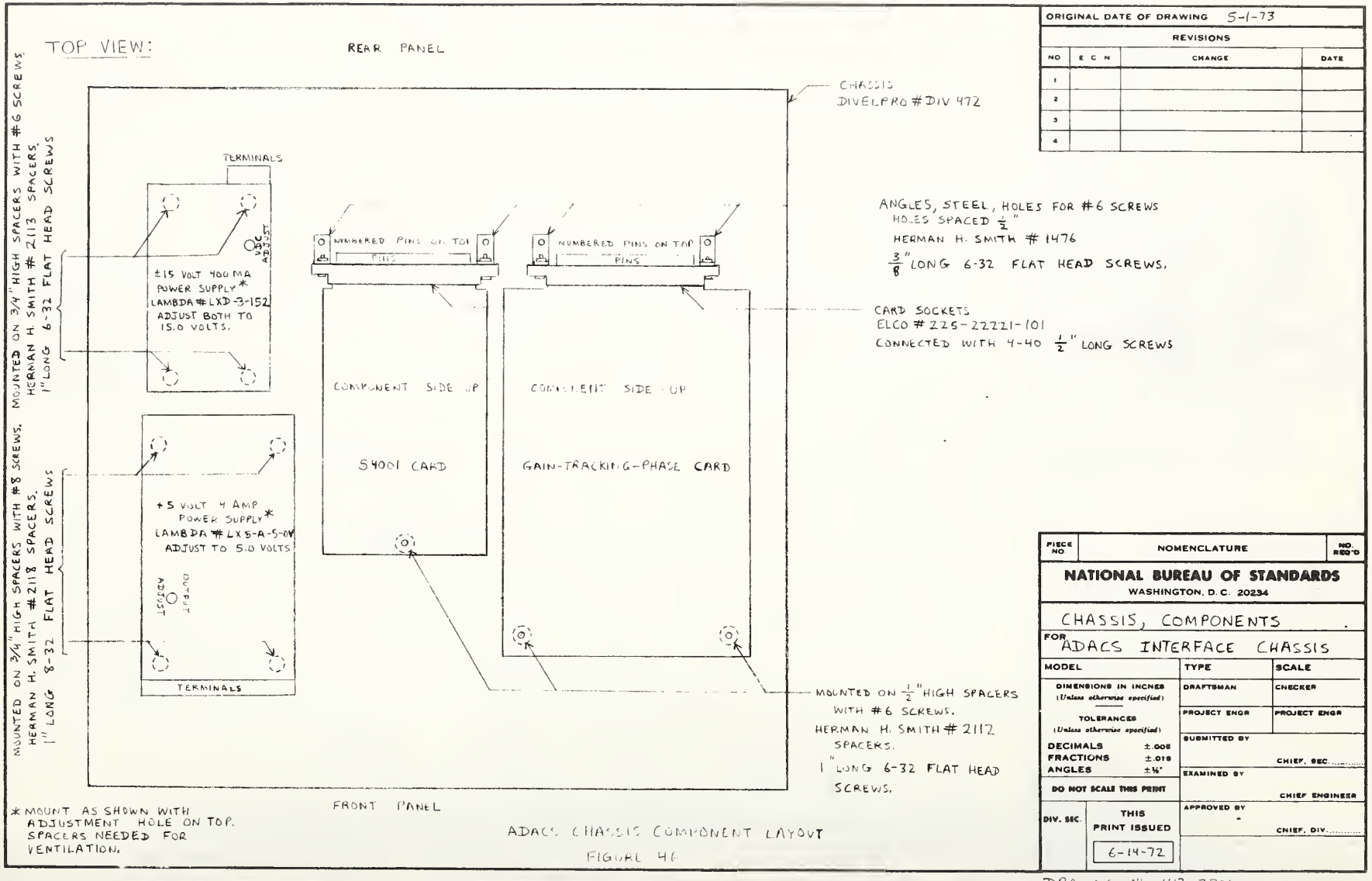

ADACS CHASSIS COMPONENT LAYOUT

FIGURE 46

ORIGINAL DATE OF DRAWING 5-1-73			
REVISIONS			
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WASHINGTON, D.C. 20234

CHASSIS, COMPONENTS

FOR ADACS INTERFACE CHASSIS

MODEL	TYPE	SCALE
DIMENSIONS IN INCHES (Unless otherwise specified)	DRAFTSMAN	CHECKER
TOLERANCES (Unless otherwise specified)	PROJECT ENGR	PROJECT ENGR
DECIMALS ±.005	SUBMITTED BY	
FRACTIONS ±.015		CHIEF, SEC.
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7. AUTHOR(S) R. J. Carpenter, K. M. Gray, D. S. Grubb and L. J. Palombo

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

The Field Service Test Model uses a computer to control the operation of from 1 to 15 EECO 881 receivers for unattended operation. Each receiver is connected to the computer by an ADACS Interface Chassis, which provides the necessary decoding and conversion for communication between the receiver and the computer.

This manual describes the overall operation of the system, modifications needed for the receivers, and construction of the ADACS Interface Chassis.

17. KEY WORDS (Alphabetical order, separated by semicolons)

Computer-control; radio receiver; U system

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☒ FOR OFFICIAL DISTRIBUTION. DO NOT RELEASE TO NTIS.

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