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U.S. DEPARTMENT OF COMMERCE/National Bureau of Standards

CHANNEL LEVEL POWER CONTROL INTERFACE

CATEGORY: HARDWARE STANDARD
SUBCATEGORY: INTERFACE

U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*

Foreword

The Federal Information Processing Standards Publication Series of the National Bureau of Standards is the official publication relating to standards adopted and promulgated under the provisions of Public Law 89-306 (Brooks Act) and under Part 6 of Title 15, Code of Federal Regulations. These legislative and executive mandates have given the Secretary of Commerce important responsibilities for improving the utilization and management of computers and automatic data processing in the Federal Government. To carry out the Secretary's responsibilities, the NBS, through its Institute for Computer Sciences and Technology, provides leadership, technical guidance, and coordination of Government efforts in the development of guidelines and standards in these areas.

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Abstract

This standard defines the functional, electrical, and mechanical interface specifications for a power control interface for use in connecting computer peripheral equipment as a part of automatic data processing (ADP) systems. This standard, together with a companion standard for I/O Channel Interface, defines the hardware characteristics for the I/O channel level interface. This revision supersedes FIPS PUB 61 in its entirety.

The Government's intent in employing this Channel Level Power Control Interface standard is to reduce the cost of satisfying the Government's data processing requirements through increasing its available alternative sources of supply for computer system components at the time of initial system acquisition, as well as in system replacement and augmentation and in system component replacement. This standard is also expected to lead to improved reutilization of system components.

When acquiring ADP systems and system components, Federal agencies shall cite this standard in specifying the power control interface for connecting computer peripheral equipment as a part of ADP systems.

Key words: automatic data processing (ADP); channel level power control interface; computer peripherals; computers; Federal Information Processing Standard; input/output; interfaces.

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Federal Information Processing Standards Publication 61-1

1982 July 13

ANNOUNCING THE STANDARD FOR

CHANNEL LEVEL POWER CONTROL INTERFACE

Federal Information Processing Standards Publications are issued by the National Bureau of Standards pursuant to section 111(f)(2) of the Federal Property and Administrative Services Act of 1949, as amended, Public Law 89-306 (79 Stat. 1127), Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 Code of Federal Regulations (CFR).

Name of Standard. Channel Level Power Control Interface (FIPS PUB 61-1).

Category of Standard. Hardware Standard, Interface.

Explanation. This standard defines the functional, electrical, and mechanical interface specifications for a power control interface for use in connecting computer peripheral equipment as a part of automatic data processing (ADP) systems. This standard, together with a companion standard for I/O Channel Interface, defines the hardware characteristics for the I/O channel level interface. This revision makes optional the Emergency Power Off (EPO) capability as specified in FIPS PUB 61 and supersedes FIPS PUB 61 in its entirety.

The Government's intent in employing this Channel Level Power Control Interface Standard is to reduce the cost of satisfying the Government's data processing requirements through increasing its available alternative sources of supply for computer system components at the time of initial system acquisition, as well as in system replacement and augmentation and in system component replacement. This standard is also expected to lead to improved reutilization of system components.

When acquiring ADP systems and system components, Federal agencies shall cite this standard in specifying the power control interface for connecting computer peripheral equipment as a part of ADP systems.

Approving Authority. Secretary of Commerce.

Maintenance Agency. Department of Commerce, National Bureau of Standards (Institute for Computer Sciences and Technology).

Cross Index. American National Standards Institute document X3T9/666, Rev. 2, Draft Proposed American National Standard Specifications for Power Control Interface.

Applicability. This standard is applicable whenever use of Federal Information Processing Standard I/O Channel Interface (FIPS-PUB-60-1) is required.

Verification of the correct operation of all interfaces that are required to conform to this standard shall, through demonstration or other means acceptable to the Government, be provided prior to the acceptance of all applicable ADP equipment.

Specifications. This standard incorporates by reference the technical specifications of ANSI document number X3T9/666, Rev. 2. Copies of the technical specifications section of the standard will be available from the National Technical Information Service as described in the **Where to Obtain Copies** section below.

Implementation. The provisions of this standard are effective June 23, 1980. All applicable equipment ordered on or after the effective date, or procurement actions for which solicitation

documents have not been issued by that date, must conform to the provisions of this standard unless a waiver has been granted in accordance with the procedure described elsewhere in this standard.

Regulations concerning the specific use of this standard in the Federal procurement will be issued by the General Services Administration to be a part of the Federal Property Management Regulations.

This standard shall be reviewed by NBS within 3 years after its effective date, taking into account technological trends and other factors, to determine whether the standard should be reaffirmed, revised, or withdrawn.

Waivers. Heads of agencies desiring a waiver from the requirements stated in this standard so as to acquire ADP equipment that does not conform to this standard, shall submit a request for such a waiver to the Secretary of Commerce for review and approval. Approval will be granted if, in the judgment of the Secretary based on all available information, including that provided in the waiver request, a major adverse economic or operational impact would occur through conformance with this standard.

A request for waiver shall include: (1) a description of the existing or planned ADP system for which the waiver is being requested, (2) a description of the system configuration, identifying those items for which the waiver is being requested, and including a description of planned expansion of the system configuration at any time during its life cycle, and (3) a justification for the waiver, including a description and discussion of the major adverse economic or operational impact that would result through conformance to this standard as compared to the alternative for which the waiver is requested.

The request for waiver shall be submitted to the Secretary of Commerce, Washington, DC 20230, and labeled as a request for Waiver to a Federal Information Processing Standard. Waiver requests will normally be processed within 45 days of receipt by the Secretary. No action shall be taken to issue solicitation documents or to order equipment for which this standard is applicable and which does not conform to this standard prior to receipt of a waiver approval response from the Secretary.

Where to Obtain Copies. Either paper or microfiche copies of this Federal Information Processing Standard, including the technical specifications, may be purchased from the National Technical Information Service (NTIS) by ordering Federal Information Processing Standards Publication 61-1 (FIPS-PUB-61-1), Channel Level Power Control Interface. Ordering information, including prices and delivery alternatives, may be obtained by contacting the National Technical Information Service (NTIS), U.S. Department of Commerce, Springfield, VA 22161, Telephone: (703) 487-4650. Payment may be made by check, money order, or deposit account.

TECHNICAL SPECIFICATIONS

FOR

CHANNEL LEVEL POWER CONTROL INTERFACE

Draft Proposed

AMERICAN NATIONAL STANDARD SPECIFICATIONS FOR POWER CONTROL INTERFACE

(Revised)

ABSTRACT

The functional and mechanical specifications are defined for a Power Control Interface which provides a sequential and interlocked means of controlling the power supplied by a computer system power control circuit to attached control units, I/O devices, channel frames, or free-standing storage frames (operating in a REMOTE status) without affecting the power on the rest of the system. By stepping the power (on or off) in discrete system components, the overall power requirements and power surge noise generation are decreased.

Several levels of power may exist, depending on the system configuration. Each (Central Processing Unit) sequentially provides power, via the Power Control Interface, to each stand-alone frame attached to the CPU. Each stand-alone frame (directly attached to the CPU) having units attached (i.e., a channel with a control unit) sequentially controls the power to each attached unit by means of the Power Control Interface.

The Power Control Interface permits the removal of any frame from the system without affecting the power on the rest of the system unless that frame is controlling other frames not shared with other control units. In addition, it has an optional feature to provide system emergency power off capability.

FOREWORD

(This Foreword is not a part of the Standard, Specifications for Power Control Interface.)

This Standard provides the specifications for the functional and mechanical characteristics of a Power Control Interface for a general purpose computer system. The Power Control Interface provides a means of controlling the power supplied by a computer system power control circuit to attached frames (operating in a remote status) without affecting the power on the rest of the system. These attached frames include control units, I/O devices, channel frames, or free-standing storage frames.

The Interface provides power-on, power-off, and emergency-power-off control to discrete systems in steps, thereby decreasing the overall power requirements and the power surge noise generation.

The design of this interface includes the following features:

1. Several levels of power depending on the system configuration.
2. Sequential power control from each Central Processing Unit (CPU) to each stand-alone frame attached to that CPU.
3. Sequential power control from each stand-alone frame (directly attached to the CPU) to each unit attached to it.
4. Provides System Emergency Power Off (EPO) capability (optional feature).

Included in the Standard is a description of the interconnections of all lines, the functional descriptions of each of these lines, and the sequence of signals on the lines for power control of connected units for both LOCAL and REMOTE operation. Implementation of the Power Control Interface also permits the removal of any control unit, I/O device, channel frame, or free-standing storage frame from the system without affecting the power on the rest of the system unless the unit removed controls other frames not shared with other control units.

The Mechanical Specification of the Interface is defined in chapter 3 of the Standard. The mechanical specification describes two system and multi-system interconnection with interlocking of the EPO circuits.

This Standard modifies the technical specifications of ANSI document X3T9/666, Rev. 2, to make Emergency Power Off capability optional.

Subcommittee X3T9 on I/O Interface, which developed X3T9/666, Rev. 2, had the following members:

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CHAPTER 1.

Introduction

1.1 Scope. This document provides the description of a Power Control Interface which will enable manufacturers to design equipment which is compatible in its power sequencing and controls. The definitions and descriptions of the power control interface lines and the optional emergency power off feature are included.

CHAPTER 2.

Functional Specification

2.1 Power Control Interface General Description. The Power Control Interface provides a sequential and interlocked means for systems powering. Stepping power in discrete systems components (sections) decreases overall power requirements and lessens power surge noise generation. All systems operating in remote control status have their powering controlled by the system power control circuit.

Several levels of power may exist, depending on the system configuration. Each central processing unit (CPU) sequentially provides power, via the power control interface, to each stand-alone frame attached to that CPU. Each stand-alone frame (directly attached to the CPU) which has units attached (a channel with a control unit), requires controls to sequentially power each such attached unit by means of the power control interface. (See figure 1 for multiple applications of the power control interface.)

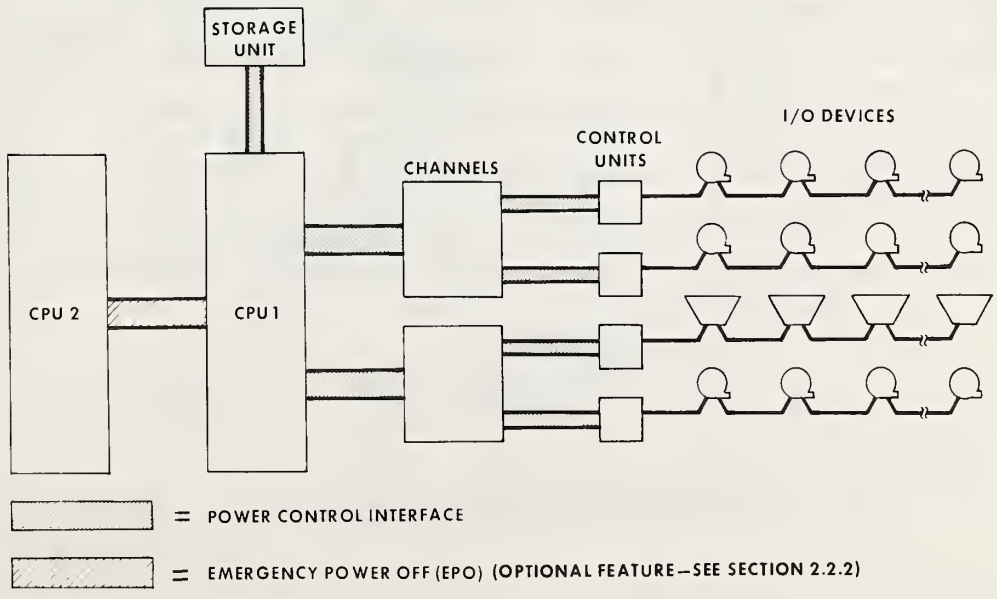


FIGURE 1. Power control interface-system application

For purposes of discussion in this publication, the controlling element will be referred to as the *system* and the controlled element as the *unit.*

2.2 Interface Line Descriptions. The power control interface lines are shown in figures 2 and 3. A power control configuration for a shared system is shown in figure 4.

These lines are assigned as follows:

Power Connector Block Pin Number	Line Name	Line Abbreviation
1	Unit Source	Unit Source
2	*EPO Control	EPO Ctrl
3	System Source	Sys Source
4	Powering Complete	Pwr Compl
5	Power Hold	Powr Hold
6	Power Pick	Pwr Pick

*EPO = Emergency Power Off (optional feature—see section 2.2.2)

The time relationships of the signals on these lines are shown in figures 5 and 6.

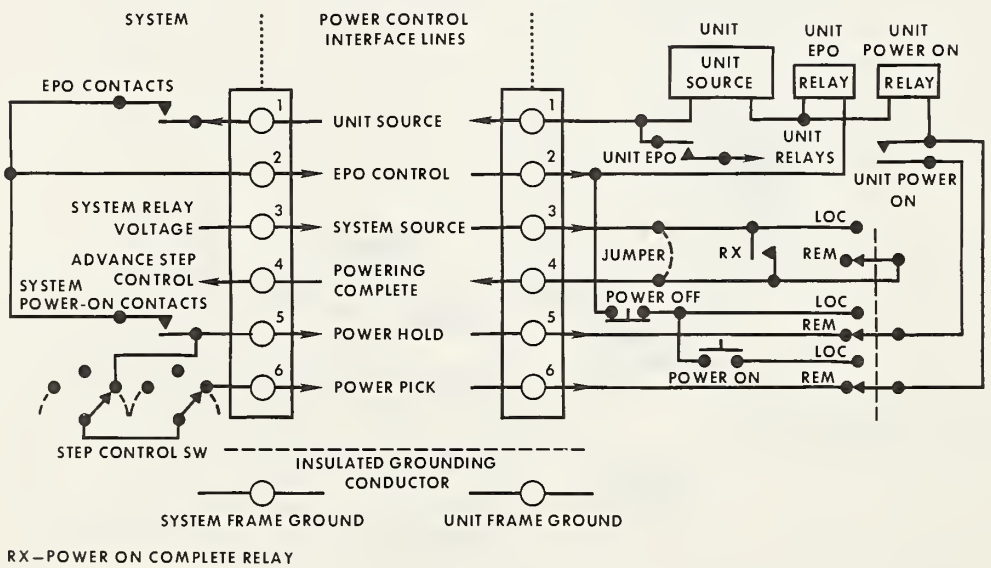
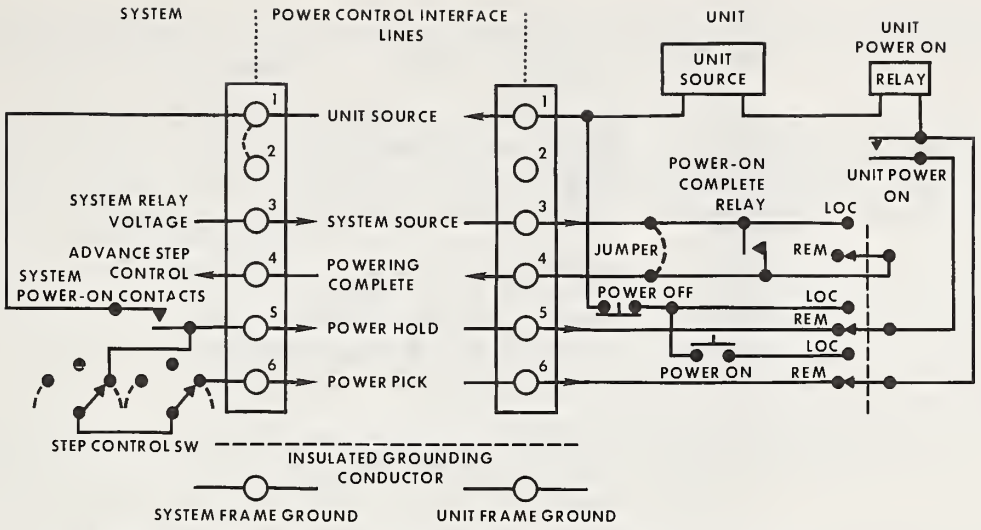
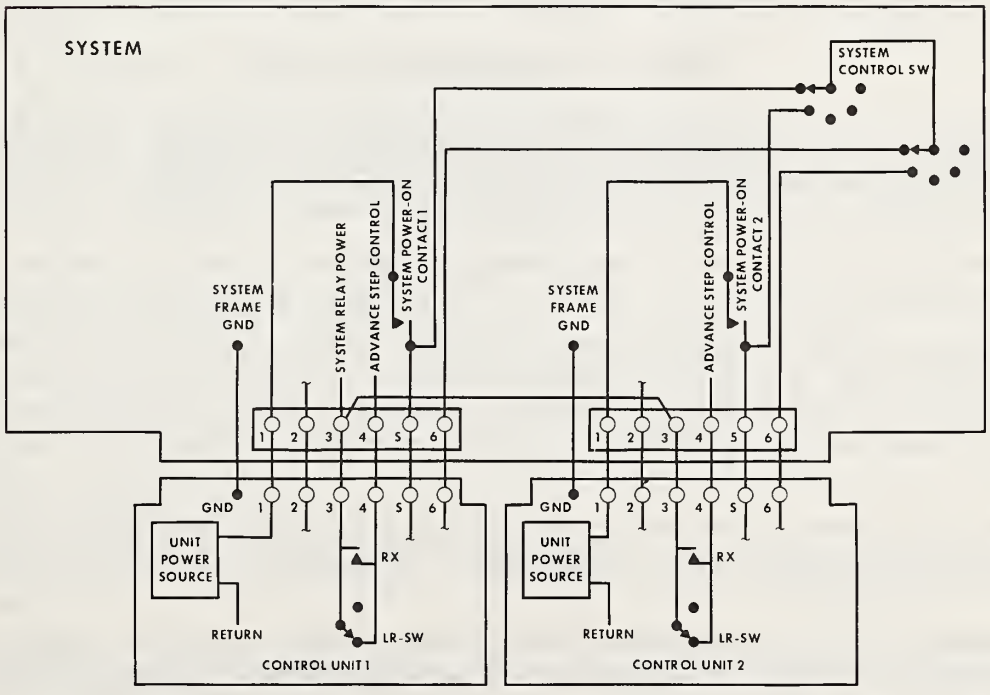


FIGURE 2. Typical power control with EPO



NOTE: THE JUMPER THAT CONNECTS PINS 1 & 2 AT THE SYSTEM INTERFACE ACCOMMODATES ATTACHMENT OF I/O THAT HAVE AN "EMERGENCY POWER-OFF" SWITCH

FIGURE 3. Typical power control without EPO



LR SW—LOCAL/REMOTE SW
RX—POWER-ON COMPLETED RELAY

FIGURE 4. Typical power control for a shared system

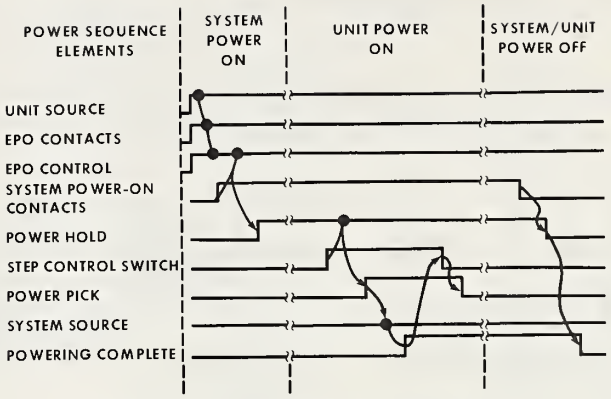


FIGURE 5. Typical power sequence with EPO

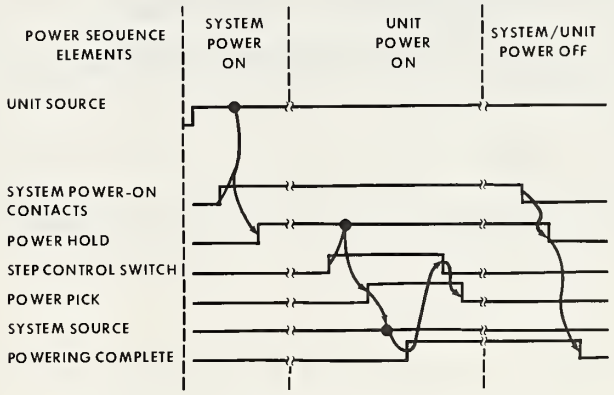


FIGURE 6. Typical power sequence without EPO

2.2.1 **Unit Source.** The 'unit source' line provides a power source from the unit being sequenced on. The power source supplies the power required by the unit for the 'EPO control,' 'power pick,' and 'power hold' functions. This 'unit source' line should not be loaded by the system.

The maximum allowable current drawn through the 'unit source' line is 500 milliamperes at 24 volts. The minimum allowable current drawn while energizing a coil or coils is 30 milliamperes.

2.2.2 **Emergency Power Off Control** (optional feature). The 'emergency power off (EPO) control' line is connected to the 'unit source' line when the EPO relay contacts are closed. In the event of an EPO condition, this line opens. This feature is an option for both control units and channels; however, the lines and pins associated with EPO are reserved and may not be used for other purposes.

Note: The EPO option is required for any installations which do not implement a disconnecting means in the data processing room in conformance to Article 645 of the National Electrical Code, ANSI/NFPA No. 70-1978.

2.2.3 **System Source.** The 'system source' line provides a power source from the system controlling the sequencing. This source supplies the power to advance the system step control circuit. This source should not be loaded by the unit.

The maximum allowable current drawn through the 'system source' line is 500 milliamperes at 24 volts. The minimum allowable current drawn while energizing a coil or coils is 30 milliamperes.

2.2.4 Powering Complete. The 'powering complete' line is connected to the 'system source' line when one of three conditions exist:

1. Local/remote switch is set to LOCAL.
2. Local/remote switch is set to REMOTE and the unit-power sequence is complete. 'System source' supplies power to the power complete line via the power-on completed relay contact. This connection need be maintained only as long as the 'power pick' line is energized. (See section 2.2.6 "Power Pick.")
3. Power for the unit is not controlled by the system and a jumper is placed between the two lines.

2.2.5 Power Hold. The 'power hold' line is connected to the 'unit source' line when the system has power on. 'Power hold' causes unit power to remain on (after once being turned on) until either:

1. System power is dropped with the unit local remote switch set to REMOTE, or,
2. Unit power is locally turned off by the unit power off switch when the unit local remote switch is set to LOCAL. (Refer to section 2.3.2 "Power Off.")

2.2.6 Power Pick. The 'power pick' line is connected to the 'power hold' line when the step control switch closes the contacts for the unit to be powered. It is connected, in this manner, until the step control senses a signal on the 'powering complete' line.

'Power pick' initiates the power-on sequence in the unit (providing the unit is in remote status). The maximum allowable current drawn through the 'power pick' line is 500 milliamperes at 24 volts.

A possible implementation would be for 'power pick' to be connected to the unit-power-on relay coil. Energizing this relay with 'power pick' causes one of its contact sets to connect power hold to the coil, thus keeping the relay energized after 'power pick' drops and as long as 'power hold' remains energized. (See figure 2.)

2.3 Normal Power Sequencing Conditions

2.3.1 Power On.

With EPO option (refer to figure 2 for the following):

1. With the EPO switch reset, the system power-on switch is closed.
2. 'Unit source' voltage is sent from each unit and is returned to each unit (after passing through the EPO relay and power on/off switch contacts for that unit) as the 'EPO control' and 'power hold' lines.

Without EPO option (refer to figure 3 for the following):

1. The system power-on switch is closed.
2. 'Unit source' voltage is sent from each unit and is returned to each unit (after passing through the system power-on contacts as the unit power hold line).

With or without EPO option:

3. 'System source' voltage is sent to all units. (Or, it may already be on before the system power-on switch is closed.)
4. The step control switch advances to the first position.
5. A path from 'power hold' to 'power pick' is completed for the unit connected to the first step position.
6. If the unit local/remote switch is set to LOCAL, no unit power-on sequence takes place due to making 'power pick' active. Instead, the path from 'system source' to 'powering complete' is completed through the local/remote switch.

   If the local/remote switch on the unit is set to REMOTE, unit power-on takes place. When the sequence is complete, the unit closes the path from 'system source' to 'powering complete.' If the unit has a sequential powering circuit to supply power to units attached to

it (i.e., the "unit" actually serves as a "system" as well), bringing up 'powering complete' will be delayed until all units have been powered.

7. Upon receipt of 'powering complete' at the system, the step control switch advances to the next position and opens 'power pick' to the unit just powered.
8. Steps 5, 6, and 7 are repeated until all power sequencing is complete.

2.3.2 Power Off.

1. The system power-on contacts open.
2. The 'power hold' line opens.
3. If the unit is in remote status, the power on the unit drops ('unit source' remains up) and the 'powering complete' line opens.
4. If the unit is in local status, no change in the power status occurs.

2.3.3 Emergency Power Off. When the EPO option is used, emergency power off control is accomplished by contact point control (normally open points that closed after reset of the EPO switch) and all units in the equipment configuration are under the control of EPO regardless of whether in local or remote status. If the EPO option is not used, deactivation of the unit emergency power off switch shall remove all hazardous voltages beyond the unit's power control compartment. (See section 2.4.6 "Unit Emergency Power-Off Switch.")

2.4 Local Power Controls. Certain power controls may be included in a unit (or device) for local control of power, depending on the use and design of the unit.

A unit designed for customers use in an offline mode must make the on/offline, local/remote, power-on, and power-off switches available to the operator.

2.4.1 Local/Remote Switch. Stand-alone frames may have a local/remote switch to permit switching that unit to system power control or to its own power control.

The effect of the setting of this switch, with various combinations of unit and system power, is shown in the table, "Local/Remote Switch Effects." The normal procedure for Case 2 is to bring up unit power before switching to remote. The switching would then have no effects (Case 4).

When in local status, the unit does not respond to any system power control except EPO, if the EPO option is used. The 'powering complete' line for the unit is connected to the 'system source' line via the local/remote switch.

Local/Remote Switch Effects

Case	Switching From:	Unit Power	System Power	Effect
1	Local to Remote	Off	Off	None
2	Local to Remote	Off	On	None*
3	Local to Remote	On	Off	Unit drops power
4	Local to Remote	On	On	None
5	Remote to Local	Either	Either	None

*A unit may be designed to automatically cause power to be turned on in this case, but this is optional.

2.4.2 Online/Offline Switch. Normal use of the local/remote switch for changing the power state of a unit requires the use of the online/offline switch. Transitions in power are then made while in offline mode.

2.4.3 Power-on Switch. The power-on switch must be under the control of the local/remote switch and is active only if the local/remote switch is set to LOCAL.

If power-on switch is not exposed (unit is not to be used by the operator in an offline mode), a pushbutton or toggle switch for power-on condition must be provided. This switch should be readily accessible to maintenance personnel and should be active only in the local position.

2.4.4 Power-Off Switch. If the unit is designed for use in an offline mode, the power-off switch must be a red pushbutton (or toggle switch) readily accessible to the operator. If it is to turn off power without regard to the local/remote switch, it must be labeled POWER OFF. If it turns off power only in local, the power-off pushbutton must be labeled PWR OFF IF IN LOCAL.

A power-off switch is not normally exposed on a unit designed for system power sequencing only. However, if it is exposed, and the local/remote switch is also exposed, the rules stated in the preceding paragraph apply. When the power-off switch is exposed, but the local/remote switch is not, the power-off switch must be labeled PWR OFF IF IN LOCAL.

2.4.5 Supply Disconnect Switch. Each unit must have a supply disconnect switch (circuit breaker) readily accessible to maintenance personnel. This switch is not interlocked by the local/remote switch. The supply disconnect switch shall remove all hazardous voltages beyond the power control compartment. Hazardous voltages shall be removed within two seconds.

2.4.6 Unit Emergency Power-Off Switch. If the EPO option is not used, each unit shall have a unit emergency power off switch readily accessible to the operator. This switch shall provide the same level of control as the supply disconnect switch for the unit.

2.5 Unit Removal. It is possible to physically remove any control unit, I/O device, channel frame, or free-standing storage frame from the system, without affecting the power on the rest of the system, with the following two exceptions:

1. Removing a channel frame physically from the system deactivates all control units and devices controlled from that channel frame, unless they are being shared with other channel frames.
2. Removing a control unit physically from the system deactivates all devices controlled from that control unit, unless they are being shared with other control units. In the case of a shared I/O device, the device is deactivated only if its primary power is supplied through the control unit removed from the system.

2.6 Shared Units.

2.6.1 Shared Units with EPO. When a unit implementing the EPO option is shared between systems, multiple power control interfaces are required, one for each system. Cabling within the unit is as shown in figure 7.

Unit power is brought up when the first system powers up and is dropped when the last system drops power, unless an EPO condition occurs. An EPO condition on both systems causes the attached unit to drop its power.

2.6.2 Shared Units without EPO. When the EPO option is not used and a unit is shared between systems, multiple power control interfaces are required, one for each system. Cabling within the units is shown in figure 8 for two systems sharing a single control unit and in figure 9 a multisystem configuration sharing a single control unit. Unit power is brought up when the first system powers up and is dropped when the last system drops power.

2.7 Multisystem Emergency Power Off. When a system configuration includes more than one CPU and the EPO option is used, interlocking of the EPO circuits of the related CPU's may be desired, EPO interlocking is required when units are shared between the CPU's. This interlocking must be such that an EPO condition detected in one of the CPU's will cause the EPO circuits of all connected CPU's to open, thus dropping power.

Each CPU may then power up after resetting the EPO circuit that caused the overall EPO condition.

To accomplish interlocking, each CPU must provide a multisystem EPO control interface connector and associated circuitry. The interface is shown in figure 10 and a typical implementation is shown in figure 7.

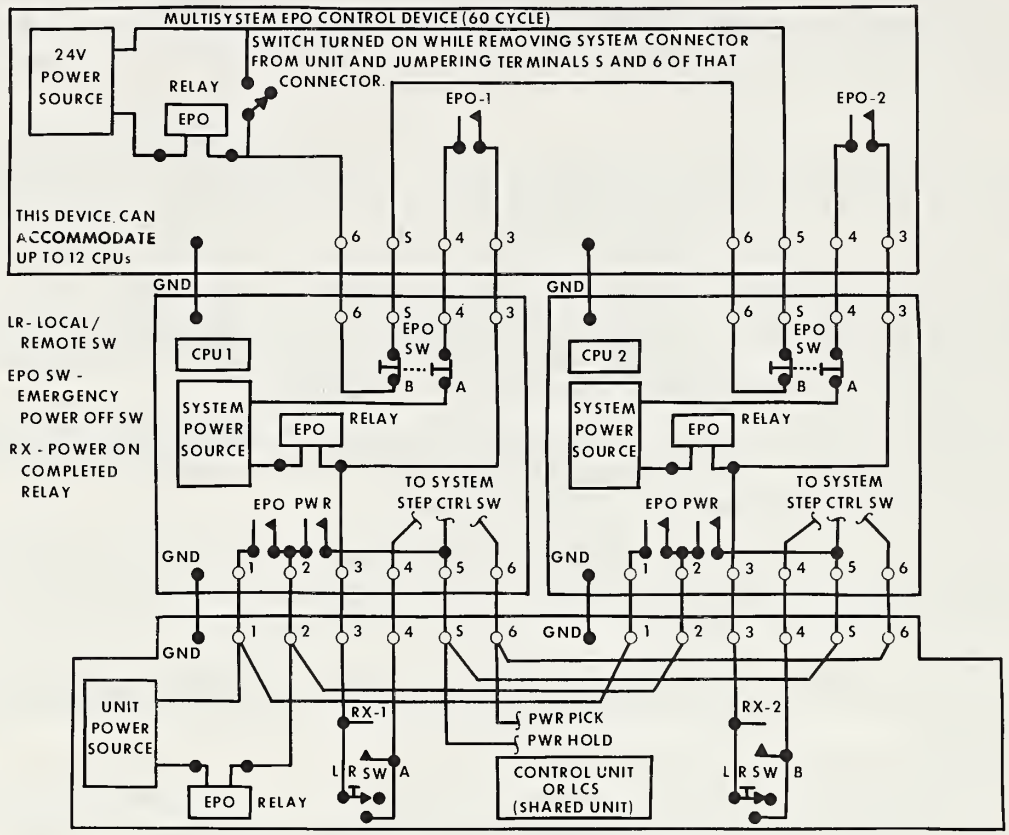


FIGURE 7. Shared unit configuration with EPO option

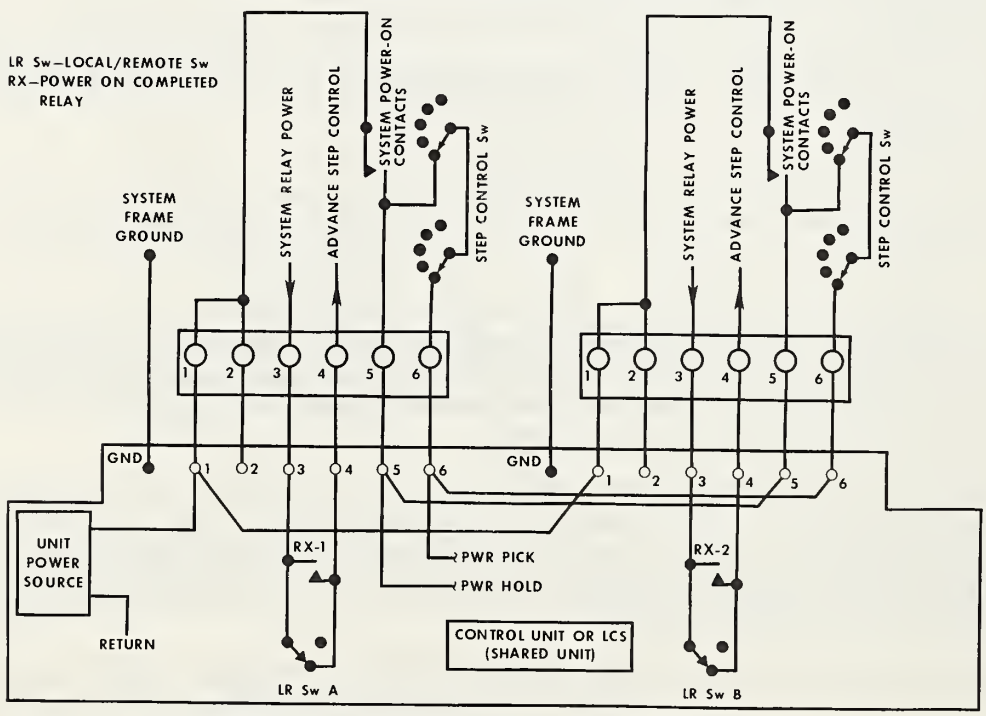


FIGURE 8. Shared unit configuration without EPO option

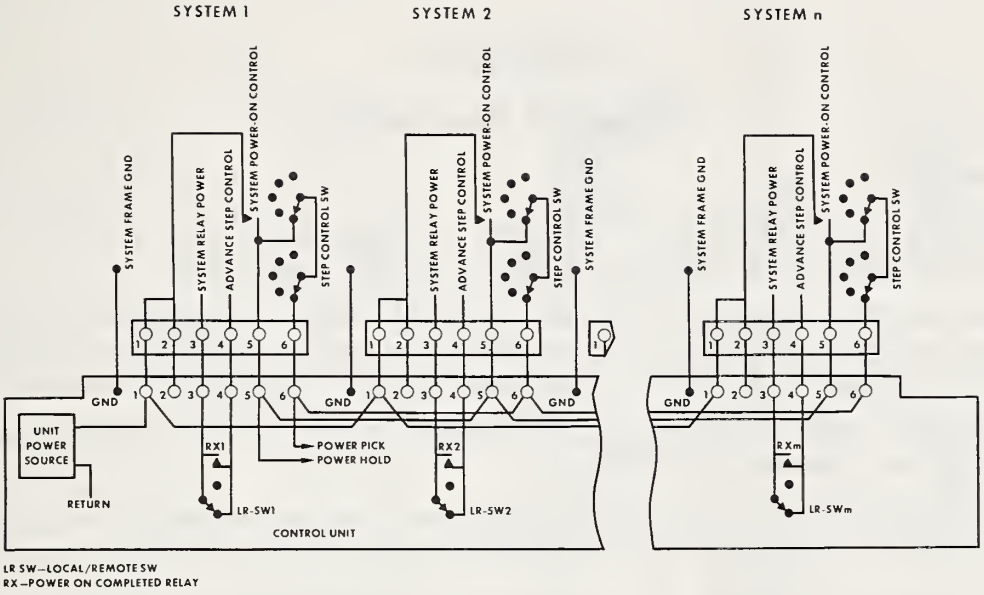


FIGURE 9. Multisystem configuration without EPO option

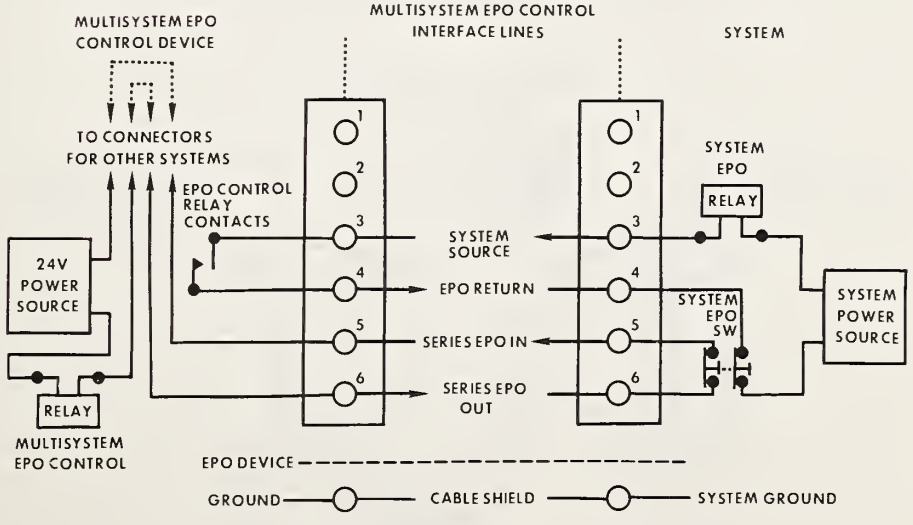


FIGURE 10. Multisystem EPO control interface

CHAPTER 3.

Mechanical Specification

3.1 Interconnection.

3.1.1 Two-System Interconnection. In a system configuration containing only two CPU's, interlocking of the EPO circuits can be accomplished by a single, special cable.

3.1.2 Multisystem Interconnection. When the system configuration includes up to 12 CPU's, the interlocking of the EPO circuits can be accomplished by the multisystem EPO control device shown in figures 7 and 10. This control device continually senses the EPO circuits of all connected CPU's.

The multisystem EPO control device is a self-contained device, which obtains its primary power independently of any of the associated CPU's.

3.2 Dual System EPO Control. Dual systems EPO control can be provided as shown in figure 11. The interlocking of the EPO circuits can be accomplished by a single, special cable.

3.3 Power Cables and Connectors. The maximum cable length shall not exceed 150 feet.

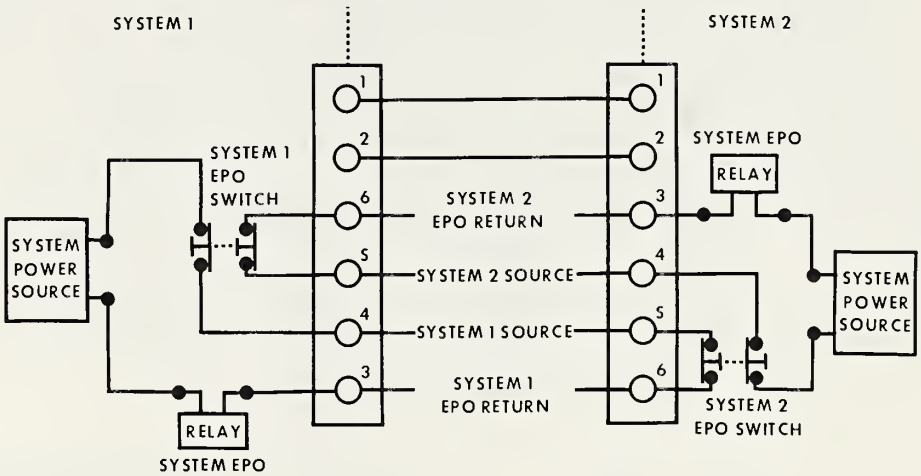


FIGURE 11. Dual system EPO control interface

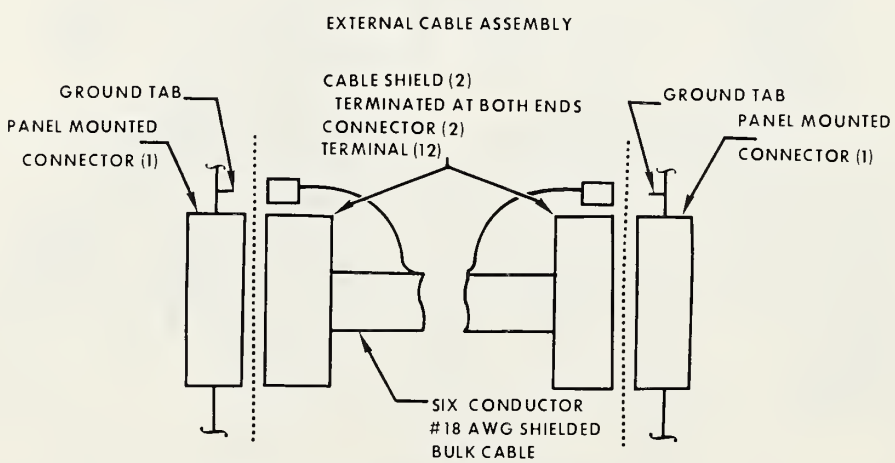


FIGURE 12. Power control and cable connector

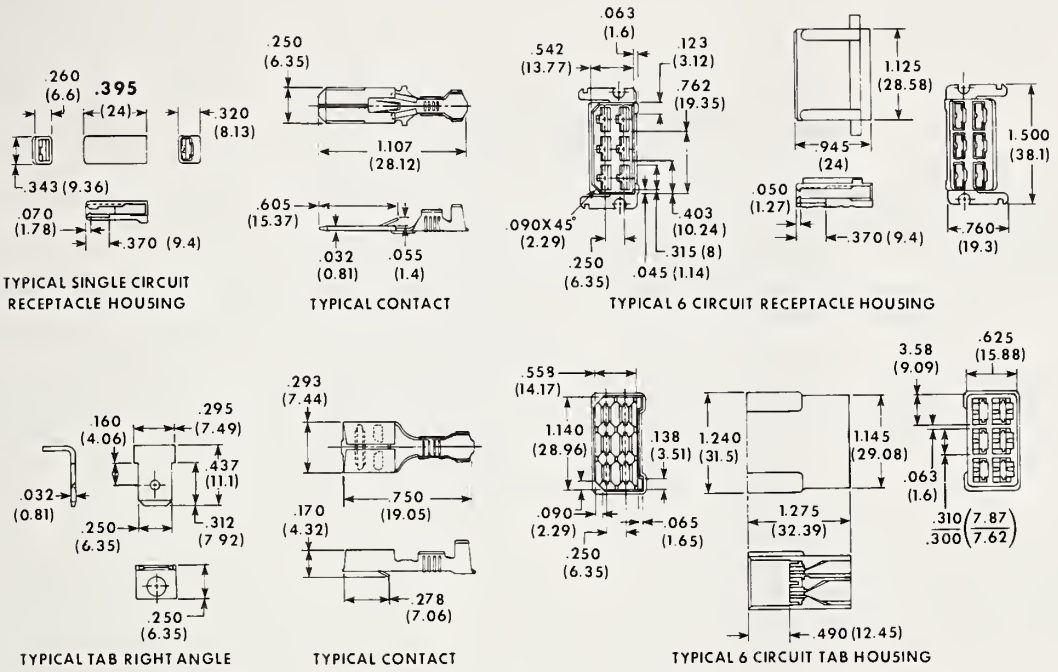


FIGURE 13. Power control connector

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December 18, 1990

National Institute of Standards and Technology

[Docket No. 900101-0219]

RIN 0693-AA59

Approval of Revisions to Federal Information Processing Standards (FIPS) Family of Input/Output Interface Standards

AGENCY: National Institute of Standards and Technology (NIST), Commerce.

ACTION: The purpose of this notice is to announce that the Secretary of Commerce has approved revisions to the Federal Information Processing Standards (FIPS) family of input/output interface standards, and has approved discontinuation of the exclusion and verification lists for these standards.

SUMMARY: On March 20, 1990, notice was published in the Federal Register (55 FR 10272) proposing revision of Federal Information Processing Standards (FIPS) 60-2, 61-1, 62, 63-1, 97, 111, 130, and 131 to make them non-mandatory, and discontinue the exclusion and verification lists for these standards. This proposal superseded the proposal for revision of these standards announced in the Federal Register (52 FR 44462) of November 19, 1987. Procedures for the Exclusion List for FIPS 60, 61, 62, 63, and 97 were published in the Federal Register on

September 3, 1982 (47 FR 38959–38960). Procedures for the Verification List for FIPS 60, 61, 62, 63, and 97 were published in the Federal Register on December 11, 1979 (44 FR 71444–71445) and on April 7, 1981 (46 FR 20719–20720).

The written comments submitted by interested parties and other material available to the Department relevant to these proposed revisions were reviewed by NIST. On the basis of this review, NIST recommended that the Secretary approve revisions to the input/output family of standards and approve discontinuation of the exclusion and verification lists for these standards. NIST prepared a detailed justification document for the Secretary's review in support of those recommendations.

This notice provides only the changes to the revised standards.

EFFECTIVE DATE: These revisions are effective December 18, 1990.

ADDRESSES: Interested parties may obtain copies of FIPS PUBS 60–2, 61–1, 62, 63–1, 97, 111, 130, and 131 from the National Technical Information Service, U.S. Department of Commerce, Springfield, VA 22161.

FOR FURTHER INFORMATION CONTACT: Ms. Shirley Radack, National Institute of Standards and Technology, Gaithersburg, MD 20899, telephone (301) 975–2833.

SUPPLEMENTARY INFORMATION: Under the provisions of 40 U.S.C. 759(d), the Secretary of Commerce is authorized to promulgate standards and guidelines for Federal computer systems, and to make such standards compulsory and binding to the extent to which the Secretary determines necessary to improve the efficiency of operation, or security and privacy of Federal computer systems.

The family of I/O interface standards currently includes:

a. FIPS 60–2, I/O Channel Interface, revised July 29, 1983.

b. FIPS 61–1, Channel Level Power Control Interface, revised July 13, 1982.

c. FIPS 62, Operational Specifications for Magnetic Tape Subsystems, revised December 30, 1980.

d. FIPS 63–1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, revised April 14, 1983; Supplement to FIPS PUB. 63–1, Additional Operational Specifications for Variable Block Rotating Mass Storage Subsystems, April 14, 1983.

e. FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, February 4, 1983.

f. FIPS 111, Storage Module Interfaces (with extensions for enhanced storage module interfaces), April 18, 1985.

g. FIPS 130, Intelligent Peripheral Interface (IPI), July 16, 1987.

h. FIPS 131, Small Computer System Interface (SCSI) July 16, 1987.

The following revisions are being made effective immediately upon publication. A delayed effective date is not required because these standards are exempt from the Administrative Procedure Act by U.S.C. 553(a)(2).

Revisions to Federal Information Processing Standards 60–2, 61–1, 62, 63–1, 97, 111, 130, and 131.

FIPS 60–2, I/O Channel Interface, is revised as follows:

Applicability. This standard addresses the interconnection of computer peripheral equipment as a part of ADP systems for the following types of peripherals: (1) Magnetic tape equipment employing open reel-to-reel magnetic tape storage devices, specifically excluding magnetic tape cassette and tape cartridge storage devices, (2) magnetic disk storage equipment employing disk drives each having a capacity greater than 7 megabytes per storage module, excluding flexible disk and disk cartridge devices having a smaller storage capacity per device, and (3) other peripheral equipment employing peripheral device types for which operational specifications standards have been issued as Federal Information Processing Standards. This standard is recommended for use in the acquisition of peripheral equipment for ADP systems with input/output channel interfaces as specified in the technical specifications, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective December 13, 1979. The first revision became effective June 23, 1980, and the second revision became effective July 29, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 61–1, Channel Level Power Control Interface, is revised as follows:

Applicability. This standard addresses the power control interface in connecting computer peripheral equipment to ADP systems. It is recommended for use when FIPS 60–2 is used, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective June 23, 1980, and the first revision became effective July 13, 1982. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 62, Operational Specifications for Magnetic Tape Subsystems, is revised as follows:

Applicability. This standard addresses magnetic tape equipment connected to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such equipment, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective June 23, 1980. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 63–1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, is revised as follows:

Applicability. This standard addresses peripheral device dependent operational interfaces for connecting variable block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such variable block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. This standard became effective June 23, 1980, and the first revision became effective April 14, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, is revised as follows:

Applicability. This standard addresses the peripheral device dependent operational interface specifications for connecting fixed block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such fixed block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective February 4, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 111, Storage Module Interfaces, is revised as follows:

Applicability. This standard addresses connection of a disk drive to a controller as part of an ADP system. This standard is recommended for use in the acquisition of disk systems that are

connected to small and medium sized computer systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. This standard became effective May 18, 1985. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 130, Intelligent Peripheral Interface (IPI), is revised as follows:

Section 8, Applicability. This standard applies to the connection of computers to storage peripheral device controllers. This standard is recommended for use in the acquisition of magnetic disk drives, optical disk drives, and tape drives to be connected to minicomputer systems, when it is determined that interchange of equipment between different systems is likely.

Section 10, Implementation. This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

Section 11, Waivers. This standard is non-mandatory. No waivers are required.

FIPS 131, Small Computer System Interface (SCSI) is revised as follows:

Section 8, Applicabiiity. This standard addresses the connection of small computers to peripheral devices with integral controllers. This standard is recommended for use in the acquisition of storage peripherals and small computer systems for office or laboratory use, when it is determined that interchange of equipment between different systems is likely.

Section 10, Implementation. This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

Section 11, Waivers. This standard is non-mandatory. No waivers are required.

Dated: December 12, 1990.

John W. Lyons,

Director.

[FR Doc. 90-29563 Filed 12-17-90; 8:45 am]

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