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EIA STANDARD

High Speed 25-Position Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment

EIA-530

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ELECTRONIC INDUSTRIES ASSOCIATION
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EIA-530

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FOREWORD

This foreword is not part of EIA Standard EIA-530 and is included for information purposes only.

This standard has been developed to serve as a complement to EIA-232-D for data rates above 20,000 bits per second. It, together with EIA-422-A and EIA-423-A, provides a convenient means of implementing the higher data rates using the same mechanical connector as specified in EIA-232-D.

It is intended that this standard gradually replace EIA-449 for the higher data rates. It provides, in the Appendix, for interoperability with equipment conforming to EIA-449.

HIGH SPEED 25-POSITION INTERFACE FOR DATA TERMINAL EQUIPMENT AND DATA CIRCUIT-TERMINATING EQUIPMENT

(From Standards Proposal No. 1850, formulated under the cognizance of the EIA Subcommittee TR-30.2 on Data Transmission Interfaces.)

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HIGH SPEED 25-POSITION INTERFACE FOR DATA TERMINAL EQUIPMENT AND DATA CIRCUIT-TERMINATING EQUIPMENT

1. SCOPE

1.1 Section Abstracts

This standard is applicable to the interconnection of data terminal equipment (DTE) and data circuit-terminating equipment (DCE) employing serial binary data interchange with control information exchanged on separate control circuits. It defines:

Section 2 - Signal Characteristics

Section 3 - Interface Mechanical Characteristics

Section 4 - Functional Description of Interchange Circuits

Section 5 - Standard Interfaces for Selected Communication System Configurations

In addition, the standard includes:

Section 6 - Recommendations and Explanatory Notes

Section 7 - Glossary of Terms

1.2 Application

This standard applies where equipment on one side of the DTE/DCE interface is intended for connection directly to equipment on the other side without additional technical considerations. Applications where cable termination, signal waveshaping, interconnection cable distance, and mechanical configurations of the interface must be tailored to meet specific user needs are not precluded but are beyond the scope of this standard.

1.3 Serialization

This standard applies to data communication systems where the data is bit serialized by the DTE and the DCE places no restrictions on the arrangement of the sequence of bits provided by the DTE.

1.4 Signaling Rates

This standard is applicable for use at data signaling rates in the range from 20,000 to a nominal upper limit of 2,000,000 bits per second. Equipment complying with this standard, however, need not operate over this entire data signaling rate range. They may be designed to operate over

a narrower range as appropriate for the specific application.

1.5 Synchronous/Nonsynchronous Communication

This standard applies to both synchronous and nonsynchronous serial binary data communication systems.

1.6 Classes of Service

This standard applies to switched, non-switched, dedicated, leased or private line service, either two-wire or four-wire. Consideration is given to both point-to-point and multipoint operation.

2. SIGNAL CHARACTERISTICS

2.1 Electrical Characteristics

The electrical characteristics of the interchange circuits are specified in the two following standards:

(1) EIA-422-A[1], "Electrical Characteristics of Balanced Voltage Digital Interface Circuits"

(2) EIA-423-A, "Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits"

For the purpose of assigning electrical characteristics, the interchange circuits defined in Section 4.3 are divided into two categories as follows.

2.1.1 Category I Circuits

The following nine interchange circuits are classified as Category I circuits:

Circuit BA (Transmitted Data)
Circuit BB (Received Data)
Circuit DA (Transmit Signal Element Timing, DTE Source)
Circuit DB (Transmit Signal Element Timing, DCE Source)
Circuit DD (Receiver Signal Element Timing, DCE Source)
Circuit CA (Request to Send)
Circuit CB (Clear to Send)
Circuit CF (Received Line Signal Detector)
Circuit CC (DCE Ready)
Circuit CD (DTE Ready)

The individual Category I circuits shall use the balanced electrical characteristics of EIA-422-A. Two leads shall be brought out to the interface connector for each Category I circuit as shown in Figure 2.1(a). Thus, each interchange circuit consists of a pair of wires interconnecting a balanced generator and a differential receiver.

2.1.2 Category II Circuits

The following three interchange circuits are classified as Category II circuits:

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[1] To keep this standard current, the designation "A" is used to indicate the "current level" of the standard so designated.

Circuit LL (Local Loopback)
Circuit RL (Remote Loopback)
Circuit TM (Test Mode)

The Category II circuits shall use the unbalanced electrical characteristics of EIA-423-A. Each Category II interchange circuit consists of one wire interconnecting an unbalanced generator and a differential receiver as shown in Figure 2.1(b). Circuit AB (Signal Ground) is the common return for Category II interchange circuits. The EIA-423-A generators shall employ waveshaping suitable for operation over an interface cable length of at least 60 meters (200 feet), the maximum cable length allowed for nontailored applications (see Section 6.5).

2.2 Protective Ground (Frame Ground)

In DTEs and in DCEs, protective ground is a point which is electrically bonded to equipment frame. It may also be connected to external grounds (e.g., through the third wire of the power cord).

It should be noted that protective ground (frame ground) is not an interchange circuit in this standard. If bonding of the equipment frames of the DCE and the DTE is necessary, a separate conductor should be used which conforms to the appropriate national or local electrical codes. Attention is called to the applicable Underwriters' Laboratories regulation applying to wire size and color coding.

2.3 Shield

In order to facilitate the use of shielded interconnecting cable, interface connector contact number 1 is assigned for this purpose. This will permit the cable associated with the DTE to be composed of tandem connectorized sections with continuity of the shield accomplished by connection through this contact in the connectors. Normally the DCE should make no connection to interface connector contact number 1. It is recognized that for certain electromagnetic interference (EMI) suppression situations, additional provisions may be necessary but are beyond the scope of this standard.

2.4 Grounding

Proper operation of the interchange circuits requires the presence of a path between the DTE circuit ground and the DCE circuit ground. This path is obtained by means of interchange Circuit AB, Signal Ground. Both the DCE and the

DTE normally should have their circuit ground (circuit common) connected to their protective ground (frame ground) through a resistance of 100 ohms (±20%) having a power dissipation rating of one-half watt.

Figure 2.2 illustrates the grounding arrangement.

2.5 "Fail Safe" Operation

2.5.1 The receivers for the following interchange circuits:

Circuit CC (DCE Ready)
Circuit CA (Request to Send)
Circuit CD (DTE Ready)

shall be used to detect a power-off condition in the equipment connected across the interface and the disconnection of the interconnection cable. Detection of either of these conditions shall be interpreted as an OFF condition of the interchange circuit.

2.5.2 The receiver for each control circuit, except those control circuits specified in Section 2.5.1, shall interpret the situation where the conductor is not implemented in the interconnecting cable as an OFF condition.

2.6 General Signal Characteristics

2.6.1 Interchange circuits transferring data signals across the interface point shall hold the marking (binary ONE) and spacing (binary ZERO) conditions for the total nominal duration of each signal element.

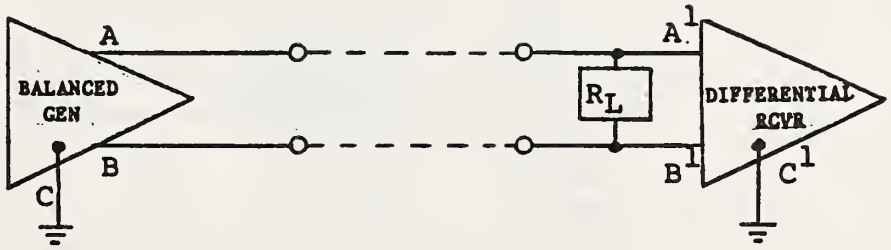
Distortion tolerances for synchronous systems are set forth in EIA-334-A, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission." Standard nomenclature for specifying signal quality for nonsynchronous systems are set forth in EIA-363, "Standard for Specifying Signal Quality for Transmitting and Receiving Data Processing Terminal Equipment Using Serial Data Transmission at the Interface with Non-Synchronous Communication Equipment." Distortion tolerances for nonsynchronous systems are set forth in EIA-404-A, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment."

2.6.2 Interchange circuits transferring timing signals across the interface point shall hold ON and OFF conditions for nominally equal periods of time consistent with acceptable tolerances as specified in EIA-334-A.

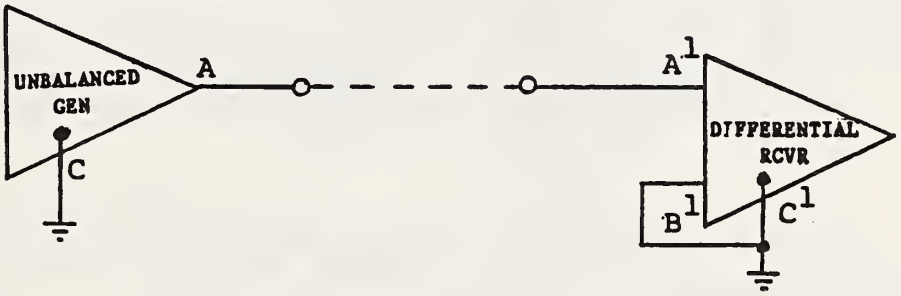
Accuracy and stability of the timing information on Circuit DD (Receiver Signal Element Timing) is required only when Circuit CF (Received Line Signal Detector) is in the ON condition. Drift during the OFF condition of Circuit CF is acceptable; however resynchronization of the timing information on Circuit DD must be accomplished as rapidly as posssible following the OFF to ON transition of Circuit CF.
It is desirable that the transfer of timing information across the interface be provided during all times that the timing source is capable of generating this information (i.e., it should not be restricted only to periods when actual transmission of data is in progress). During periods when timing information is not provided on a timing interchange circuit, the interchange circuit shall be clamped in the OFF condition.

2.6.3 Tolerances on the relationship between data and associated timing signals shall be in accordance with EIA-334-A.

(a) CATEGORY I CIRCUITS



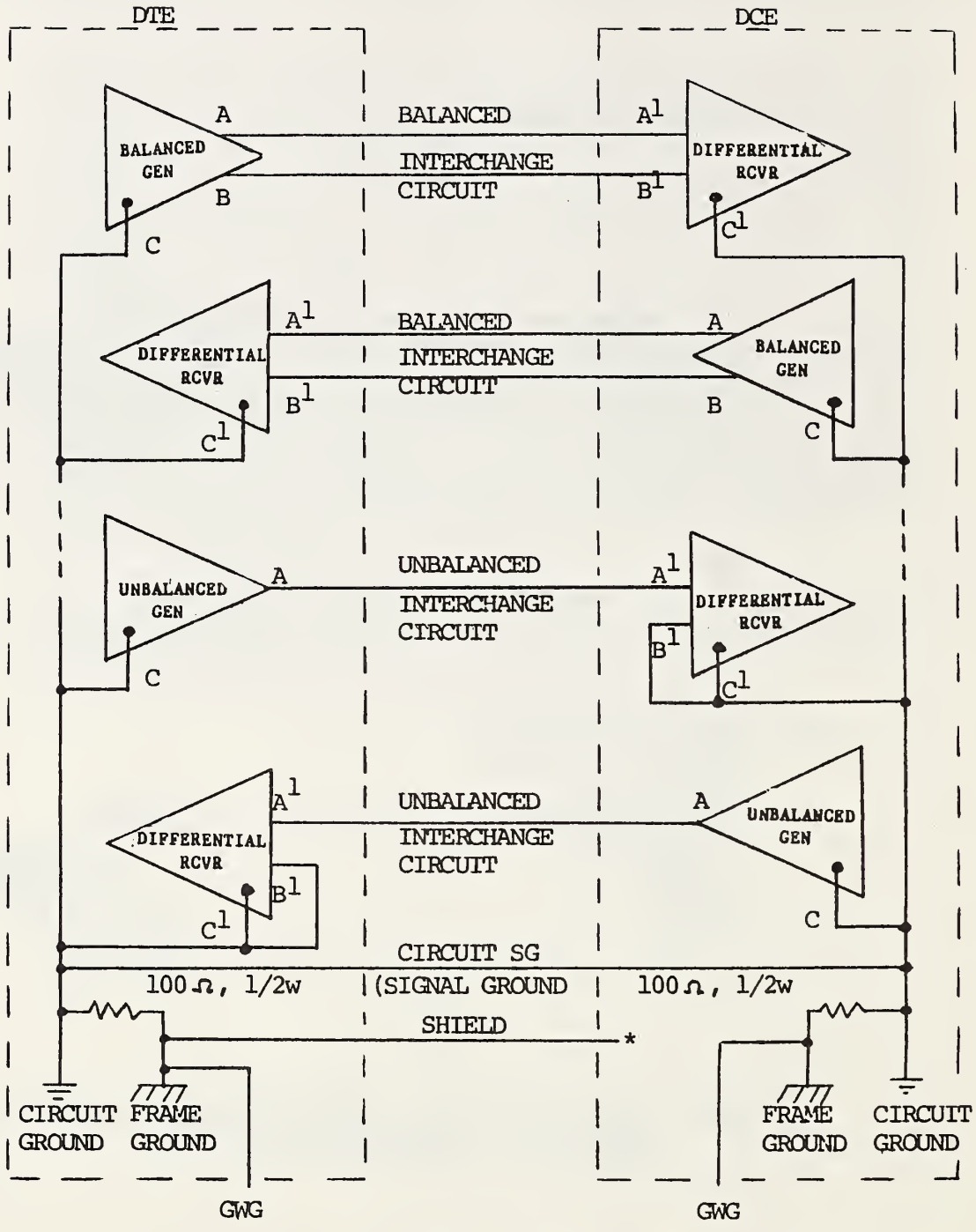
(b) CATEGORY II CIRCUITS



NOTE: The A, A^1, B, B^1, C and C^1 designations are those specified in EIA-422-A and EIA-423-A.

FIGURE 2.1

GENERATOR AND RECEIVER CONNECTIONS AT INTERFACE



NOTES: GWG is green wire ground of power system.

*Normally no connection to shield in DCE (see Section 2.3).

FIGURE 2.2

GROUNDING ARRANGEMENT

3. INTERFACE MECHANICAL CHARACTERISTICSE

3.1 Definition of Mechanical Interface

The point of demarcation between the DTE and the DCE is located at a plugable connector signal interface point between the two equipments which is less than 3 meters (10 feet) from the DCE (see Figure 3.1). A 25-position connector is specified for all interchange circuits.

The DCE shall be provided with the connector as specified in Section 3.3, having female contacts and a male shell. The connector shall be either physically attached to the DCE or extended by means of a short cable (less than 3 meters or 10 feet). The DTE shall be provided with a cable having the connector as specified in Section 3.3, having male contacts and a female shell. The total length of the cable associated with the DTE shall not exceed 60 meters (200 feet) for nontailored applications (see Section 6.10). The mechanical configuration for connections of the interface cable at points other than the point of demarcation is not specified.

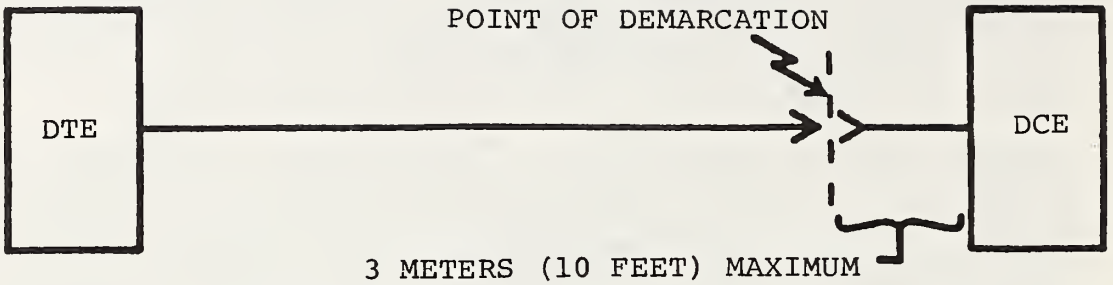
3.2 Intermediate Equipment

When additional functions are provided in a separate unit inserted between the DTE and DCE, the connector with female contacts, as indicated above, shall be associated with the side of this unit which interfaces with the DTE while the cable with the connector with male contacts shall be provided on the side which interfaces with the DCE.

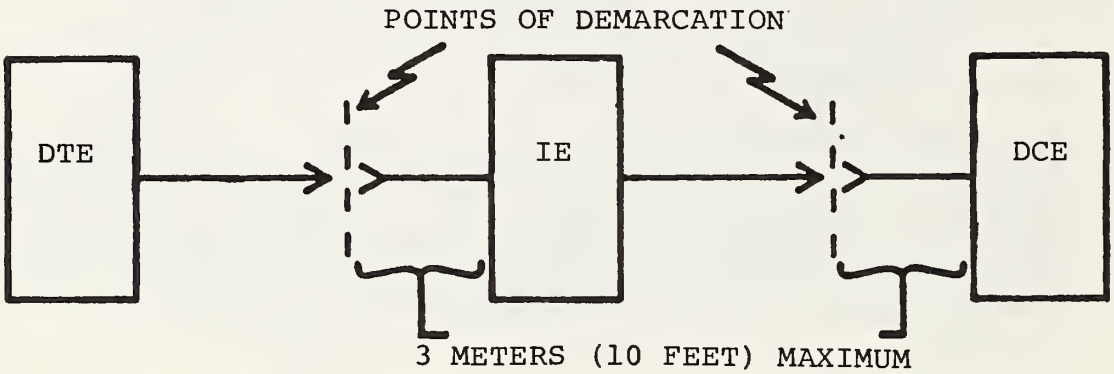
3.3 Interface Connector

3.3.1 Figure 3.2 illustrates the DTE connector which has male (pin) contacts and a female shell (plug connector). Figure 3.3 illustrates the DCE interface connector which has female (socket) contacts and a male shell (receptacle connector). Contact numbering is also illustrated in these Figures. Figures 3.4, 3.5 and 3.6 illustrate contact spacing and dimensions.

3.3.2 Multiple arrangements could be used for fastening the connectors together. No preferred method is recommended.



DTE TO DCE INTERCONNECTION



DTE TO DCE INTERCONNECTION WITH INTERMEDIATE EQUIPMENT

→ CONNECTOR(S) WITH MALE CONTACTS AND FEMALE SHELL

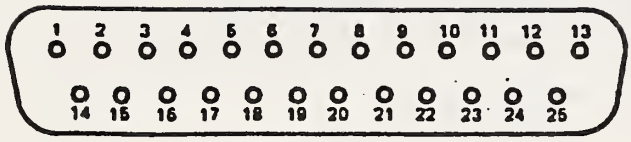
≺ CONNECTOR(S) WITH FEMALE CONTACTS AND MALE SHELL

IE INTERMEDIATE EQUIPMENT

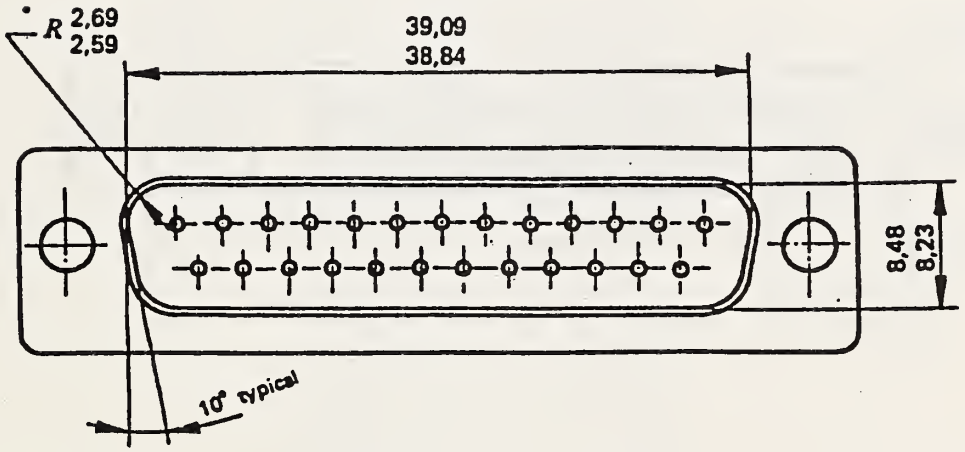
FIGURE 3.1

INTERCONNECTION OF EQUIPMENT

Dimensions in millimetres



DTE connector face
contact numbering



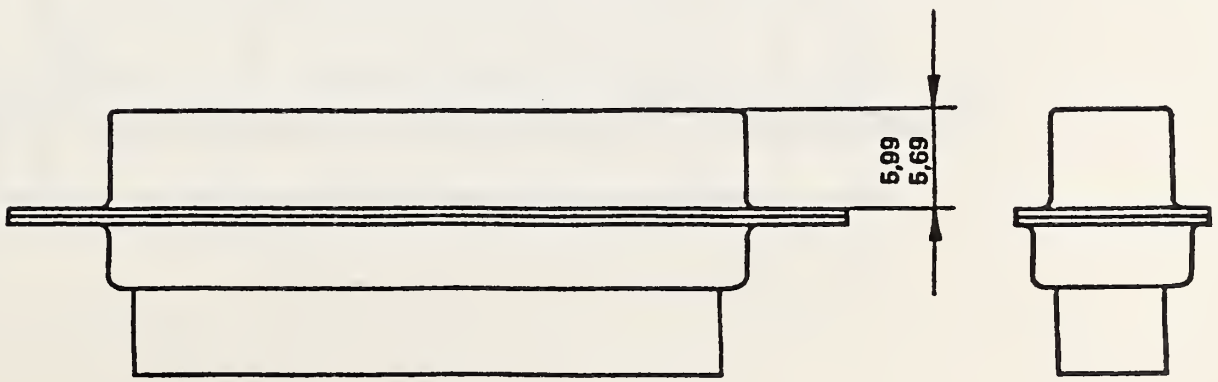
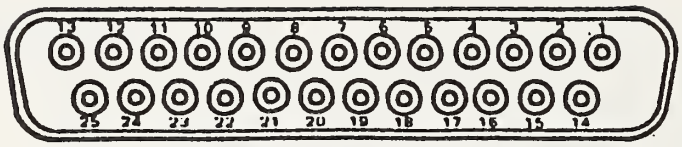
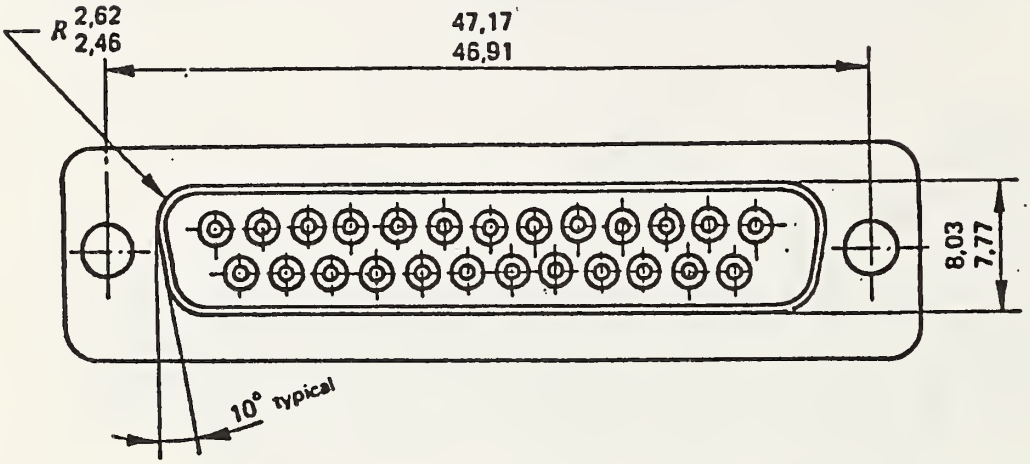


FIGURE 3.2
DTE INTERFACE CONNECTOR

Dimensions in millimetres



DCE connector face
contact numbering



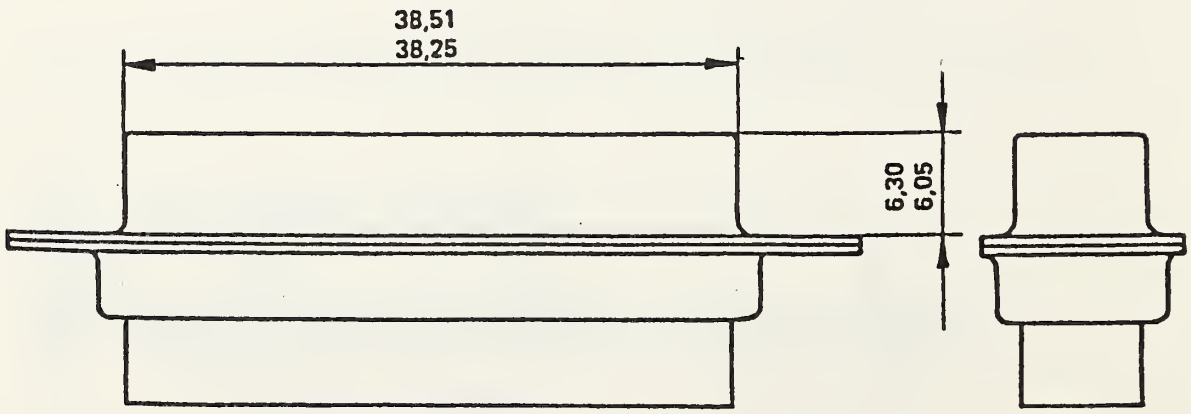


FIGURE 3.3
DCE INTERFACE CONNECTOR

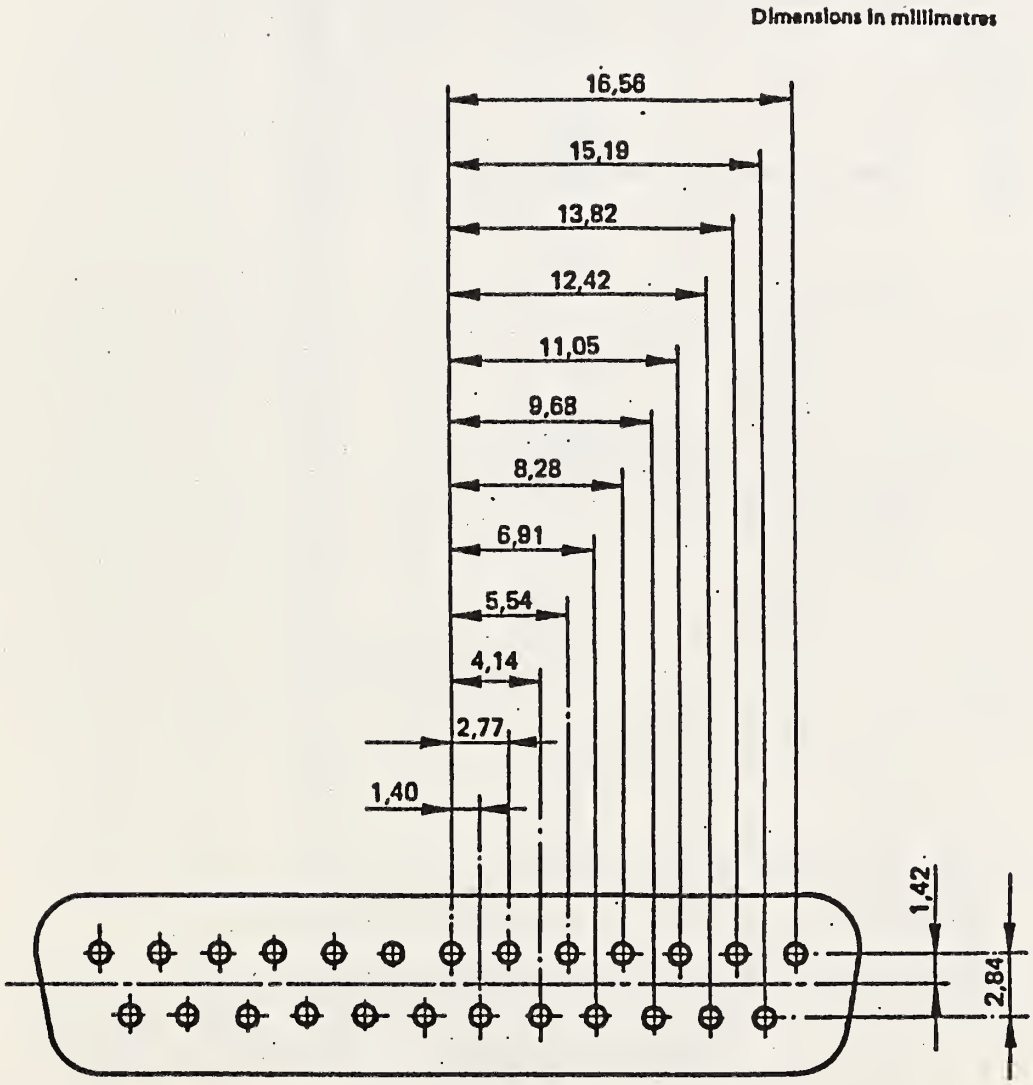


FIGURE 3.4
INSERT DIMENSIONS

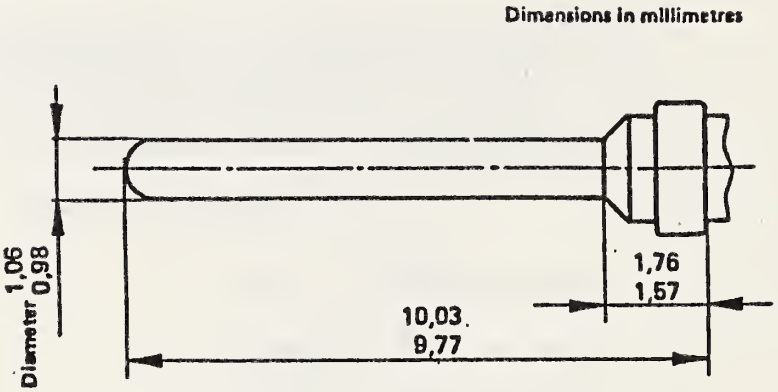
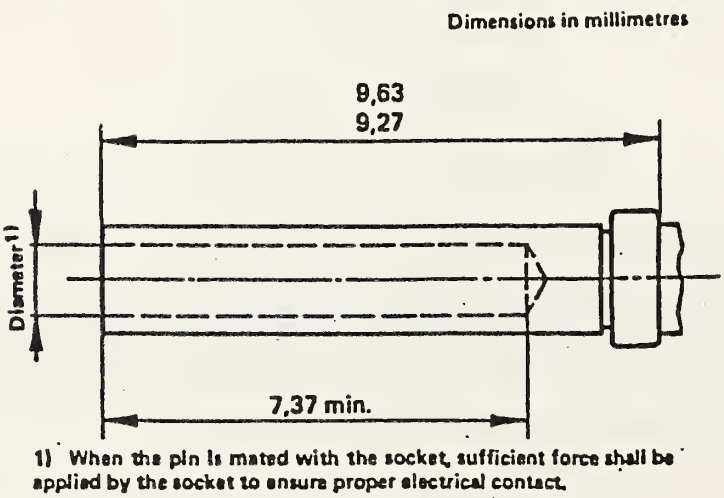


FIGURE 3.5
MALE CONTACT



1) When the pin is mated with the socket, sufficient force shall be applied by the socket to ensure proper electrical contact.

FIGURE 3.6
FEMALE CONTACT

3.4 Connector Contact Assignments

3.4.1 Contact assignments are listed in Figure 3.7.

CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS	CIRCUIT CATEGORY	DIRECTION TO DCE	DIRECTION FROM DCE
1	Shield	-			
2	BA	A-A'	I	X	
3	BB	A-A'	I		X
4	CA	A-A'	I	X	
5	CB	A-A'	I		X
6	CC	A-A'	I		X
7	AB	C-C'	-		
8	CF	A-A'	I		X
9	DD	B-B'	I		X
10	CF	B-B'	I		X
11	DA	B-B'	I	X	
12	DB	B-B'	I		X
13	CB	B-B'	I		X
14	BA	B-B'	I	X	
15	DB	A-A'	I		X
16	BB	B-B'	I		X
17	DD	A-A'	I		X
18	LL	A-A'	II	X	
19	CA	B-B'	I	X	
20	CD	A-A'	I	X	
21	RL	A-A'	II	X	
22	CC	B-B'	I		X
23	CD	B-B'	I	X	
24	DA	A-A'	I	X	
25	TM	A-A'	II		X

NOTE: Interchange Points A-A', B-B' for each Category I circuit should be assigned twisted pairs in interconnecting cables to minimize cross-talk.

FIGURE 3.7 CONNECTOR CONTACT ASSIGNMENTS

4. FUNCTIONAL DESCRIPTION OF INTERCHANGE CIRCUITS

4.1 General

This section defines the basic interchange circuits which apply, collectively, to all systems.

4.2 Classifications of Circuits

CIRCUIT MNEMONIC	CIRCUIT NAME	CIRCUIT DIRECTION	CIRCUIT TYPE
AB	SIGNAL GROUND	-	-
BA	TRANSMITTED DATA	TO DCE	DATA
BB	RECEIVED DATA	FROM DCE	
DA	TRANSMIT SIGNAL ELEMENT TIMING (DTE SOURCE)	TO DCE	TIMING
DB	TRANSMIT SIGNAL ELEMENT TIMING (DCE SOURCE)	FROM DCE	
DD	RECEIVER SIGNAL ELEMENT TIMING (DCE SOURCE)	FROM DCE	
CA	REQUEST TO SEND	TO DCE	CONTROL
CB	CLEAR TO SEND	FROM DCE	
CF	RECEIVED LINE SIGNAL DETECTOR	FROM DCE	
CC	DCE READY	FROM DCE	
CD	DTE READY	TO DCE	
LL	LOCAL LOOPBACK	TO DCE	CONTROL
RL	REMOTE LOOPBACK	TO DCE	
TM	TEST MODE	FROM DCE	

FIGURE 4.1 INTERCHANGE CIRCUITS

Interchange circuits fall into four general classifications:

Ground or Common Return Circuits,
Data Circuits,
Control Circuits, and
Timing Circuits.

A list of interchange circuits showing circuit mnemonic, circuit name, circuit direction, and circuit type is

presented in Figure 4.1.

4.3 Definitions of Interchange Circuits

4.3.1 Circuit AB - Signal Ground

Direction: Not Applicable

This conductor directly connects the DTE circuit ground (circuit common) to the DCE circuit ground (circuit common) to provide a conductive path between the DTE and DCE signal commons (see Section 2.4).

4.3.2 Circuit CC - DCE Ready

Direction: From DCE

Signals on this circuit indicate the status of the local DCE. That is, the local DCE is connected to a communication channel.

This circuit shall be used only to indicate the status of the local DCE. The ON condition shall not be interpreted as either an indication that a communication channel has been established to a remote data station or the status of any remote station equipment.

The OFF condition shall appear at all other times and shall be an indication that the DTE is to disregard signals appearing on all other interchange circuits with the exception of Circuit TM (Test Mode).

Circuit CC shall be held in the OFF condition for DCE tests where testing is not conducted through the DTE/DCE interface. Circuit CC shall respond normally (i.e. not clamped OFF) for DCE tests where testing is conducted through the DTE/DCE interface.

4.3.3 Circuit BA - Transmitted Data

Direction: To DCE

The data signals originated by the DTE, to be transmitted via the data channel to one or more remote data stations, are transferred on this circuit to the DCE.

In all systems, the DTE should hold Circuit BA in

the Binary ONE (marking) condition unless an ON condition is present on all of the following circuits:

1. Circuit CA (Request to Send),
2. Circuit CB (Clear to Send), and
3. Circuit CC (DCE Ready),
4. Circuit CD (DTE Ready).

The DCE shall disregard all signals appearing on Circuit BA during the time that an OFF condition is present on one or more of the above circuits.

All data signals that are transmitted across the interface on Circuit BA during the time an ON condition is maintained on all of the above circuits shall be transmitted to the communication channel by the DCE. The term "data signals" includes the binary ONE (marking) condition, reversals, and sequences such as SYN coded characters to maintain timing synchronization.

4.3.4 Circuit BB - Received Data

Direction: From DCE

The data signals generated by the DCE, in response to data channel line signals received from a remote data station, are transferred on this circuit to the DTE.

Circuit BB shall be held in the binary ONE (marking) condition at all times when Circuit CF (Received Line Signal Detector) is in the OFF condition.

On a half-duplex channel, Circuit BB shall be held in the binary ONE (marking) condition when Circuit CA (Request to Send) is in the ON condition and for a brief interval following the ON to OFF transition of Circuit CA to allow for the completion of transmission (see Circuit BA - Transmitted Data) and the decay of line reflections.

4.3.5 Circuit DA - Transmit Signal Element Timing (DTE Source)

Direction: To DCE

Signals on this circuit provide the DCE with transmit signal element timing information. The ON to OFF transition shall nominally indicate the center of each signal element on Circuit BA (Transmitted Data).

When Circuit DA is implemented in the DTE, the DTE shall normally provide timing information on this circuit whenever the DTE is in a POWER ON condition. It is permissible for the DTE to withhold timing information on this circuit for short periods provided Circuit CA (Request to Send) is in the OFF condition. (For example, the temporary withholding of timing information may be necessary in performing maintenance tests within the DTE).

4.3.6 Circuit DB - Transmit Signal Element Timing (DCE Source)

Direction: From DCE

Signals on this circuit provide the DTE with transmit signal element timing information.

The DTE shall provide a data signal on Circuit BA (Transmitted Data) in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB.

The DCE shall normally provide timing information on this circuit whenever the DCE is in a POWER ON condition. It is permissible for the DCE to withhold timing information on this circuit for short periods provided Circuit CC (DCE Ready) is in the OFF condition. (For example, the withholding of timing information may be necessary in performing maintenance tests within the DCE.)

4.3.7 Circuit DD - Receiver Signal Element Timing (DCE Source)

Direction: From DCE

Signals on this circuit provide the DTE with receive signal element timing information.

The transition from ON to OFF condition shall nominally indicate the center of each signal element on Circuit BB (Received Data).

The DCE shall normally provide timing information on this circuit whenever the DCE in in a POWER ON condition (see Section 2.6.2). It is permissible for the DCE to withhold timing information on this circuit for short periods provided Circuit CC (DCE Ready) is in the OFF condition. (For example, the withholding of timing information may be necessary in performing maintenance tests within the DCE.)

4.3.8 Circuit CA - Request to Send

Direction: To DCE

Signals on this circuit control the data channel transmit function of the local DCE and, on a half-duplex channel, control the direction of data transmission of the local DCE. On one-way only channels or duplex channels, the ON condition maintains the DCE in the transmit mode. The OFF condition maintains the DCE in a non-transmit mode.

On a half-duplex channel, the ON condition maintains the DCE in the transmit mode and inhibits the receive mode. The OFF condition maintains the DCE in the receive mode.

A transition from OFF to ON instructs the DCE to enter the transmit mode (see Section 6.2). The DCE responds by taking such action as may be necessary and indicates completion of such actions by turning ON Circuit CB (Clear to Send), thereby indicating to the DTE that data may be transferred across the interface on Circuit BA (Send Data).

A transition from ON to OFF instructs the DCE to complete the transmission of all data which was previously transferred across the interface on Circuit BA and then assume a non-transmit mode or a receive mode as appropriate. The DCE responds to this instruction by turning OFF Circuit CB when it is prepared to again respond to a subsequent ON condition of Circuit CA.

> NOTE: A non-transmit mode does not imply that all line signals have been removed from the communication channel (see Section 6.2).

When Circuit CA is turned OFF, it shall not be turned ON again until Circuit CB has been turned OFF by the DCE.

An ON condition is required on Circuit CA as well as on Circuit CB, and Circuit CC (DCE Ready), whenever the DTE transfers data across the interface on Circuit BA.

It is permissible to turn Circuit CA ON at any time when Circuit CB is OFF regardless of the condition of any other interchange circuit.

4.3.9 Circuit CB - Clear to Send

Direction: From DCE

Signals on this circuit indicate whether the DCE is conditioned to transmit data on the data channel.

The ON condition together with the ON condition on Circuit CA (Request to Send) and Circuit CC (DCE Ready), is an indication to the DTE that signals presented on Circuit BA (Transmitted Data) will be transmitted to the communication channel.

The OFF condition is an indication to the DTE that it should not transfer data across the interface on Circuit BA since this data will not be transmitted to the line.

The ON condition of Circuit CB is a response to the occurrence of a concurrent ON condition on Circuit CC and Circuit CA, delayed as may be appropriate by the DCE for establishing a data communication channel (including the removal of the mark clamp on Circuit BB of the remote DCE) to a remote DTE.

4.3.10 Circuit CF - Received Line Signal Detector

Direction: From DCE

Signals on this circuit indicate whether the receiver in the DCE is conditioned to receive data signals from the communication channel, but does not indicate the relative quality of the data signals being received.

Circuit CF is not affected by the condition of an equalizer in a DCE.

The ON condition on this circuit is presented when the DCE is receiving a signal which meets its suitablility criteria. These criteria are established by the DCE manufacturer.

The OFF condition indicates that no signal is being received or that the received signal does not meet the suitability criteria established by the DCE manufacturer.

The indications on this circuit shall follow the actual onset or loss of signal by appropriate guard delays.

The OFF condition of Circuit CF shall cause Circuit BB (Received Data) to be clamped to the binary ONE

(marking) condition.

On half-duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following the ON to OFF transition of Circuit CA (see Circuit BB).

4.3.11 Circuit CD - DTE Ready

Direction: To DCE

Signals on this circuit are used to control switching of the DCE to the communication channel. The ON condition prepares the DCE to be connected to the communication channel and maintains the connection established by external means (e.g. manual and automatic call origination and answering).

The OFF condition causes the DCE to be removed from the communication channel following the completion of any "in process" transmission.

4.3.12 Circuit LL - Local Loopback

Direction: To DCE

Signals on this circuit are used to control the LL test condition (see Section 6.3.1) in the local DCE.

The ON condition of Circuit LL causes the DCE to transfer the output of the DCE transmitting signal converter from the communication channel to the receiving signal converter of the same DCE, through such circuitry as may be required for proper operation. After establishing the LL test condition, the DCE turns ON Circuit TM (Test Mode). After Circuit TM is turned ON, the DTE may operate in a duplex mode, exercising all of the circuits in the interface.

The OFF condition of Circuit LL causes the DCE to release the LL test condition.

4.3.13 Circuit RL - Remote Loopback

Direction: To DCE

Signals on this circuit are used to control the RL test condition (see Section 6.3.2) in the remote DCE.

The ON condition of Circuit RL causes the local DCE to signal the establishment of the RL test condition in the remote DCE. After turning ON Circuit RL and detecting an ON condition on Circuit TM (Test Mode), the local DTE may operate in a duplex mode, exercising the circuitry of the local and remote DCEs. The OFF condition of Circuit RL causes the DCE to signal the release of the RL test condition.

Test condition RL places the communication system out of service to the DTE associated with the DCE containing the RL loopback. When RL is activated, the DCE containing the RL loopback shall present an OFF condition on Circuit CC (DCE Ready) and present an ON condition on Circuit TM. If test condtion RL in the remote DCE is activated from the local DCE (by manual means or by means of Circuit RL), the local DCE shall allow Circuit CC to respond normally and shall present an ON condition on Circuit TM.

4.3.14 Circuit TM - Test Mode

Direction: From DCE

Signals on this circuit indicate whether the local DCE is in a test condition.

The ON condition of Circuit TM indicates to the DTE that the DCE has been placed in a test condition. The ON condition of Circuit TM shall be in response to an ON condition of Circuit LL (Local Loopback) or Circuit RL (Remote Loopback) and indicates that the test condition has been established. The ON condition shall also be in response to either local or remote activation by other means of any DCE test condition. Activation of a telecommunications network test condition (e.g., facility loopback) which is known to the DCE shall also cause Circuit TM to assume the ON condition. The OFF condition of Circuit TM indicates that the DCE is not in a test mode and is available for normal service. When testing is conducted through the DTE/DCE interface, Circuit CC (DCE Ready) operates in a normal manner. When testing is not conducted through the DTE/DCE interface, Circuit CC is held in the OFF condition.

5. STANDARD INTERFACES FOR SELECTED COMMUNICATION SYSTEM CONFIGURATIONS

5.1 General

This section describes a selected set of data transmisssion configurations. For each of these configurations a standard set of interchange circuits (defined in Section 4) is listed. (See Section 6.1).

Provision is made for additional data transmission configurations not defined herein. Interchange circuits for these applications must be specified separately, for each application, by the supplier.

5.2 Data Transmission Configurations

Data transmission configurations for which standard sets of interchange circuits are defined are as follows:

Type SR (Send-Receive)
Type SO (Send-Only)
Type RO (Receive-Only)
Type DT (Data and Timing only)

Figure 5.1 lists the interchange circuits to be provided for each data transmission configuration.

5.3 Conditions

For a given interface type, generators and receivers shall be provided for every interchange circuit designated M (mandatory) in Figure 5.1. In addition, generators and receivers shall be provided for interchange circuits designated S and T where the service is switched and synchronous, respectively.

All control interchange circuits listed in Figure 4.1 not provided with an operational generator shall be provided with a dummy generator (see Section 6.4). The dummy generator shall permanently hold the circuits in the OFF condition.

In the interest of minimizing the number of different types of equipment, additional interchange circuits having operational generators or receivers may be included in the design of a general unit capable of satisfying the requirements of several different applications. Where operational generators or receivers not on the standard list are provided for a given configuration, the designer of this equipment must be prepared to find an open circuit on the other side of the interface, and the system shall not suffer

degradation of the basic service.

INTERCHANGE CIRCUIT		CONFIGURATION			
	TYPE SR	TYPE SO	TYPE RO	TYPE DT
AB	SIGNAL GROUND	M	M	M	M
BA	TRANSMITTED DATA	M	M		M
BB	RECEIVED DATA	M		M	M
DA	TRANSMIT SIGNAL ELEMENT TIMING (DTE SOURCE)	O	O		O
DB	TRANSMIT SIGNAL ELEMENT TIMING (DCE SOURCE)	T	T		T
DD	RECEIVER SIGNAL ELEMENT TIMING (DCE SOURCE)	T		T	T
CA	REQUEST TO SEND	M	M		
CB	CLEAR TO SEND	M	M		
CF	RECEIVED LINE SIGNAL DETECTOR	M		M	
CC	DCE READY	M	M	M	
CD	DTE READY	S	S	S	
LL	LOCAL LOOPBACK	O			
RL	REMOTE LOOPBACK	O			
TM	TEST MODE	M	M	M	

M = Mandatory interchange circuits for a given configuration.
T = Additional interchange circuits required for synchronous operation.
S = Additional interchange circuit required for switched service.
O = Optional interchange circuits.

FIGURE 5.1

STANDARD INTERFACES FOR SELECTED COMMUNICATION SYSTEM CONFIGURATIONS

6. RECOMMENDATIONS AND EXPLANATORY NOTES

6.1 Alternate Use of Communication Service

The control interchange circuits at the interface point are arranged to permit the alternate use of communication service as follows:

a. A DTE designed for Transmit-Only or Receive-Only operation may also use either Half-Duplex or Duplex service.

b. A DTE designed for Half-Duplex operation may also use Duplex service.

6.2 Line Signals

The turning ON of Circuit CA (Request to Send) does not necessarily imply the turning ON of a line signal on the communication channel. Some DCEs might not have a line signal as it is understood in this standard, e.g. the signal can be a modified digital base-band signal.

Conversely, in DCEs which do not transmit a "line signal", the turning OFF of Circuit CA does not necessarily command the removal of that line signal from the communication channel. On a duplex channel, the DCE might autonomously transmit a training signal to hold AGC circuits or automatic equalizers in adjustment, or to keep timing locked (synchronized) when Circuit CA is OFF.

It is not within the scope of this standard to specify in detail what occurs on the communication channel (line) side of the DCE. Therefore, the definition for Circuit CA uses the terminology "assume the transmit mode" intentionally avoiding reference to "carrier" or "line signals".

However, the requirement for multipoint systems is recognized. DCEs intended for this type of operation should permit the sharing of a communication channel by more than one transmitter and should, when in a non-transmit mode, place no signal on the communication channel which might interfere with the transmission from another DCE in the network.

6.3 Use of Circuits for Testing

A group of three interchange circuits are defined to permit fault isolation testing to be done under control of the DTE. The three circuits are:

Circuit LL (Local Loopback),
Circuit RL (Remote Loopback), and
Circuit TM (Test Mode).

The test control (Circuit LL and Circuit RL) and status (Circuit TM) circuits are considered a desirable step toward a uniform methodology for fault isolation. These circuits will assist the user of DTEs and DCEs in identifying the defective system unit.

Figure 6.1 illustrates the local loopback (LL) and remote loopback (RL) tests as seen from the local DTE. A symmetrical set of loopback tests could exist as seen from the remote DTE.

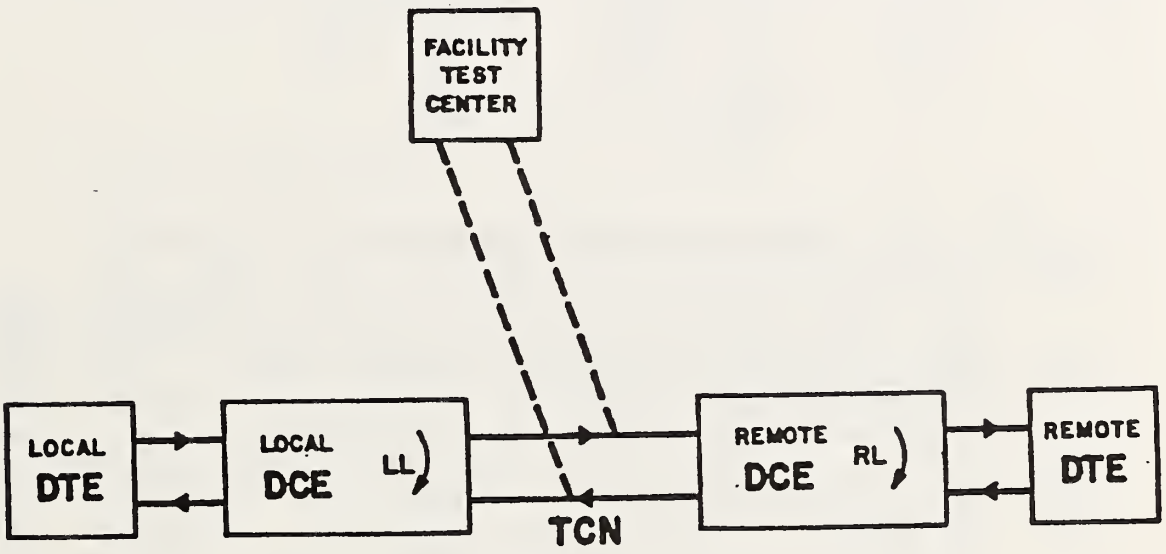


FIGURE 6.1 ILLUSTRATIVE SYSTEM

6.3.1 Local Loopback (LL Test)

This test condition provides a means whereby a DTE may check the functioning of the DTE/DCE interface and the transmit and receive sections of the local DCE. The local DCE also may be tested with a test set in place of the DTE. In the LL test, the output of the transmitting section of the DCE is returned to the receiving section of the DCE, through such

circuitry as may be required for proper operation. In many DCEs the transmitted signal is not suitable for direct connection to the receiver. In such cases it is preferable to include appropriate signal shaping or conversion in the loop-around circuitry so that all elements used in normal operation are checked in the test condition. In the LL test, the communication channel is electrically disconnected from the signal processing circuits of the DCE and terminated as appropriate.

The condition of various interchange control circuits at the local DTE/DCE interface during a local loopback (LL) test condition is summarized in the following table:

Interchange Circuit	Condition
CC	ON
LL	ON
RL	OFF
TM	ON

6.3.2 Remote Loopback (RL Test)

This test condition provides a means whereby a DTE or a facility test center may check the transmission path up to and through the remote DCE to the DTE interface and the similar return transmission path. In this test, Circuit BA (Transmitted Data) and Circuit BB (Received Data) are disconnected or isolated from the remote DTE at the interface and connected to each other in the remote DCE. In synchronous DCEs, arrangements may be required to provide a suitable transmit clock when the RL test condition is activated, and in some instances buffer storage between Circuit BB and Circuit BA may be required.

Remote control of the RL test at the distant DCE through the local DTE/DCE interface is highly desirable to permit automation of the end-to-end testing of a circuit from a central site. Test control is suitable primarily in point-to-point applications but could be used in multipoint configurations with the addition of an address detection capability in the DCE. This test permits circuit verification without the aid of the distant DTE and is supported by inherent remote loopback capability in many present-day DCEs.

Test RL and test LL cannot be performed simultaneously. Consequently, the ON states of

Circuit RL (Remote Loopback) and Circuit LL (Local Loopback) are mutually exclusive.
Circuit RL implies that the remote DCE be signaled from the local DCE to activate the RL test condition. Since such control is effected over the communication channel, appropriate measures must be taken to guard against false operation by data or noise.

The condition of various interchange control circuits at the local and remote DTE/DCE interfaces during a remote loopback (RL) test condition is summarized in the following table:

Interchange Circuit	Local Interface	Remote Interface
CC	ON	OFF
LL	OFF	OFF
RL	ON	OFF
TM	ON	ON

6.3.3 Test Mode

Circuit TM provides the indication from the DCE to the DTE that the DCE is in a test condition. This circuit:

(1) Provides electrical indication that the DCE is in a test condition either in response to control from the DTE or in response to any other action (e.g., telecommunication network initiated testing or manually controlled DCE testing).

(2) Provides action-reaction type control across the interface which verifies completion of requested action.

(3) Permits Circuit CC (DCE Ready) to function normally during test modes where testing is conducted through the DTE/DCE interface and prevents any ambiguity between testing and other modes when Circuit CC is in the OFF condition.

6.4 Dummy Generator

At the interface connector, it is necessary that a voltage be present, from either an operational generator or a dummy

generator, for every control interchange listed below.

DTE CONTROL INTERCHANGE CIRCUIT GENERATORS		DCE CONTROL INTERCHANGE CIRCUIT GENERATORS	
CA	Request to Send	CC	DCE Ready
LL	Local Loopback	CB	Clear to Send
RL	Remote Loopback	CF	Received Line Signal Detector
CD	DTE Ready	TM	Test Mode

A dummy generator shall meet the open-circuit, test termination and short-circuit generator requirements of EIA-422-A or EIA-423-A, as appropriate. A dummy generator satisfying these requirements may be implemented with a 2-watt resistor of 47 ohms (±5%) connected to a dc source voltage between 4 and 6 volts. If a dummy generator is used on one or more of the following interchange circuits:

Circuit CC (DCE Ready),
Circuit CD (DTE Ready), and
Circuit CA (Request to Send),

It shall also meet the generator power-off requirement of EIA-422-A or EIA-423-A, as appropriate.

A single dummy generator may be employed to supply the signal to more than one interchange circuit. Therefore, only two dummy generators are required when both ON and OFF circuit conditions are to be provided.

It is not necessary for the interface cable associated with the DTE to provide separate conductors for each interchange circuit requiring a dummy generator. Instead, two conductors may be employed in the interface cable, one connected to a positive voltage dummy generator in the DTE and the other connected to a negative voltage dummy generator in the DTE. At the interface connector, these two conductors are connected to multiple connector contacts, as appropriate.

6.5 Relationship Between Signaling Rate, Signal Risetime and Interface Cable Distance

The relationship between signaling rate and interface cable distance for balanced interchange circuits is specified in EIA-422-A. Using the guidelines of EIA-422-A, operation over 60 meters (200 feet) of cable limits the maximum signaling rate of balanced interchange circuits to 2,000,000 bits per second. Timing signals, which operate at twice the signaling rate of data signals, may be up to 4,000,000 bits per second. Operation over cable distances greater than 60 meters (200 feet) can be accomplished, in many cases, but is

considered a tailored application.

Additional guidance is provided in EIA-422-A.

6.6 Cautionary Note

The connector used in this recommendation, is also used for EIA-232-D, which employs electrical characteristics that, if improperly connected to some silicon devices designed to meet the EIA-422-A and EIA-423-A electrical characteristics specified in this recommendation, could damage those devices.

7. GLOSSARY OF TERMS

This section defines terms used in this standard.

7.1 Data Transmission Channel

The transmission media and intervening equipment involved in the transfer of information between DTEs. A data transmission channel includes the signal conversion equipment. A data transmission channel may support the transfer of information in one direction only, in either direction alternately, or in both directions simultaneously and the channel is accordingly classified as defined in the following sections.

7.2 One Way Only (Unidirectional) Channel

A channel capable of operation in only one direction. The direction is fixed and cannot be reversed.

7.3 Half-Duplex Channel

A channel capable of operating in both directions but not simultaneously. The direction of transmission is reversible.

7.4 Duplex Channel (Full-Duplex Channel)

A channel capable of operating in both directions simultaneously.

7.5 Synchronous Data Transmission Channel

A data channel in which timing information is transferred between the DTE and the DCE. Transmit timing signals can be provided by either the DTE or by the DCE. Receive timing is provided by the DCE. A synchronous data channel will not accommodate Start/Stop data signals at the same data signaling rate unless the time intervals separating successive significant instants are whole multiples of a unit interval (i.e., signals are transmitted isochronously) and timing signals are interchanged at least at the transmitting station.

7.6 Nonsynchronous Data Transmission Channel

A data channel in which no separate timing information is transferred between the DTE and the DCE.

7.7 Dedicated Line

A communication channel which is nonswitched, i.e., which is permanently connected between two or more data stations. These communication channels are also referred to as "leased" or "private"; however, since leased and private switched networks do exist, the term "dedicated" is preferred herein to define a nonswitched connection between two or more stations.

7.8 Interchange Circuit

A circuit between the DTE and the DCE for the purpose of exchanging data, control or timing signals or for use as a ground or common return.

7.9 Generator

The electronic circuitry at the transmitting end (source) of an interchange circuit which converts binary digital signals to signals having the required electrical characteristics for transmission over the interchange circuit.

7.10 Receiver

The electronic circuitry at the receiving end (sink) of an interchange circuit which converts signals received from the interchange circuit to binary digital signals.

7.11 Signal Conversion Equipment

Those portions of the DCE which transform (e.g., modulate, shape, etc.) the data signals exchanged across the interface into signals suitable for transmission through the associated communication media or which transform (e.g., demodulate, slice, regenerate, etc.) the received line signals into data signals suitable for presentation to the DTE.

APPENDIX

INTERCONNECTING EIA - 530

WITH EIA-449

This interface may be easily interconnected with equipments using EIA-449. This may be via a connecting cable or other connecting device. The following table lists the Circuit Name and Mnemonic, and connector contact pin for each interface:

EIA-530			EIA-RS-449	
CIRCUIT, NAME, AND MNEMONIC		CONTACT	CONTACT	CIRCUIT, NAME, AND MNEMONIC
Shield	---	1	1	Shield
Transmitted Data	BA (A) BA (B)	2 14	4 22	SD (A) Send Data SD (B)
Received Data	BB (A) BB (B)	3 16	6 24	RD (A) Receive Data RD (B)
Request To Send	CA (A) CA (B)	4 19	7 25	RS (A) Request to Send RS (B)
Clear To Send	CB (A) CB (B)	5 13	9 27	CS (A) Clear to Send CS (B)
DCE Ready	CC (A) CC (B)	6 22	11 29	DM (A) Data Mode DM (B)
DTE Ready	CD (A) CD (B)	20 23	12 30	TR (A) Terminal Ready TR (B)
Signal Ground	AB	7	19	SG Signal Ground
Received Line Signal Detector	CF (A) CF (B)	8 10	13 31	RR (A) Receiver Ready RR (B)
Transmit Signal Element Timing (DCE Source)	DB (A) DB (B)	15 12	5 23	ST (A) Send Timing ST (B)
Receiver Signal Element Timing (DCE Source)	DD (A) DD (B)	17 9	8 26	RT (A) Receive Timing RT (B)
Local Loopback	LL	18	10	LL Local Loopback
Remote Loopback	RL	21	14	RL Remote Loopback
Transmit Signal Element Timing (DTE Source)	DA (A) DA (B)	24 11	17 35	TT (A) Terminal Timing TT (B)
Test Mode	TM	25	18	TM Test Mode

ANNEX A

Diagrams for finger clearance

(This annex provides additional information and does not form an integral part of the recommendation.)

This annex provides guidance on finger clearance for equipment designers.

Figure A1 shows the maximum DTE connector outline.

Figure A2 shows the minimum DCE connector spacing for the multiple interface arrangement, taking into account the various fastening devices (levers, screws, etc.) of DTE connectors.

Dimensions in millimeters

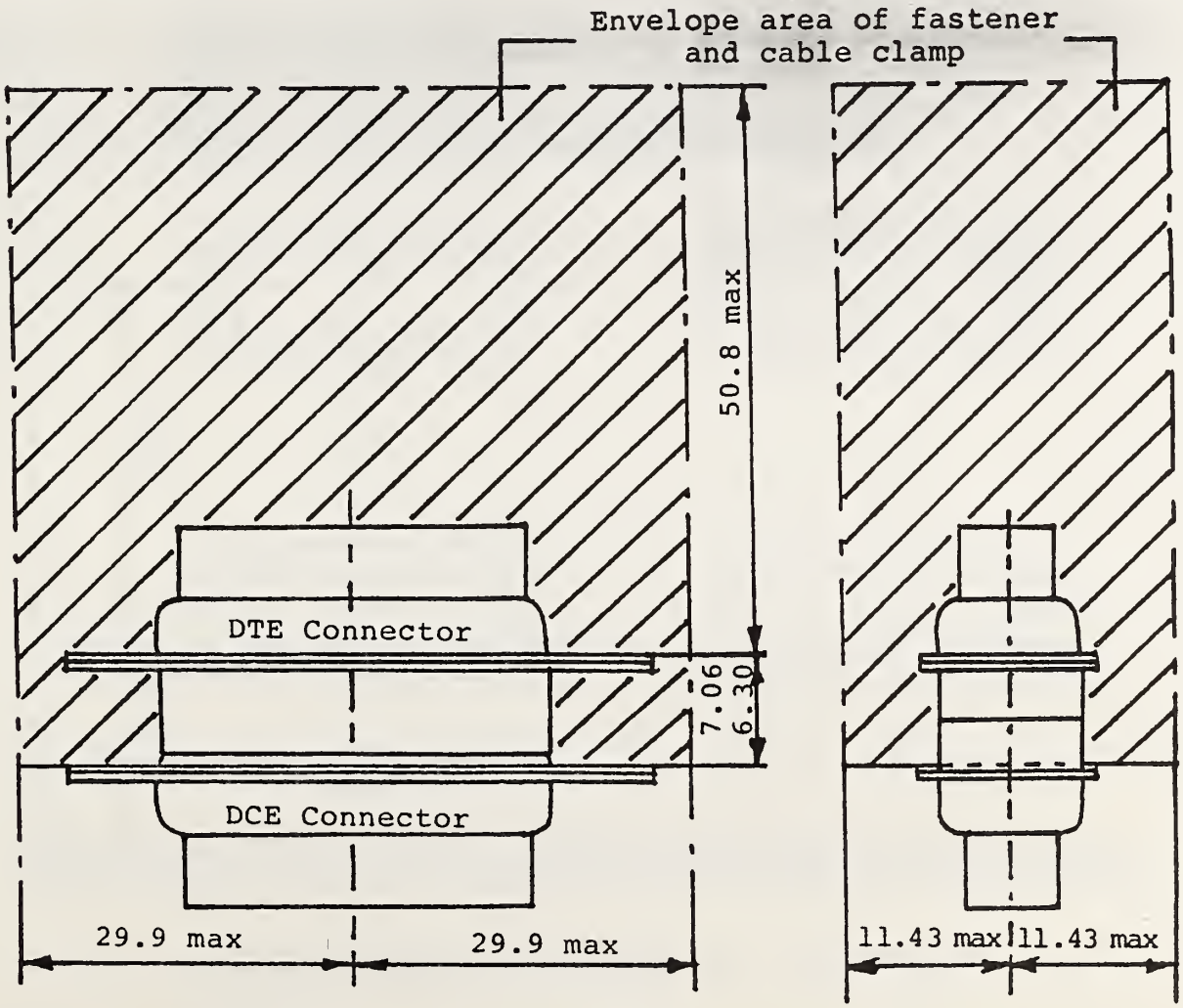


FIGURE A1 - MAXIMUM DTE CONNECTOR OUTLINE

Dimensions in millimeters

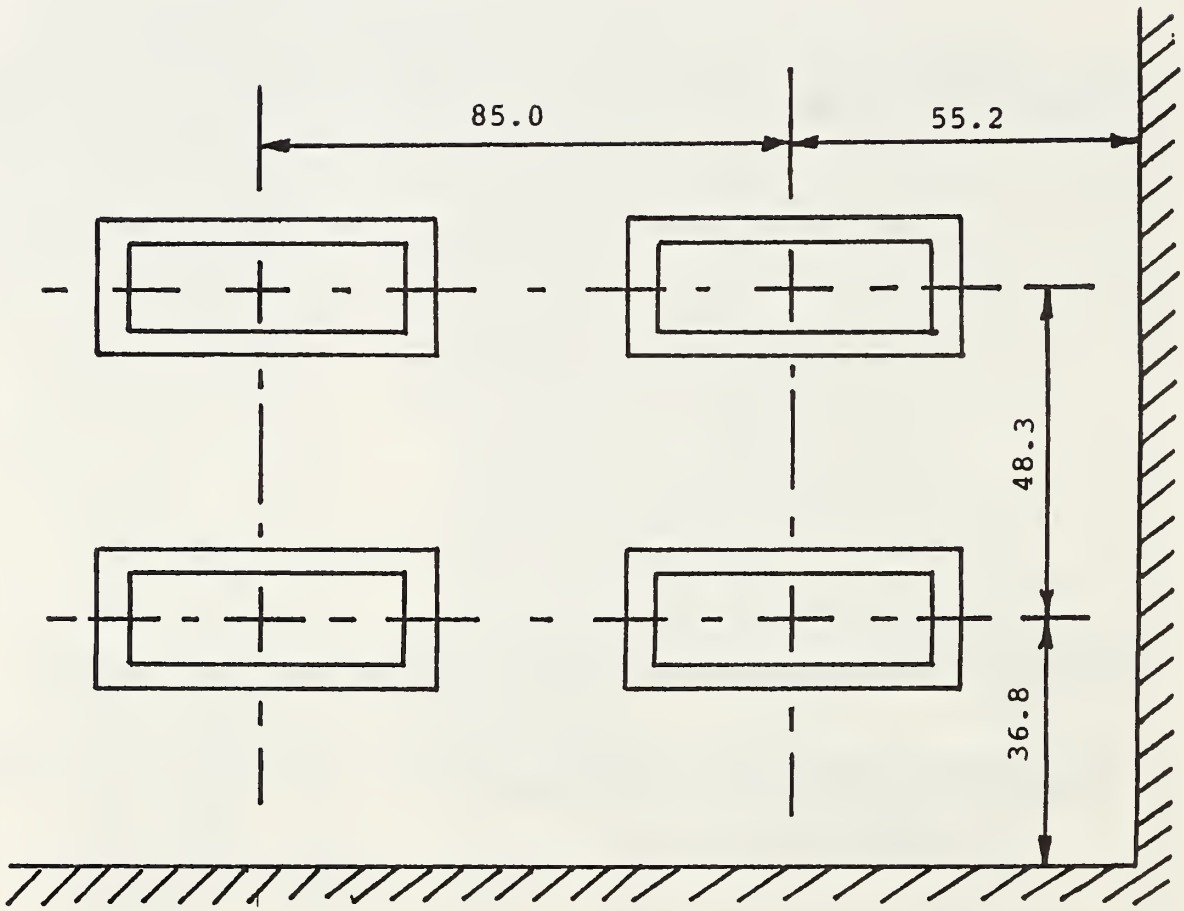


FIGURE A2 - MINIMUM DCE CONNECTOR SPACING

This standard has been adopted for Federal Government use.

Details concerning its use within the Federal Government are contained in Federal Information Processing Standards Publication 154, High Speed 25-Position Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment. For a complete list of the publications available in the Federal Information Processing Standards Series, write to the Standards Processing Coordinator (ADP), National Institute of Standards and Technology, Gaithersburg, MD 20899.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