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Detection of Deep Levels in High Power Semiconductor Materials and Devices*

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TSM and other deep level measurement techniques are used to detect, characterize, and identify deep level defects which control lifetime and leakage in semiconductor devices. These measurements are performed on an apparatus which is capable of handling full-sized wafers as well as die-sized devices. Measurements of "wafer maps" of the gold acceptor defect density in silicon reveal inhomogeneity in the defect distribution which is directly reflected in the leakage current distribution. The wafer handling capabilities make this apparatus a useful extension of routine fabrication-line diagnostic tools.

Key Words: Deep level measurements; defect distribution; power semiconductor materials; power thyristors; semiconductor measurements; thermally stimulated measurements.

1. Introduction

The measurement of deep levels in semiconductors, particularly in application to power devices, stems from two related aspects: (1) detection, identification, and control of unwanted intrinsic or process-induced impurities or defects; and (2) characterization and control of specifically introduced defects for lifetime control. The capability for the performance of the measurements and the analysis of the data have heretofore been primarily confined to laboratory studies of packaged devices. The deep level program in the National Bureau of Standards Semiconductor Technology Program (NBS-STP) is aimed at the utilization of these measurement techniques as routine diagnostic tools on wafers in the fabrication area as well as a research tool in the laboratory. The program has centered its attention on three efforts designed to implement this objective:

1. Develop processes for fabricating test structures on starting material and diffused wafers for use with deep level techniques.
2. Develop measurement methods to routinely execute deep level measurements and develop methods for analyzing the measured data to yield parameters such as energy level, emission rate, and density of defects.
3. Develop apparatus to allow deep level defect measurements on full wafers.

Deep level measurements in silicon can and do take a number of forms. In particular, such techniques as deep level transient spectroscopy (DLTS) [1][1] and thermally stimulated current and capacitance measurements (TSM) [2] are well suited for this purpose since they detect electrically active defects in the depletion region of active devices. Basically, these techniques utilize the ability of defects to emit trapped carriers after receiving sufficient thermal energy. In the thermally stimulated current measurement, the emission of carriers from the defect is detected as a flow of current through the device. For DLTS and the thermally stimulated capacitance measurement, the change in capacitance, which accompanies the slight collapse of the depletion region with emission of charge, is detected. DLTS typically uses *pn* junction devices [1], whereas either MOS capacitors or *pn* junctions are used for TSM [3]. Both methods require temperature manipulation of the device-under-test, and both techniques can yield the energy level, emission rate, and density of defects.

2. Fabrication of Test Structures

During the fabrication of high power thyristors, the wafer is subjected to a number of high temperature treatments to form the necessary *npnp* structure. This processing causes the lifetime of the starting material to degrade several orders of magnitude (ms to μs) due to the introduction or activation of unwanted defect centers. A gettering step is often used to recover some of the lifetime to a level where specific defects can be introduced to tailor the final properties of the device.

Deep level measurement techniques could be used at appropriate points during the fabrication of the device in order to monitor the presence of electrically active defects. However, it is necessary to have appropriate test structures fabricated on the starting or processed wafer to allow the measurement to be made.

For the study of defects in starting material, an ideal test vehicle for TSM is the MOS capacitor fabricated using relatively low temperature processes. Low temperatures are preferred to avoid the possibility of altering the "starting" character of the wafer as a result of test device fabrication. A process suitable for fabricating MOS capacitors on starting wafers is shown in table 1. Additional details are given elsewhere [4]. Thermally stimulated current and capacitance measurements on MOS capacitors fabricated in this way have

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[1] Figures in brackets indicate literature references at the end of this paper.

been successful in detecting the gold defect which was purposely introduced into a starting wafer. As a diagnostic tool, this test structure would be useful for screening starting material for acceptance, or to determine what intrinsic defects are present in starting material before the fabrication procedure.

TABLE 1. *Basic processing steps for MOS capacitors using low temperature fabrication procedures*

1. Wafer Clean-up
2. Chemical Vapor Deposited SiO_2 (400 °C)
3. Gate Metal Application and Definition
4. Back Side Metallization
5. Microalloy of Metallization (400 °C)

Deep level diagnostic measurements applied to in-process wafers could essentially provide "on-line" information regarding the presence of defects to the process engineer. Typically, the most severe processing step during the fabrication of a high power thyristor is the first high-temperature, long-term diffusion to form the basic *pnp* structure. This diffusion step activates or introduces unwanted defects which control the minority carrier lifetime. The ability to perform a deep level measurement on the wafer after the first diffusion would provide valuable input to both the process engineer and the device designer. Information such as the identity, density, and distribution of the defects would allow closing of the feedback loop to adjust fabrication line parameters or, more fundamentally, such information could be used by device designers as input for process and device models.

The region of primary interest for this study is the substrate *n*-region. After the first diffusion, this region is no longer directly accessible since the wafer now has an enveloping *p*-skin. The objective is to utilize the existing diffused junction and isolate one or more appropriate test structures for probing the *n*-region. There are several attributes required of the solution to this problem: (1) define and isolate the *pn* junction, (2) make contact to the *n*-region, (3) make contact to the *p*-region, (4) passivate the junction to minimize leakage currents, (5) use processing techniques which do not alter the properties of the region of interest, and (6) make measurements in wafer form. Possible device configurations for a test structure are shown in figure 1. In either case, an array of mesa diodes would be fabricated by chemical, ultrasonic, or mechanical means (or some combination of techniques). One form of passivation would be chemical vapor deposited silicon dioxide (CVD-SiO_2). Figure 1a illustrates top side *n*-contact and 1b shows a large area back side *n*-contact after removal of the *p*-diffusion by lapping.

Preliminary attempts at test structure fabrication have utilized either an ultrasonic machining or a dry plasma etching to define and isolate the junction. The ultrasonically fabricated wafer was passivated with CVD-SiO_2 and the plasma fabricated wafer was passivated by a thin thermal oxide. Acceptable devices had reverse leakage currents in the range of 10 nA or less with a 10-V applied bias. Figures 2 and 3 are photographs of the fabricated mesa diode structures.

In order to refine the mesa diode fabrication procedures described above and to investigate other methods, a test pattern (NBS-13) has been designed and produced. This test pattern includes a number of mesa diode test structures (various sizes and configurations), etch rate/etch control structures, contact resistors, and metallization continuity

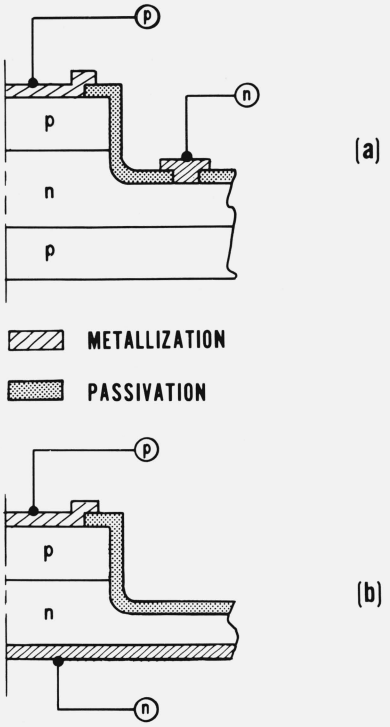

FIGURE 1. *Cross sections of the proposed mesa diodes: (a) top side n-contact, (b) back side n-contact.*

testers. Although only three levels are required for complete diode fabrication, this mask set provides additional levels to allow for flexibility in the processing procedures as well as in the choice of the procedures. Continuation of effort in this area includes investigation of different techniques for forming the mesa diodes and the optimization of procedures for fabricating routine test structures.

3. Development of Measurement Methods

In this laboratory, the primary method used for characterizing defects is the thermally stimulated current and capacitance measurement. This includes both the dynathermal current and capacitance measurements, and the isothermal capacitance transient measurement. The dynathermal TSM technique is extremely useful for quick surveys of processed devices. If the response matches that of a previously characterized defect, an identification can be made. Although either the dynathermal [2] or isothermal [5] techniques can be used to derive the important parameters, the isothermal method is preferred for accurate energy level determinations.

For the isothermal transient capacitance (ITCAP) measurement, charged defects in the depletion region of a reverse biased diode are detected by observing the decay in the depletion capacitance as the defects discharge. The procedure is as follows:

1. Cool the diode to a given temperature.
2. Apply a momentary zero-bias to charge the defects.
3. Re-establish the depletion.
4. Measure the capacitance transient decay with time.

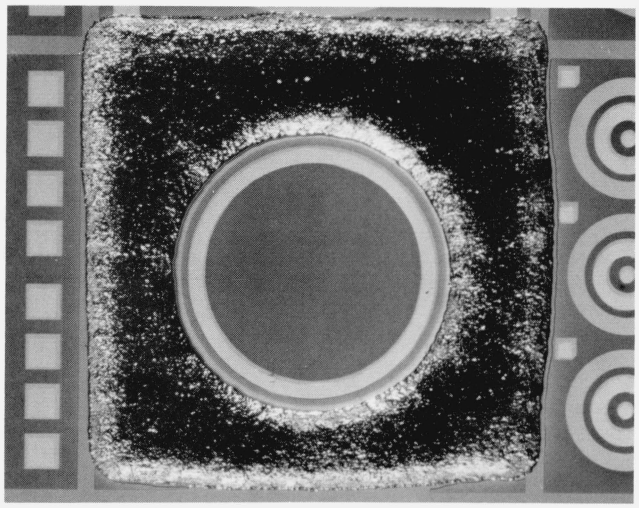

FIGURE 2. *Photograph of the ultrasonically machined mesa diode; the major diameter of the mesa is about 1.5 mm.*

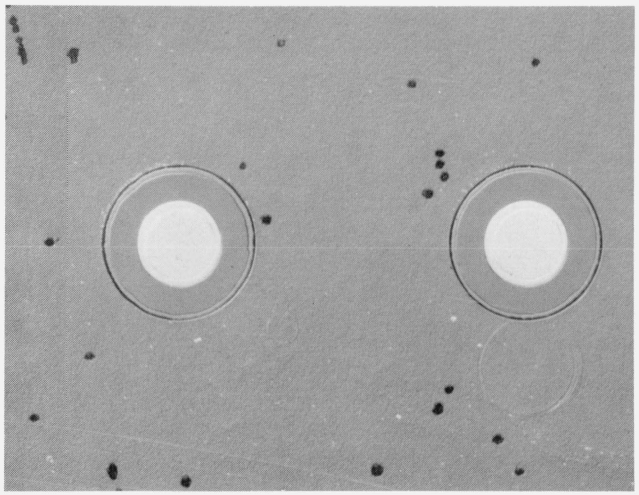

FIGURE 3. *Photograph of the plasma etched mesa diode; the major diameter of the mesa is about 230 um.*

The schematic of figure 4 illustrates the basic features of the capacitance transient. Under steady state reverse bias conditions, the capacitance assumes the final value C_f. The momentary zero-bias collapses the depletion region allowing majority carriers to charge the defect centers; the capacitance increases to C_b. After reapplying the reverse bias, the initial capacitance C_i is less than C_f due to the increased width of the space charge. As the defect centers discharge, the removal of charge from the depletion region causes decay of the capacitance value back to C_f. The exponential decay rate of the capacitance is temperature dependent. From the experimentally measured capacitance decay, one can calculate the expression [5]:

$$C_r(t) = \frac{(C_b^2 - C_i^2)(C_f^2 - C^2(t))}{(C_b^2 - C^2(t))(C_f^2 - C_i^2)} = \epsilon^{-(e_n+e_p)t} = \epsilon^{-et} \quad (1)$$

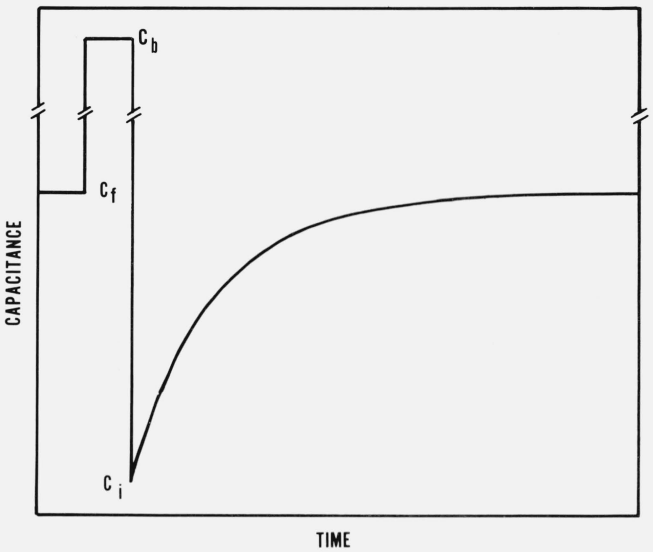

FIGURE 4. *A schematic plot of the isothermal capacitance transient with the key capacitance values identified.*

where $C(t)$ is the measured time dependent capacitance transient, C_i, C_f, and C_b are defined in figure 4, t is the time, and $e = e_n + e_p$ is the sum of the electron and hole emission rates, respectively. The emission rates can be expressed in terms of the empirical Arrhenius relation:

$$e_n = B_n T^2 \epsilon^{-\Delta E_n/kT} \quad (2)$$

$$e_p = B_p T^2 \epsilon^{-\Delta E_p/kT}. \quad (3)$$

T is the temperature in kelvins and k is the Boltzmann constant. ΔE_n and ΔE_p are, respectively, the distance in energy from the defect level to the conduction band and the valence band, and B_n and B_p are the emission coefficients. Under certain conditions one emission rate dominates. For example, if $e_n \gg e_p$ ($\Delta E_p > \Delta E_n$ and $B_n > B_p$), then e_n can be determined as a function of temperature by measuring $C_r(t)$ as given in eq (1). An Arrhenius plot of $ln(e_n/T^2)$ against T^{-1} has slope $\Delta E_n/k$ which gives the energy of the shallow level. The intercept of this plot at T = 0 gives lnB_n. For a midgap level, however, $\Delta E_n \approx \Delta E_p$, and *a priori* neglect of either e_n or e_p is not justified. Hence, the energy level determined from a plot of $ln(e/T^2)$ against T^{-1} is a "composite" level due to $e = e_n + e_p$.

Full characterization of the midgap level where ΔE_n and ΔE_p are comparable requires additional measurements. These measurements include isothermal leakage current measurements, or isothermal initial and final current or capacitance measurements. Either of these methods is capable of separating e_n and e_p and hence can independently derive ΔE_n and ΔE_p. In the isothermal initial and final capacitance measurement, the ratio e_p/e_n for a p^+n junction is determined from [5]:

$$\frac{e_p}{e_n} = \frac{N_t q \epsilon A^2}{2V} \cdot \frac{(C_b^2 - C_f^2)(C_b^2 - C_i^2)}{C_b^4(C_f^2 - C_i^2)} - 1. \quad (4)$$

N_t is the defect density (determined independently), q is the electronic charge, ϵ is the dielectric constant for silicon, A is

the junction area, and V is the applied bias. Since the sum, as determined from eq (1) and the ratio from eq (4) are known, e_n and e_p are separable. In the isothermal leakage current measurements, one determines the quantity [5]:

$$G(T) = \frac{N_t e_n e_p}{e_n + e_p}. \tag{5}$$

The empirical quantity $G(T)$ is proportional to the slope of a straight line fitted to the leakage current versus the reciprocal junction capacitance for various bias voltages. This equation along with $e = e_n + e_p$ from eq (1) again allows a separation of e_n and e_p.

As discussed above, the isothermal transient capacitance measurement is extremely useful for determining the important defect parameters. In the present mode of operation, a single capacitance transient is recorded on an x-y recorder; the response time of the x-y recorder imposes a limitation on the fastest ($e^{-1} \approx 100$ ms) capacitance decay time that can be measured. In order to alleviate this limitation, a modified ITCAP technique has been developed. It utilizes the continuous pulse mode operation of the DLTS method [1] but continues to use 1 MHz capacitance measurements (as apposed to DLTS which typically uses 20 MHz). A block diagram of the measurement apparatus for this modified ITCAP technique is shown in figure 5. The pulse generator is used to continuously pulse the diode from reverse bias to zero bias; at a given fixed temperature, this results in a continuous series of capacitance transients (one transient is shown in fig. 4). The digital processor is used to measure and record each capacitance transient and averages the results of a number of transients to improve the signal-to-noise ratio. The gate delay and gate width circuitry provide a gate signal to the analog gate which is used to clip the large zero-bias capacitance peak from the transient signal (see fig. 4). This allows maximum use of the dynamic range of the digital processor. The digital processor then calculates the appropriate time constant associated with the measured capacitance transient. These time constants or emission rates are measured as a function of temperature and the defect parameters are calculated as described earlier. This modified technique can characterize much faster transients and, in principle, is limited only by the response time of the commercial capacitance bridge (≈1 ms).

4. Development of Wafer Apparatus

Deep level measurements on packaged devices are common practice. That is, test devices are fabricated on wafers, scribed, diced, die bonded, wire bonded, and hermetically sealed in a package. The necessity to perform the operations after the fabrication of the wafer unnecessarily lengthens the time required to perform the defect measurements. In particular, application of these techniques to power devices requires wafer handling capabilities. A major objective of this study was to design and construct appropriate apparatus to allow deep level measurements on processed wafers. This approach required the development of a large-area, thermally controllable chuck, optimized for its thermal response. To accommodate these needs, a thermal chuck was designed and incorporated into a modified wafer probing apparatus. It has a temperature range from 77 K to 625 K with a heating rate in excess of 6.5 K/s and has been used to measure currents as small as 200 fA (0.2 pA) and capacitance changes as small as 5 fF (0.005 pF).

The basic components of the chuck assembly are shown in figure 6; the parts key is listed in table 2. The top plate (3) has vacuum grooves for wafer hold-down, a deep hole for thermocouple insertion and mounting holes for the wafer index-stop (2). The top plate is nickel-plated copper and is electrically isolated from the chuck body (5) by the insulator plate (4) which must provide good electrical isolation as well as good thermal conduction; a sapphire plate (0.25 mm by 67 mm dia.) was found to perform most satisfactorily and is in current use. The heart of the assembly is the chuck body (5) which consists of an integral cooling cavity and holes for the heater cartridges (10). An inverted view of this part is shown in figure 6b, with the heaters exposed. The cover plate (6) encloses the cooling cavity and attaches to the manifold (9) for the coolant fluid. The heater cartridges (10) (150 W each) are silver-soldered into the copper chuck body (5); the chuck body is subsequently heli-arc welded to the stainless steel cover plate (6) and mounting ring (7). Since the mounting ring (7) is attached to supporting hardware, it has been designed with a thin rib (0.25 mm) on the circumference to minimize heat transfer to the support. The power leads for the heater cartridges (10) are shielded along their entire length with either solid (11) or flexible metal shields. The top surface of the chuck body (5) is identical

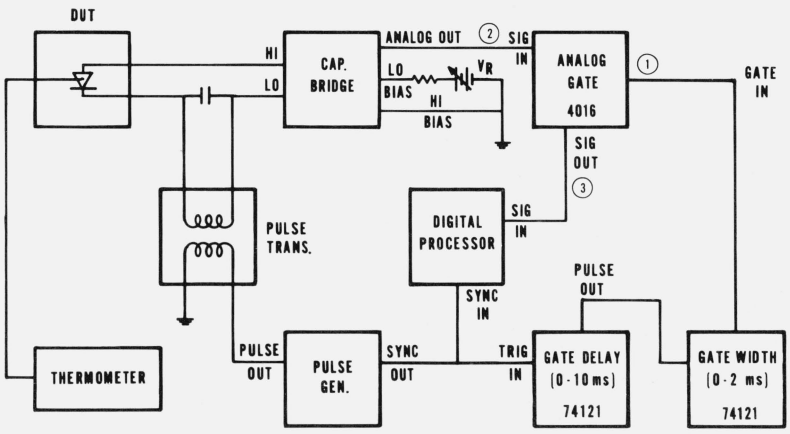

FIGURE 5. *Block diagram for the modified ITCAP method for measuring the emission rate of a defect.*

TABLE 2. *Component list for the thermal chuck*

1. 2-in (50-mm) wafer	8. Base plate
2. Wafer index-stop	9. Coolant manifold (2 ea.)
3. Top plate	10. Heater cartridge (4 ea.)
4. Insulator plate	11. Electrostatic shield (4 ea.)
5. Chuck body	12. Thermocouple (2 ea.)
6. Cover plate	13. Chuck vacuum supply (2 ea.)
7. Mounting ring	14. Leveling and locking screws (3 pr.)

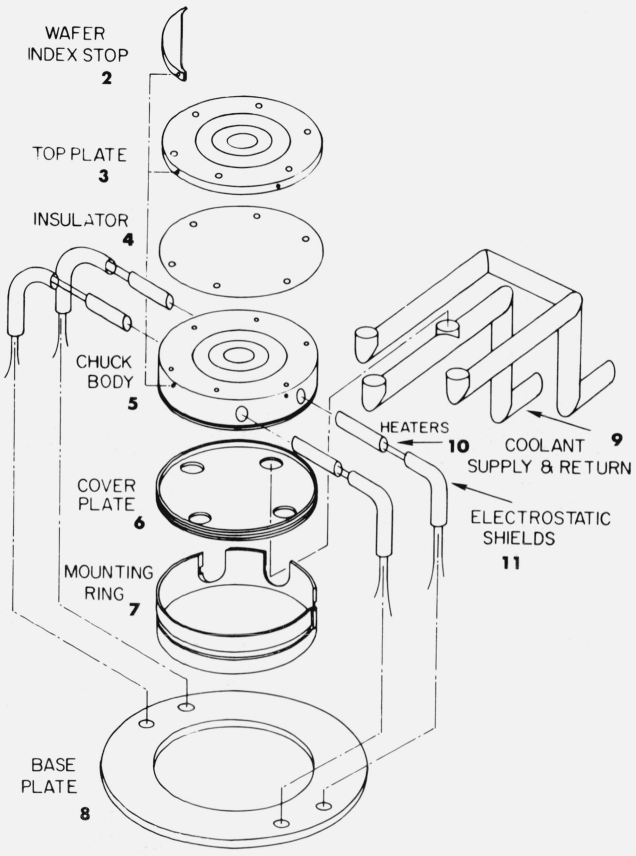

FIGURE 6. *The thermal chuck assembly: (a) Detailed view of the major components.*
(The numbers indicate major components of the assembly listed in table 2.)

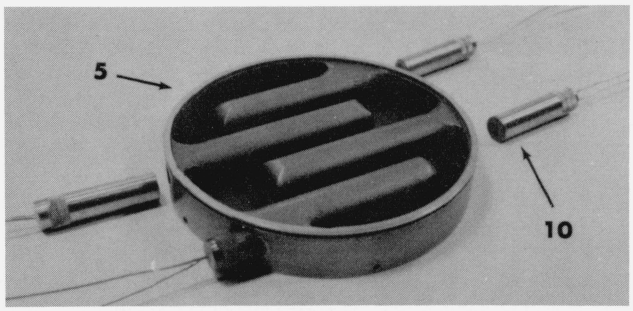

FIGURE 6. *The thermal chuck assembly: (b) Inverted view of the chuck body with the heater cartridges.*
(The numbers indicate major components of the assembly listed in table 2.)

(including vacuum grooves) to the top plate (3); for measurements which do not require electrical isolation, this feature allows higher thermal response. Figure 6c shows a photograph of the assembled thermal chuck. The two independent thermocouples (12) are seen near the top of this photograph; to eliminate possible electrical interferences, the thermocouple in the top plate is an isolated type. Each of the thermocouples has two independent elements of type K sensitivity. Also seen in this view are the pipes (13) for the chuck vacuum supply (wafer hold) and the screws (14) which are used for leveling and locking the thermal chuck assembly.

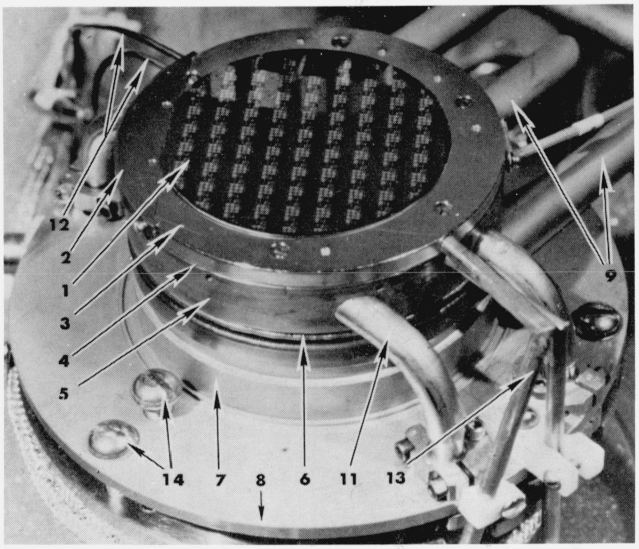

FIGURE 6. *The thermal chuck assembly: (c) Photograph of the assembled thermal chuck.*
(The numbers indicate major components of the assembly listed in table 2.)

To build in the capability for automation of measurements, the thermal chuck assembly was adapted to a modified automatic wafer prober. This commercial prober has a probe ring assembly which can accommodate as many as sixty individually adjustable probes. Once mounted and adjusted, the probes remain fixed in space. Automatic probing is accomplished by moving the chuck-mounted wafer to the appropriate position relative to the probes. The prober provides a small vertical motion (z) to raise or lower the chuck in order to make or break contact between the wafer and the probes; x-y translation is then accomplished by a table to which the chuck is mounted. After reaching the new position, the z motion is actuated to make contact with the device. This automatic feature completely eliminates manual alignment of probes after the initial alignment. A computer interface allows the probing machine to index from die to die

at a preset interval to allow automatic probing and measurements of devices on the wafer.

The low temperature requirements of the thermally stimulated measurements dictate the use of a cryogenic fluid for the thermal chuck coolant. It is important to maintain a relatively dry ambient to minimize or eliminate the condensation of water vapor on the wafer at low temperatures. For this reason, it is necessary to operate the chuck within a dry environment; this was provided by enclosing the thermal chuck and the wafer prober in a hermetically sealed box. The enclosure is continuously purged (≈2.5 sLpm) with dry nitrogen to minimize moisture penetration. A unique wafer-slide mechanism allows wafers to be inserted or removed from the box without exposing the interior of the box to the room ambient. Once inside the box, the wafer is transferred from the slide to the wafer chuck with a vacuum-operated probe. Wafer alignment is accomplished by manipulation of externally available controls. A viewport (covered during measurements) provides visual access to the wafer which is viewed through a stereo microscope. Additional details of the apparatus are available elsewhere [4].

5. Some Measurement Results

Gold is frequently used to control the lifetime or the switching characteristic of high-power diodes and thyristors. It is known to produce at least two centers in the band gap of silicon: an acceptor at $E_c - 0.55$ eV and a donor at $E_v + 0.35$ eV [6]. The gold centers are generally produced by diffusing the gold near the end of the wafer-fabrication procedure. The uniformity of the electrical activity of such centers on wafer-sized power devices is an important consideration in the ability of the device to switch uniformly over its entire area. The measurements discussed in this section directly address the question of the uniformity of the electrical activity of the gold defect centers in silicon.

As a demonstration of its wafer-mapping capability, the probing apparatus was used to map the gold-donor density in a processed wafer. Thermally stimulated current and capacitance measurements were made on the 432-μm diameter base-collector gated diode (structure 3.10) of NBS-3 [7]. This test structure is repeated at 5.08-mm intervals; there are about 70 identical devices on a standard 2-in diameter wafer. The thermally stimulated measurements were repeated across the wafer at 5.08-mm intervals using the apparatus.

The n^+p gated diodes were fabricated by a typical bipolar procedure. After growth of the field oxide, the n^+ base regions were formed by diffusing phosphorus into ⟨111⟩, 5–10 Ω·cm, p-type silicon (boron doped); the junctions were about 1.5 to 2.0 μm deep. Although an emitter diffusion was performed to complete other test structures, it was not of consequence for the test diode considered here. The gold center was introduced by the diffusion of gold (from a back side evaporation) at 825 °C for 24 h.

Figure 7 shows the thermally stimulated response from a typical diode on the processed wafer. The upper curve is the capacitance response and the lower is the current response. In each case, the response was measured by first cooling the device to near liquid nitrogen temperature. Zero bias was applied to the diode to charge all defects with majority carriers (holes); a reverse bias of 15 V was then applied to form a depletion region. The current or capacitance was measured with the depletion bias maintained while the wafer was heated with a heating rate of about 7 K/s. At the appropriate temperature the gold donor emits its trapped hole causing a measurable current, a slight collapse of the depletion region, and a measurable capacitance increase. The system noise in the x-y recorder tracings was approximately 2 fF and 100 fA for the capacitance and current, respectively.

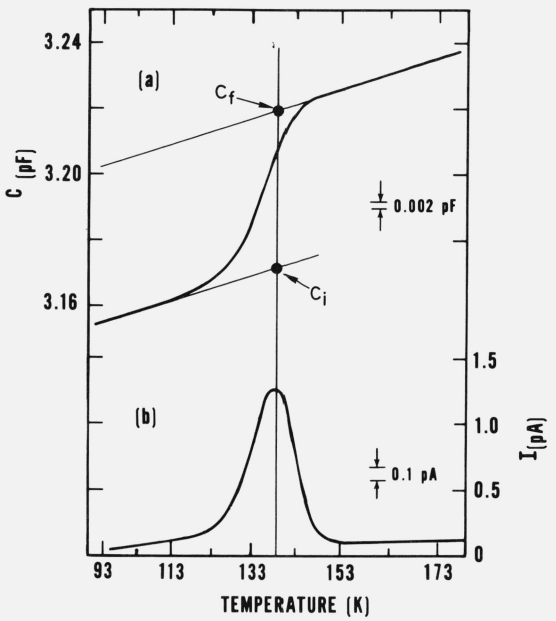

FIGURE 7. *The thermally stimulated (a) capacitance and (b) current responses of a gold-doped n^+p diode (heating rate ≈ 7K/s).*

The gold donor concentration was determined by measuring the thermally stimulated capacitance response as a function of wafer position. Following the work of Buehler and Phillips [3], the defect concentration is given by

$$\frac{N_t}{N_A} \approx \frac{2(C_f - C_i)}{C_f}. \tag{6}$$

N_t/N_A is the ratio of the defect density to the background acceptor density; C_f and C_i are given in figure 7. This expression is valid for the case when only one charge carrier is emitted, and $C_b^2 \gg C_i^2$ [3] where C_b is the zero bias diode capacitance. These conditions are satisfied in this measurement of the gold donor density. Note that in this measurement only the total charge flow, as evidenced by the change in capacitance, is important; the result is independent of the heating rate. An independent measure of the average acceptor density of the depletion region is required and was determined from a room temperature measurement of the capacitance-voltage characteristic of the same junction used for the TSM. The acceptor density, N_A, was calculated from the Schottky equation:

$$N_A = \frac{2C_1^2C_2^2(V_2 - V_1)}{q\epsilon(C_1^2 - C_2^2)}. \tag{7}$$

C_1, V_1 and C_2, V_2 are the capacitance-voltage pairs taken from the diode C-V characteristic. C_1 and C_2 were measured with applied reverse bias voltages of 5 and 15 volts, respectively, for V_1 and V_2. These data were used to calculate the absolute defect density from eq (6). Figure 8 displays the gold donor density (8a) and the boron acceptor density (8b) as a function of position on the wafer. In each case, the darker areas represent regions of higher density. Judging from figure 8, it appears that there is no relationship between the gold donor defect density and the boron acceptor background. The system noise (2 fF or 0.002 pF) suggests that gold donor densities in the range of 1×10^{12} cm^{-3} would be detectable in this wafer.

An important performance specification for all diodes, rectifiers, and thyristors is the off-state current or the reverse leakage current, I_R. Under reverse bias conditions, the total current through the junction is the sum of space charge generation current and diffusion current generated in the neutral region within a diffusion length of the depletion edge. A simplified expression for the space charge generation current is given by [8]:

$$I_{\text{gen}} = \frac{q K N_t W A_J}{2 \cosh [(E_i - E_t)/kT]}. \tag{8}$$

E_i is the intrinsic fermi energy, E_t is the trap energy, W is the space charge width, A_J is the junction area, and K is the product of the intrinsic carrier concentration, thermal carrier velocity, and a simplified carrier cross section. Similarly, the diffusion current from the n-side of a p^+n junction is [9]:

$$I_{\text{diff},p} = q G_M L_p A_J. \tag{9}$$

G_M is the minority carrier generation rate and L_p is the diffusion length for holes. The space charge generation current is seen to be directly proportional to the trap density and the depletion volume (WA_J) which is proportional to the applied bias. However, I_{gen} is important only when the trap level is near midgap ($E_t \approx E_i$). The diffusion current is dependent on a different generation volume ($L_p A_J$), but is independent of the applied bias.

In another study, the thermally stimulated current and capacitance measurement technique was used to determine the defect density of a gold-doped wafer processed with p^+n gated diodes. The gold was introduced into the n-type wafer after the planar diodes were fabricated by a 24-h, 800 °C heat treatment of a back side gold deposit. Figure 9 shows a typical current and capacitance response of a device on the wafer. The defect response causing the capacitance transition and current peak near 225 K is due to emission from the gold acceptor near midgap at 0.547 eV below the conduction band edge. After the acceptor emission, the device is clearly seen to enter the temperature-dependent reverse leakage regime. This is also clear evidence that leakage in the gold-doped diode occurs through the midgap acceptor level. Using the thermally stimulated capacitance technique as described earlier, the density of the gold acceptor defect was mapped

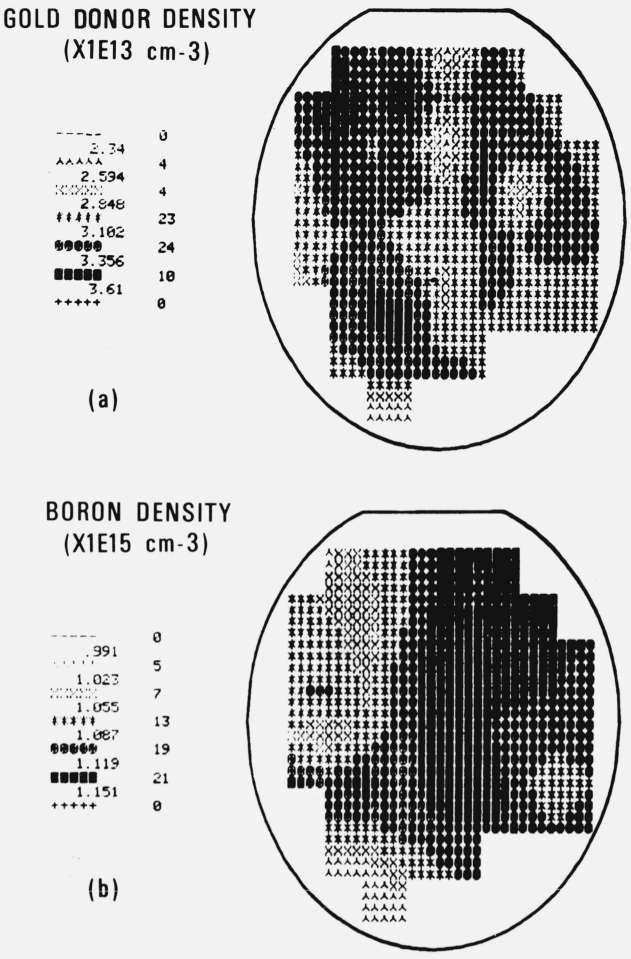

FIGURE 8. *Wafer maps of (a) the gold donor density and (b) the boron acceptor density in the p-region of n^+p diodes.*
(Approximately 70 data points are plotted on a grid corresponding to the 5.08-mm spacing of the devices on the wafer. Shading at intermediate points is derived by interpolation.)

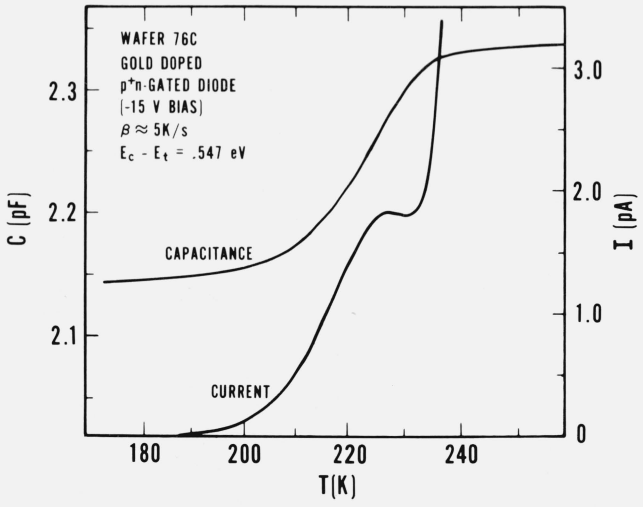

FIGURE 9. *Thermally stimulated capacitance and current responses of the midgap gold acceptor (heating rate ≈ 5 K/s).*

as a function of position on the wafer (fig. 10a). The total variation of the defect density is 1.89 to 7.55 × 10^{13} cm^{-3} from light to dark regions, respectively. The wafer map graphically reveals the nonuniformity of the distribution of the active gold defects.

The reverse leakage current for the same devices was also measured. The temperature was maintained at 23 °C and the applied bias was −15 V. The results illustrated in figure 10b show a variation in the leakage from 0.257 to 1.045 nA.

The pattern of the current leakage wafer map is virtually identical to the pattern of the gold acceptor defect density map. Where the defect density is low, the leakage current is low. Plotted in figure 11 is the reverse leakage current against the acceptor defect density. Each point represents one of the 65 devices on the wafer. Although there is significant scatter, there is an obvious near-linear relationship between the reverse leakage current and the defect density.

Without additional detailed measurements of the leakage current as a function of temperature, it is not possible to evaluate the extent to which the diffusion current contributes to the leakage. An extrapolation of a linear "best fit" to the data of figure 11 toward zero defect density intersects the current axis near 0.1 nA. This is suggestive of the bias-independent diffusion contribution to the leakage. (Note: Surface leakage was minimized by appropriate bias on the gate of each device.)

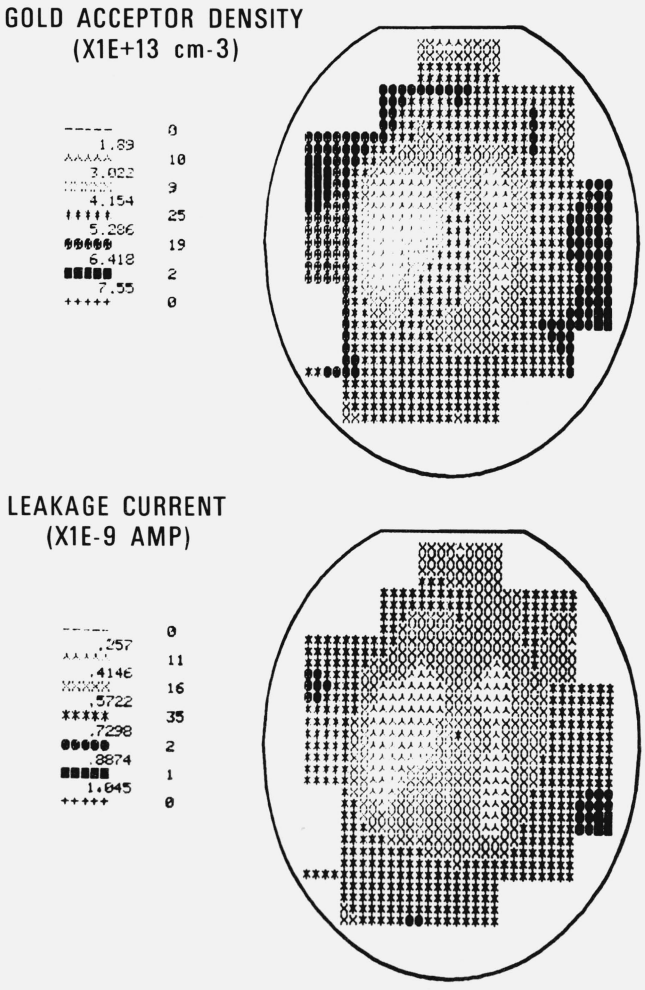

FIGURE 10. *Wafer maps of (a) the gold acceptor defect density and (b) the reverse leakage current.*
(Approximately 65 devices spaced at 5.08-mm intervals on the 51-mm wafer were measured).

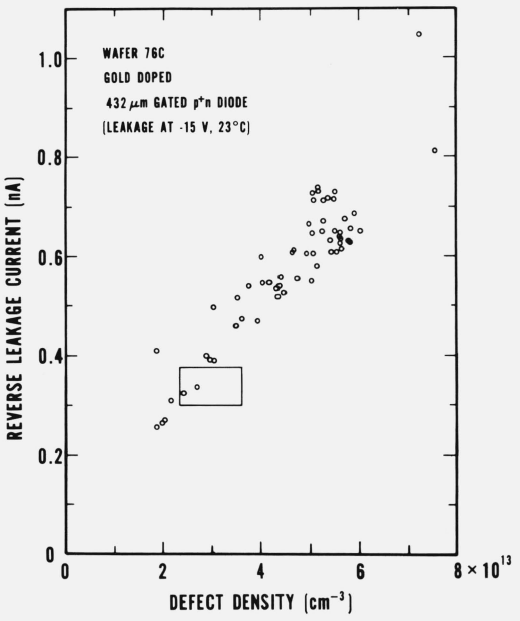

FIGURE 11. *Plot of the reverse leakage current versus the acceptor defect density.*
See text for discussion of the rectangular area.

The wafer map of the gold donor density in p-type silicon (fig. 8a) showed only a 50-percent variation from 2.34 to 3.61 × 10^{13} cm^{-3}. A reverse leakage measurement was also made on this wafer and plotted. The data points from this wafer all fall within the rectangle shown in figure 11. (The fact that the rectangle is low may mean that the diffusion component in the p-type wafer is smaller than in the n-type wafer.) Again, there is significant scatter in the data; however, it is clear that these n^+p devices share the same relationship as the p^+n devices. The gold donor is a shallow level (0.345 eV above the valence band), and hence its emission occurs at temperatures well below the onset of reverse leakage (fig. 7). Therefore, the donor defect cannot influence the reverse leakage. However, the fact that data for the gold donor in the n^+p devices fall essentially on the same curve as for the p^+n devices suggests evidence to the contrary. These data can be reconciled by realizing that there is a one-to-one correspondence between the acceptor and donor defect in gold-doped silicon and that reverse leakage in the n^+p as well as the p^+n is controlled by the midgap acceptor level.

These results demonstrate the unique capabilities of this temperature-controllable wafer probing apparatus. The ability to perform deep level measurements at the wafer level for process control or process diagnostics is a valuable addition to the process engineer's selection of analytical tools.

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