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A Transistor Screening Procedure Using Leakage Current Measurements

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A study of the aging behavior of low-power germanium alloy switching transistors has revealed a relationship between small changes in junction leakage current, induced by a brief aging stress, and later deterioration in performance. This relationship may provide the basis for a nondestructive screening procedure which would serve to identify germanium alloy transistors likely to deteriorate through excessive growth of junction leakage current. The proposed screening procedure involves the determination of relatively small changes in junction leakage current, increases of the order of 15 percent or more, associated with 1,000 hours of aging at a shelf (bake) stress of 100 °C. Because the leakage current changes of interest are small, relatively high demands are placed upon measurement repeatability. There is evidence that transistors bearing identical type numbers but of different manufacture respond differently to the same screening procedures and would therefore require different screening limits.

Key Words: Aging behavior, alloy transistors, failure prediction, leakage current, screening procedures, temperature stress, transistor, transistor failure, transistor screening.

1. Summary

The data from a 20,000-hr transistor aging behavior study indicate that small changes in junction leakage current, induced by baking, provide a means for identification of units likely to deteriorate through growth of leakage current. A subsequent independent experiment, which included transistors of different manufacture, provided further evidence that this behavior may be generally characteristic of germanium alloy transistors. The second experiment also examined the effects of more stringent screening stresses.

2. Introduction

Studies of aging behavior of transistors are never free from many of the confounding effects which tend to degrade measurement repeatability. The data from recent experiments indicate that, generally, junction leakage current tends to decrease during early stages of aging. As aging continues, or as aging stresses are increased, the downward trend ultimately reverses. For some transistors, junction leakage currents were observed to increase from the outset. Those units exhibiting the largest increase formed a group which contained all (or nearly all, depending upon performance criteria) of the transistors which deteriorated more rapidly as aging continued. It appears that for these transistors, early increases in leakage current are a manifestation of a continuous process during which leakage current continues to increase, leading eventually to "failure." Since leakage-current degradation is not uncommon, careful observation of early changes in leakage current shows promise as a basis for a practical means of screening transistors to further improve transistor reliability.

The fractional changes in leakage current of interest are relatively small, and therefore all sources of variability in the measurement process are of concern. The inherent behavior of the device itself is one such source, and in some instances is the major source of variability. The measurement of transistor parameter values is not only dependent upon bias conditions and ambient temperature, but also upon the time duration of the measurement and upon the bias and temperature histories resulting from prior measurement and aging stresses. For example, voltage breakdown measurements using current-limited values even as low as 10 μA have been observed to commonly cause marked disturbances in the leakage current values, requiring several weeks for the effects to subside. Voltage breakdown measurements should be avoided wherever sensitive leakage current measurements are being made. As another example, the transfer of a transistor from an aging to a testing environment is accompanied by a shift in parameter values which usually requires several days to approach a new center value. This stabilization effect [1] appears repeatable for a given transistor but is not consistent among transistors. The above mentioned disturbances cannot, in general, be eliminated, but their effects may be substantially reduced by careful choice of operating procedures and test methods.

Similarly, the instability of measurement equipment, especially long-term drift, as well as variation in ambient temperature during measurement, introduces errors which cloud the meaningfulness of aging behavior data.

The National Bureau of Standards in cooperation with the Department of the Navy is conducting

[1] Zierdt, C. H., Jr., On importance of operating tests as compared to storage tests of transistors, The Solid State Journal 2, No. 9, 21–27 (1961).

transistor aging studies in which every reasonable effort is being applied towards minimization of unwanted variability in the aging data through careful instrumentation, selection of test methods and procedures, and design of experiments. A key feature of the instrumentation for measurement of d-c parameters, for example, is close ambient-temperature control. The transistors are immersed in a "constant-temperature" recirculating air stream. The air stream temperature is centered at 25 °C and fluctuations are regulated within ± 0.01 °C. Further precautions include replication of measurements coupled with computer analyses programmed to detect and identify questionable agreement between replications. This enables us to repeat questionable measurements, if necessary.

These and other precautions have helped to maintain a high level of equipment performance and measurement repeatability. A case in point is the record of temperature-sensitive leakage current measurements accumulated during the course of a three-year aging study wherein each of 10 "control" transistors was measured a total of over 3,000 times. Among these measurements are four sets of junction leakage current measurements, each set consisting of 300 recordings. These recordings were found to have gradually decreased approximately $1\frac{1}{2}$ to 2 percent during the 3-year period. The major part of this decrease is traceable to creep of 0.08 °C in the calibration point of a thermometer due to stabilization of the glass bulb. Corrections for the gradual change in ambient temperature between each measurement period resulted in an estimated coefficient of variation of less than 1 percent. This performance record is consistent throughout the data and demonstrates the stability of the transistor-measurement system combination and serves as a measure of confidence which may be placed in the transistor aging data discussed in this paper.

3. First Experiment

The first of two experiments described in this paper provided a survey of the behavior of approximately 500 type 2N396 germanium alloy transistors in response to a wide range of aging stresses. The second experiment used approximately 100 transistors to explore more fully behavior in the 100 to 125 °C region and to introduce different types and manufacture of germanium alloy transistors into the study. All transistors had met stringent military requirements and were considered "high reliability" units.

A full reporting of the first experiment, in which over $\frac{1}{4}$ million measurements have been recorded, would be prohibitively lengthy. A brief description of the entire experiment, however, is given in the appendix. Attention is focused on that part of the experiment involving the four groups of transistors which were subjected to four different combinations of aging. Each combination was calculated to produce a junction temperature of 100 °C (identified as aging conditions 13, 14, 15, and 18 in table 3). This temperature lies roughly in the center of the aging-stress spectrum for the total experiment.

The 100 °C aging conditions are of particular interest because the small but significant changes in leakage current, occurring within the first 1,000 hr of aging, take on meaningful significance when compared with later aging behavior.

The aging conditions at 55 °C and below produced too little deterioration in 20,000 hr of aging to be of much value in testing relationships between early change and aging. Comparison of results for the different aging temperatures, however, were not inconsistent with the expectation that failure rates (and chemical activity) double for each approximately 10 °C increase in junction temperature. The volume of data from the lower stress conditions, 55 °C and below, provided assurance that the measurement system, as well as the transistors, was quite stable and factors affecting repeatability were in close control.

The aging conditions at 145 °C and above, on the other hand, caused relatively rapid deterioration, and in a few cases, total destruction occurred prior to the first measurement period, i.e., during the first 340 hr of aging. Further aging showed conclusively that the failure rates were too high to expect the data for these conditions to shed much light on the meaningfulness of small early changes.

For the reasons given above, the remainder of the discussion of the first experiment will be devoted to the behavior of the four groups consisting of 160 transistors aged with the junction temperature maintained at 100 °C for a total of 20,000 hr.

4. Data

Each of the four groups of 40 transistors was subjected to a different combination of ambient temperature and applied bias power. The four aging conditions are identified in table 3 of the appendix. Three of the conditions were essentially shelf aging at an ambient temperature of 100 °C; condition number 13 provided no bias power, condition 15 included a nominal 3 mW of power dissipation, and condition 18 subjected the collector-to-base junction to a reverse bias voltage stress of -24 V. The fourth aging condition provided a combination of 70 °C ambient temperature and 120 mW of power dissipation which was the power required to raise the junction temperature to an estimated 100 °C.

The general effect of the four 100 °C aging conditions was to cause only a very small and gradual increase in the dispersion of the electrical parameters with no perceptible trend in the modal values. For those transistors which eventually exhibited substantial degradation, the changes were mainly gradual and thus presented the problem as to when performance should be judged "unsatisfactory." Since no particular circuit applications with associated performance limits were involved, the basis for such a decision is necessarily arbitrary. The criteria selected are similar to those appearing in the specification for the environmental acceptance tests, IEBO (-10 V) or

ICBO (−10 V) greater than 10 μA or hFE (10 mA, −5 V) less than 20. Using these criteria, the performance of a total of 10 transistors became "unsatisfactory" during the 20,000 hr of aging at 100 °C. (The total elapsed time of the experiment, including the measurement periods, exceeds 3 years.)

The records of behavior of these 10 transistors have been scrutinized and a summary is given in table 1. On the left, the individual transistors are identified along with their respective aging conditions. The code numbers for the aging conditions are fully described in table 3 of the appendix. "Unsatisfactory" transistors appeared in all four conditions, and differences in the number of "unsatisfactory" units corresponding to each condition are not sufficiently large to be considered significant. For these reasons, and for the lack of any other substantial differences in observed transistor behavior between the four aging conditions, it was decided to combine the data for the subsequent analyses.

TABLE 1. *Summary of aging behavior of "unsatisfactory" transistors*

Transistor and plug No.	Aging condition	0-hr values of		Early changes			Hours of aging	Deterioration					
				Ratio values of IEBO or ICBO, whichever is larger				"Unsatisfactory" criteria			Character of deterioration		
		IEBO	ICBO	340-hr	1,000-hr	1,000-hr		hFE*	IEBO	ICBO	Avalanche	Ohmic leakage	Other
		μA	μA	0-hr	0-hr	340-hr		< 20	> 10 μA	> 10 μA			
8−1058	15	2.163	1.645	3.578	3.795	1.061	2.0 k		X		E		
3−1066	18	.9479	1.152	1/1.039	2.101	2.182	2.0 k			X		EC	
0−1040	13	1.107	1.612	1.218	1.737	1.426	3.4 k	X				EC	
0−1052	14	[v] 2.191	1.496	3.658	3.854	1.054	11. k		X		E		
3−1064	18	1.361	1.489	1/1.106	1.213	1.342	11. k			X		C	
0−1050	14	[w] 1.169	[w] 2.873	1.041	1.066	1.024	14. k		X				(1)
8−1046	13	1.029	1.206	1/1.013	1/1.062	1/1.049	20. k		X				(2)
3−1068	18	.6595	.7854	1.014	1.064	1.049	20. k			X		C	
1−1070[L]	18	1.189	1.447	1/1.081	1/1.082	1.005	20. k			X		C	
2−1070	18	1.256	1.215	1.732	2.190	1.265	20. k		X			EC	

[L] Case leak detection test was applied after 20 khr to all of above transistors except 0−1050 and 8−1046. Only 1−1070 leaked; rate was ≈ 200×10^{-8} std. cm^3/s.
[v] Variable.
[w] Only 0-hr measurement was variable.

(1) Wafer was found to be cracked.
(2) Large and abrupt increase in emitter current.
"E" Indicates emitter and "C" collector junction.

Returning to table 1, the initial or 0-hr IEBO (−10 V) and ICBO (−10 V) values listed on the left were obtained before application of the aging stresses. The distribution of these values is not perceptibly different from that of the larger group of "satisfactory" transistors. Even the single maximum value listed would have been ineffective for screening, because at least 10 "satisfactory" transistors had larger values. We conclude therefore that these 0-hr values provide no effective means for identification of the "unsatisfactory" transistors.

Variability of the parameter values during measurement was another property of interest. A few of the 0-hr measurements in table 1 bear superscripts indicating that these measurements were classified as variable on the basis that the automatic digital voltmeter, which has a 2- to 3-sec conversion time, would not balance within 50 sec. This variability test was applied uniformly to all transistors throughout the experiment. There is no evidence that 0-hr measurement variability is uniquely related to deterioration. Over an extended period of aging, however, the time-series measurements indicated that consistently variable units exhibited more pronounced deterioration. The association was not so close (nor the technique amenable) as to favor the use of this criterion to screen potential failures.

In contrast to the ineffectiveness of the 0-hr leakage current measurements, *changes* in the value of junction leakage current observable within the first 1,000 hr of accelerated aging appear promising as a screening index. None of the other parameters in the experiment, measured or computed as listed in the appendix, appears to be as useful. For this reason the remainder of table 1 provides only for comparison between fractional changes in junction leakage current measurements and deterioration. Ratio values greater than unity indicate an increase in leakage current with time.

The ratio values given are the ratio of the 340-hr measurement divided by the 0-hr measurement, and the ratio of the 1,000-hr measurement divided by the 0-hr measurement. In each instance the ratio indicates the fractional change in junction leakage current; either the IEBO or ICBO change is listed, whichever is the larger. By thus combining the larger change into one table, a closer relationship between early fractional changes and deterioration in either junction is more apparent than if IEBO or ICBO were treated separately.

Although table 1 does not indicate which junction current is associated with the larger ratio value listed, the data reveal that with one exception, the junction associated with the larger ratio value was also the junction which deteriorated and led to "unsatisfactory" performance. The one exception was transistor 0–1040, where "unsatisfactory" was indicated by hFE* becoming less than 20, first observed after 3.4 khr of aging. In the very next measurement period (4.7 khr), the ICBO value exceeded 10 μA, and it was the collector junction which exhibited the larger ratio value. The consistent correspondence between early changes and deterioration in the same junction argues for the existence of a determinative relationship.

5. Character of Deterioration in Performance

The "Hours of Aging" in table 1 indicate when the transistor was first observed not to have met performance criteria, and was thereby adjudged "unsatisfactory." In each instance there was an increase in leakage current. The nature of these increases suggested the three categories listed under "Character of Deterioration." Avalanche conduction was ascribed to two transistors which exhibited a several-fold increase in (emitter) junction leakage current at 10 V with essentially no associated increase at 2 V. Conduction by current multiplication was clearly present. The second, and most common form of deterioration, was a gradual increase in leakage current for both bias levels. Six transistors displayed this type of deterioration. For each measurement period the estimated intrinsic saturation current, which was found by extrapolation of the current versus voltage curve to estimate the saturation current at 0 V, remained relatively constant, thus indicating the presence of a linear (ohmic) relationship between bias voltage and observed leakage current. The third characteristic of deterioration, designated "other," applies to two transistors which became catastrophic failures. The first of these two transistors, number 0–1050, developed a collector-to-base and collector-to-emitter "short," which was apparently caused by a fractured wafer found by optical examination. The presence of the overt fault was observed after this transistor, as well as all other transistors under study, was remounted and soldered to a new type of high-temperature plug. The implied causal relationship, damage by remounting, is not so clear-cut as it might appear in light of the following considerations. First, the soldering and handling techniques had been checked in a preliminary experiment in which the effects of the same soldering techniques were found to produce no significant change (less than 1 percent) in leakage current. All transistors were monitored before and after remounting, and only 0–1050 showed a change. Second, earlier behavior of 0–1050 was suspect. The initial 2-V ICBO value was 12 μA, and the 10-V value was, oddly, only 3 μA. Both measurements were variable. Replicate ICBO measurements made later in the same day were also variable, but were near 1 μA. The initial higher values did not repeat. Measurements of hFE were variable and large. They became normal after 340 hr of aging. In fact, from the 340-hr measurement period until the time it was withdrawn from the experiment at 14 khr, transistor 0–1050 was one of the best-behaved units in its aging condition. The above observation would lead one to suspect the wafer was cracked in the beginning. Such a suspicion is not unreasonable, in view of the fact that six of the original 500 transistors received for this experiment were found to have fractured wafers.

The second transistor, 8–1046, exhibited an abrupt increase in emitter leakage current between 14 and 20 khr of aging, with no prior indication of impending deterioration. The resulting voltage-current relationship had the character of ohmic conduction (~ 10 kΩ), but differing from the six other transistors classified as having ohmic leakage in that the change appeared as an abrupt steplike increase. Unfortunately, in removing the case for optical examination, the transistor was damaged.

With the exceptions of transistors 0–1050 and 8–1046, which had previously had their cases removed, the "unsatisfactory" transistors were subjected to 125 °C mineral-oil gross-leak detection test and a helium fine-leak detection test. Only transistor 1–1070 was found to leak, and at a rate of approximately 200×10^{-8} std. cm^3/s. (He).

6. Changes in Leakage Current Related to Deterioration

Table 1 lists the values relating early fractional changes in junction leakage current to deterioration which led to "unsatisfactory" performance. It is of interest to note that the two transistors which exhibited the largest early fractional changes were the only two which later developed avalanche conduction. The large fractional change in leakage current occurred within the first 340 hr of aging.

The significance of the relationships between fractional changes and deterioration is more fully revealed in figures 1, 2, and 3. Figure 1 relates aging behavior to the fractional increase in junction leakage current associated with the first 340 hr of the aging stress. Both junction currents were measured, but only the larger of the two fractional changes was plotted. The distribution of the ratio values for the entire 160 transistors is shown by the major histogram. The smaller receding histograms show cumulatively the ratio values for those transistors which had become "unsatisfactory" by the time indicated. The crosshatch shows when a transistor was first observed to be "unsatisfactory."

Similarly, figure 2 relates the change produced by the first 1,000 hr of aging to later behavior. A comparison of the two figures shows that, in general, the 1,000-hr ratio values of the "unsatisfactory" units fall more consistently in the upper range of the ratio distribution than do the 340-hr ratio values. In figure 2, the correspondence between relatively high ratio values and deterioration is clearly more pronounced for those units which deteriorated more rapidly, as

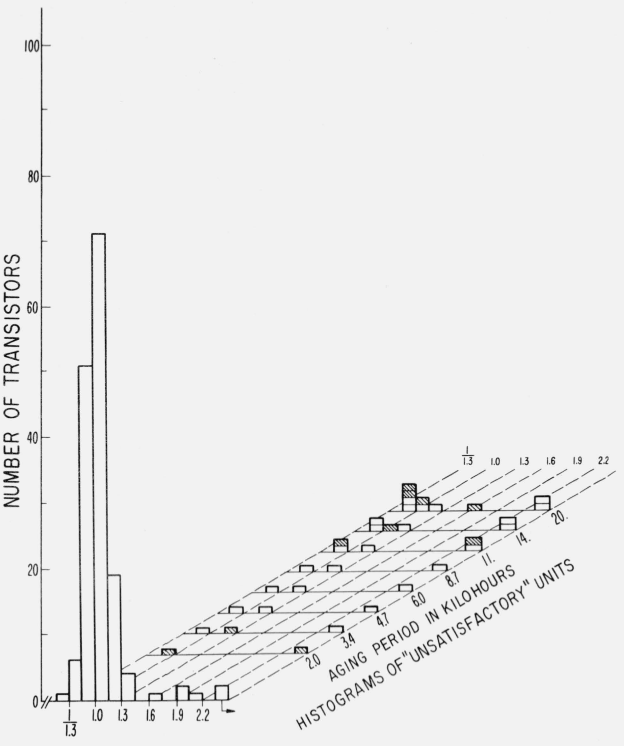


FIGURE 1. *Histogram of ratio values showing change in* IEBO *or* ICBO *after 340 hr of aging.*

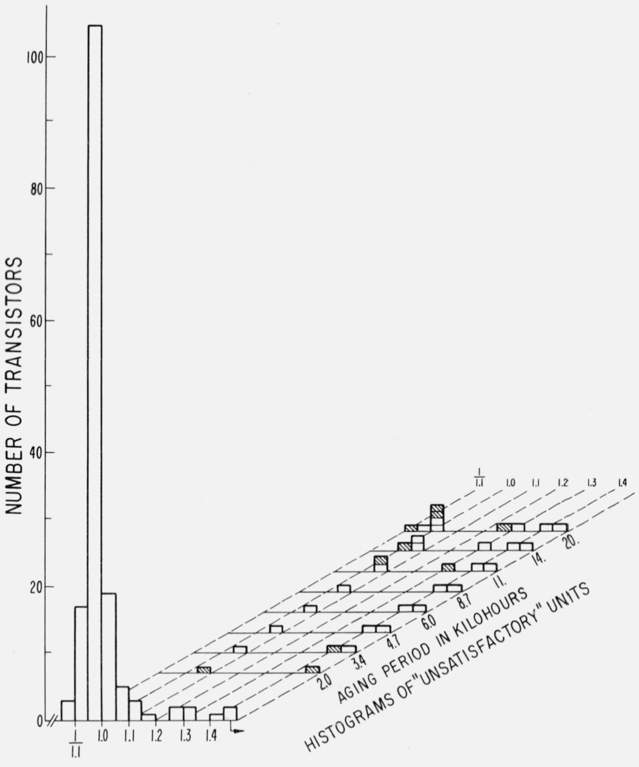


FIGURE 3. *Histogram of ratio values showing change in* IEBO *or* ICBO *between 340 and 1,000 hr of aging.*

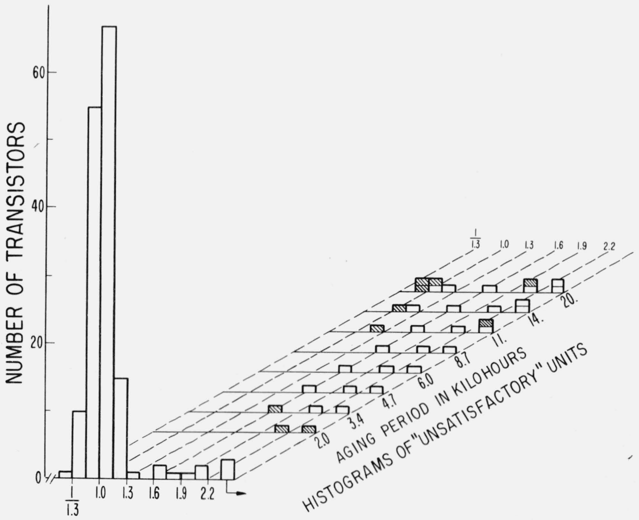


FIGURE 2. *Histogram of ratio values showing change in* IEBO *or* ICBO *after 1,000 hr of aging.*

shown by the histograms through 8.7 khr. The relationship becomes more tenuous for those units which last longer, as indicated by the histogram distributions spreading down scale with increasing time.

Figure 3 relates the change observed between 340 and 1,000 hr of aging to later behavior, thereby excluding the more pronounced effects associated with the first several hundred hours of aging. The distribution of values was so much more compact that the class interval of figure 3 was reduced to roughly one-third that used in figures 1 and 2 in order to obtain a reasonable representation of the distribution.

The relationships in figures 1 through 3 suggest means for the identification of transistors likely to deteriorate. These data are based on 100 °C stress for screening as well as for subsequent aging. It should be borne in mind that this stress is higher than that which would normally be encountered in applications. A convenient and reasonable approximation may be made of expected aging performance by assuming that the rate of deterioration doubles for every 10 °C increase in junction temperature.[2] For example, the rate of deterioration at 55 °C may be conservatively estimated to be 1/10 that at 100 °C. Figures in this report, therefore, may serve to roughly approximate aging under more normal conditions (say 55 °C) by multiplying the time scale (associated with 100 °C aging conditions) by 10. Reexamining figure 2 with the expanded time scale in mind indicates that the

[2] Peck, D.S., Semiconductor Reliability Predictions from Life Distribution Data, ch. 5 of Semiconductor Reliability, edited by Shwop, J. E. and Sullivan, H. J. (Reinhold Pub. Corp., New York, 1961).

first three "unsatisfactory" units might have caused trouble in an application by not providing "satisfactory" service for at least 1 or 2 years. On the other hand, the remainder of the transistors would have become "unsatisfactory" only after a period of service in excess of 10 years. The fact that the first three "unsatisfactory" transistors have unusually large ratio values strengthens the expectation that the relationship between ratio values and later preformance may serve as the basis for a practical screening test to detect transistors likely to exhibit junction leakage current deterioration.

Since the suggested screening procedures stem from an *a posteriori* examination of all the data, no significant tests of the effectiveness of these procedures can be made using these same data. A second, smaller experiment described later in this paper provides a set of independent data which is used for this purpose. However, in order to demonstrate the observed relationships of the first experiment in a screening test context, an example of a screening analysis is presented.

7. A Screening Example

The ideal screening test serves a dual goal; one is to reject all units which would, in fact, fail to meet ensuing operational requirements for at least a specified period of time, and the other goal is to not reject any units which would meet such requirements. Failure to achieve the former goal through the erroneous acceptance and use of faulty units would lead to unreliable performance. Because this is of obvious and immediate concern to the consumer, this type of error is usually associated with a consumer's risk. On the other hand, failure to achieve the *latter* goal through the erroneous rejection of satisfactory units would directly penalize the producer of such units. This type of error is therefore associated with a producer's risk. It is evident that one or the other of these errors can be made as small as is desirable at the expense of increasing the other. A graphic view of the interplay between these two errors for various choices of performance time requirements and screening criteria is presented in figures 4, 5, and 6. The information was derived from figures 1, 2, and 3, respectively. The three groups of histograms in each figure illustrate the effects of choices of screening limits by application of three different magnitudes of fractional change upon which to base the decision to reject or accept individual transistors. The indicated sets of limits are arbitrary and were chosen so as to provide a reasonable basis for discussion.

Each bar in figures 4, 5, and 6 is a complete analysis in itself, relating screening results with aging performance. The screening test identifies those transistors to be rejected. The number of rejected units is indicated by the height of the bar above the axis. Superimposed on the bar is the aging performance record whereby the individual transistors are classified as "unsatisfactory" if they fail to meet the end-of-life requirements within the time period indicated on the abscissae. For example, the second bar from the left

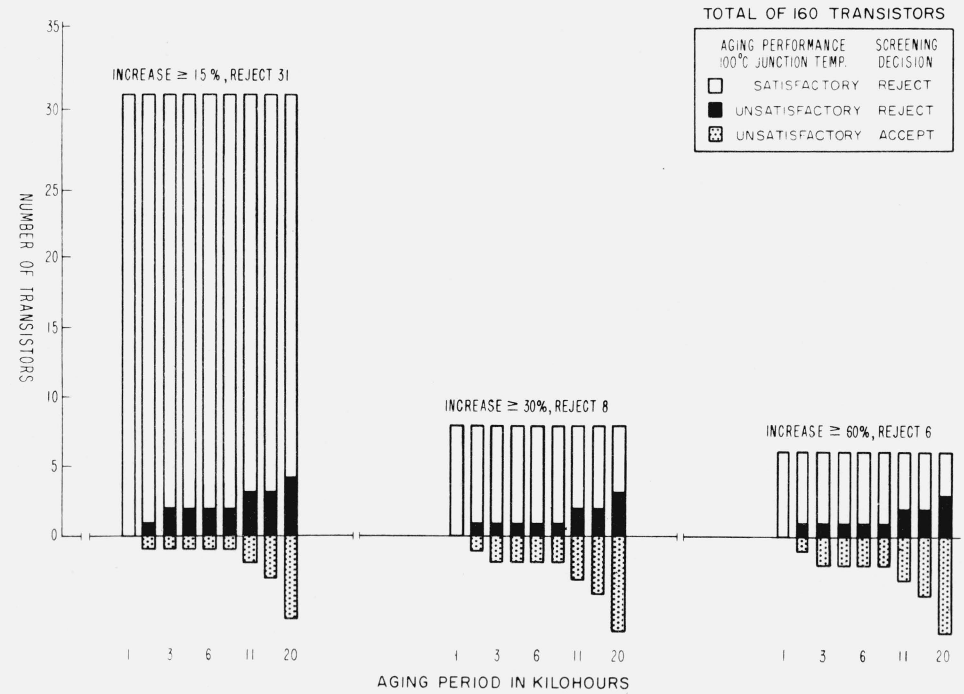


FIGURE 4. *Screening analyses using relative change in values of* IEBO *or* ICBO *after 340 hr of aging.*

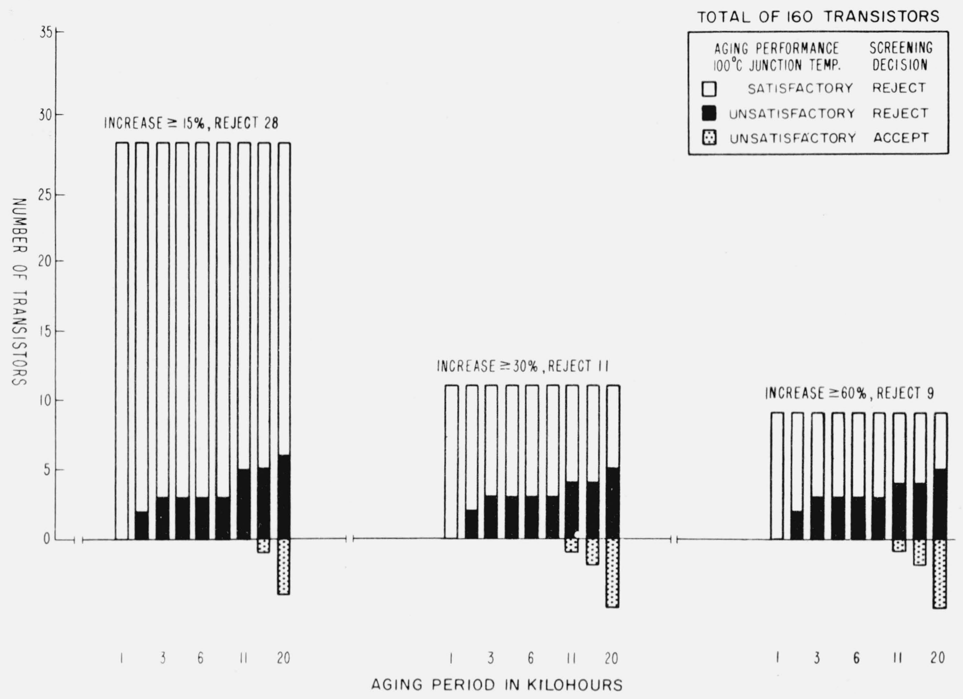


FIGURE 5. *Screening analyses using relative change in values of* IEBO *or* ICBO *after 1000 hr of aging.*

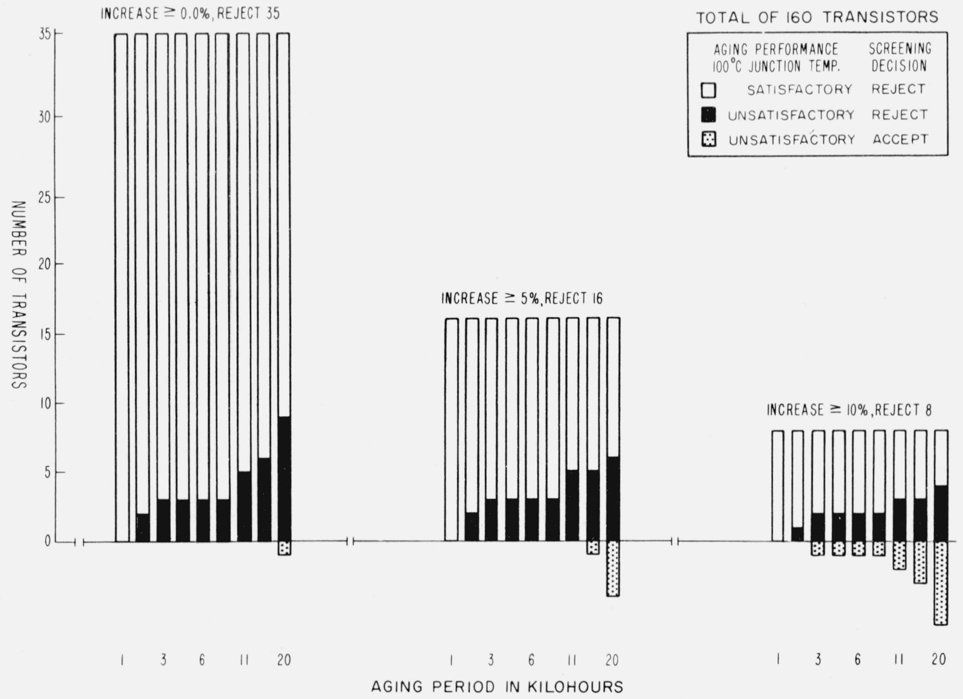


FIGURE 6. *Screening analyses using relative change in values of* IEBO *or* ICBO *between 340 and 1,000 of aging.*

in figure 4 indicates that after 340 hr of aging the junction leakage current (IEBO or ICBO) increased 15 percent or more in 31 of the transistors out of the total of 160. Two transistors out of the 160 were "unsatisfactory" after 2 khr of aging at 100 °C, one of which was within the group of 31 rejects and is represented by the black portion of the column. The second "unsatisfactory" transistor was not among the rejected groups and is represented by a dotted column extending below the axis. There remains, of course, the total number (128) of "satisfactory" units accepted correctly. The column in our example with the three area distinctions thus indicates:

1. By the height of the bar over the axis, the number (31) of transistors rejected;
2. by the white area, the number (30) of "satisfactory" units rejected in error, which is related to the "producer's risk";
3. by the black area, the number (1) of "unsatisfactory units rejected correctly;
4. by the dotted area, the number (1) of "unsatisfactory" units accepted in error, which is related to the "consumer's risk."

It is important to recognize that the time scales of figures 4, 5, and 6 refer to performance at 100 °C, a temperature which can be expected to produce more rapid aging than those ordinarily encountered in normal usage. Aging corresponding to a junction temperature of 55 °C would be more realistic and may be conservatively estimated by multiplying the time scale by a factor of ten. The basis for this procedure was discussed in the previous section.

A comparison of figures 4, 5, and 6 sets figure 4 apart by the relatively larger number of "unsatisfactory" units accepted (associated with "consumer's risk"), even though the corresponding errors associated with "producer's risk" are roughly comparable. It appears that a substantial reduction in the risk to the consumer is gained (without unduly increasing risk to the producer) by extending the screening stress to 1,000 hr rather than terminating at 340 hr.

There are several distinctions which should be noted between figures 5 and 6. The difference in screening results between the 5 percent steps of figure 6, despite the smaller increments, is more pronounced than that between the 15 percent steps of figure 5. This may have been expected because 340- to 1,000-hr ratio values of figure 6 form a more compact distribution (shown in figure 3) than the values for figure 5 (shown in figure 2). The effective use of the information in figure 6 requires a finer measurement distinction. The need for finer distinctions is obviously undesirable; as the necessary resolution approaches the magnitude of measurement error, the effectiveness of fine distinctions evaporates. Stated in other words, one of the desirable qualities of a screening parameter is that it have a broad distribution, and one of the essential qualities is that its dispersion be large relative to measurement error. For these reasons the criteria represented in figure 5 are favored. An additional desirable quality is the apparent lack of sensitivity of screening results to the choice of the ratio change, whether it be 30 or 60 percent.

On the basis of the factors discussed above, it was decided to eliminate the 340-hr measurement period and use only the observed relative change after being subjected to an accelerated aging stress for 1,000 hr, as illustrated in figure 5.

8. Second Experiment

The value of the screening concept discussed in this report depends, to a large extent, upon the relation of early-changes versus deterioration being a general behavioral characteristic, a characteristic which other types of transistors and transistors of different manufacture have in common. The completion of a modest second experiment tends to confirm that the relationship does exist for other types and manufacture of germanium alloy transistors.

As a sequel to the first experiment, a second was initiated, wherein approximately 125 °C junction temperature screening stress was applied for 1,000 hr and then reduced to 100 °C for continued aging. The parameters measured were identical, and the form of the data was similar to that of the first experiment. It was, therefore, a simple matter to apply the screening criteria to the data without foreknowledge of the actual performance. For this reason, and the fact that the data of the second experiment are independent of those used (in the first experiment) in development of the screening test, the second experiment provides a valid basis for evaluation of the effectiveness of the screening procedure.

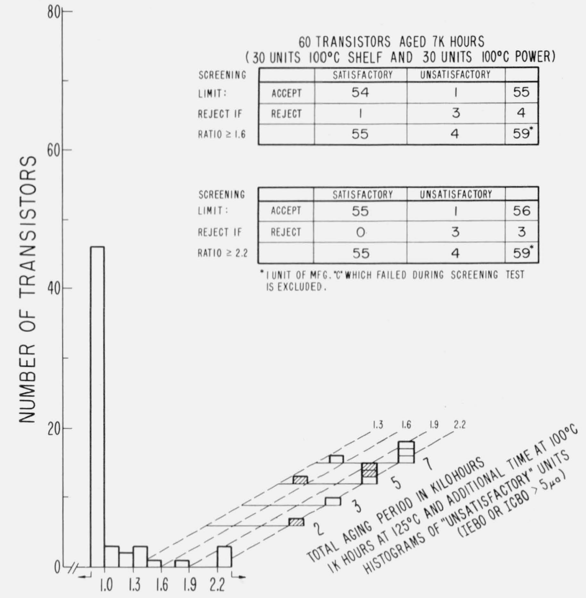
The second experiment consisted of applying a screening test and then aging all units for nearly one year. The experiment included a group of 40 type R212 transistors of manufacture B, 40 of manufacture C, and 40 type 2N396 transistors of manufacture E. The 2N396 units are the same type and manufacture as those used in the first experiment. Furthermore, an effort was made to compare results of two different forms of screening stress. Half the transistors were exposed to a 1,000-hr bake screening stress of 125 °C with no applied power. The remaining half of the transistors were exposed to a contrasting screening stress having a low ambient temperature combined with a high power dissipation calculated to produce the same 125 °C junction temperature. The latter stress was obtained with an ambient temperature of −65 °C (which is a commonly accepted temperature test point) combined with the calculated bias power of 760 mW.

The calculations were based on measured values of thermal resistance. The thermal resistance of the units of manufacture B was somewhat higher than that of the other two groups. It was decided, since ratings were similar, to apply the same bias power for all three groups, even though the estimated rise in junction temperature would be approximately 5 percent greater for the units of manufacture B. This later proved to be a crucial decision resulting in rapid deterioration of units of manufacture B.

After completion of the two screening tests, the two groups were again subdivided, half of each group being subjected to 6,000 hr of 100 °C shelf aging and the remaining half subjected similarly to power aging. The estimated 100 °C junction temperature for power aging was obtained with the combination of 70 °C ambient temperature and 120 mW of bias power (condition 14 in table 3).

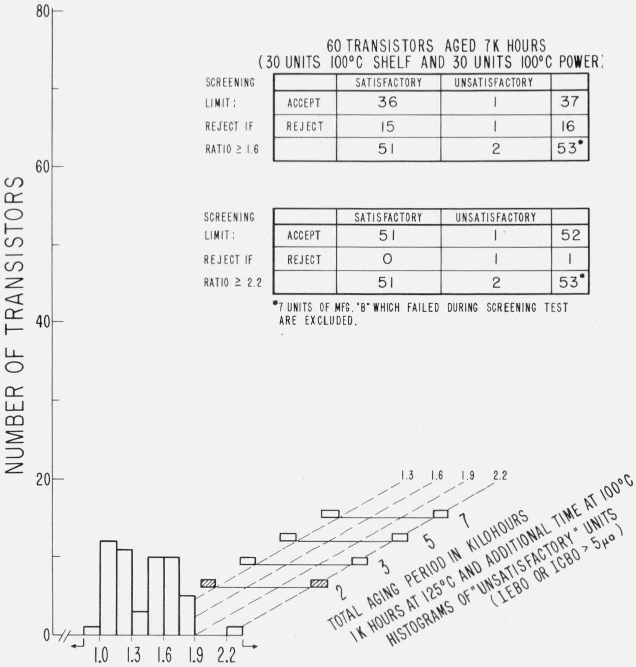
Figure 7 summarizes the results of the 125 °C bake stress screening test. Similarly, figure 8 summarizes the results of the power stress screening test. The criterion for "satisfactory" performance was that IEBO and ICBO at 10 V must be no greater than 5 μA, as called for in the procurement specification for R212 transistors. Referring to the histograms, which show the distribution of fractional changes in junction leakage (IEBO or ICBO, whichever is the larger) induced by the screening stress, in figure 7 the pronounced mode lies below 1.0 and contrasts sharply with the bimodal distribution in figure 8, where both modes lie above 1.0. This indicates that the 125 °C shelf stress produced a reasonably uniform decrease in leakage current for all three manufacturers' transistors, whereas the nominal 125 °C power stress produced nonuniform increases in leakage current. The nonuniformity was due mainly to the R212 transistors of manufacture B exhibiting substantial deterioration; the leakage current increased in value to the extent that it exceeded 5 μA in 7 out of 20 transistors. Since these seven units no longer met the criterion for "satisfactory" performance, they were removed from the experiment. It is likely that the deterioration of these units was caused by excessively high junction temperature. As was mentioned earlier, the thermal resistance of the transistors of manufacture B was somewhat higher than that of the others and was calculated to produce a junction temperature more nearly 135 °C than the estimated 125 °C of the others. In sharp contrast to the above described deterioration under the power screening stress, the transistors of manufacture B exhibited the least degradation during the 125 °C shelf screening stress or the prolonged 100 °C shelf or power aging stress. The collective results of this experiment indicate that the effects of the power screening stress used was critically sensitive to the difference in thermal resistance and could have led to erroneous conclusions regarding the relative merits of the units of manufacture B. These results illustrate the possible hazards of applying uniformly, to a given type of transistor, excessive power as a means for screening or accelerating aging effects.

Referring again to figures 7 and 8, the relationship between fractional changes in leakage current and subsequent aging is shown for aging periods extending from 2,000 to 7,000 hr, as was done in a similar fashion in figures 1, 2, and 3. Although two aging conditions were used, a 100 °C bake stress and a 100 °C junction temperature obtained with applied power, the limited volume of data indicated no significant difference in aging behavior and, therefore, data from the two conditions were combined. The effectiveness of the screening process is illustrated in the two boxes in the upper portions of figures 7 and 8. The screening criterion of 1.6 ratio or greater, in the upper box, was



HISTOGRAM OF RATIO VALUES SHOWING CHANGE IN IEBO OR ICBO AFTER 1,000 HOURS OF SHELF AGING AT 125° C.

FIGURE 7. *Analysis of 125 °C screening test (shelf).*



HISTOGRAM OF RATIO VALUES SHOWING CHANGE IN IEBO OR ICBO AFTER 1,000 HOURS OF POWER AGING AT ESTIMATED 125° JUNCTION TEMPERATURE.

FIGURE 8. *Analysis of 125 °C screening test (power).*

chosen because it is the largest of those used in the first experiment, and therefore allows comparison of the results. Since the screening stress was larger (125 °C), a second analysis was made using a larger value as a screening criterion. The second value, 2.2, was the largest one available without reprocessing the data and, fortunately, appears to be a reasonable choice.

The footnote under the boxes of figure 7 indicates that one unit of manufacture C failed, i.e., became "unsatisfactory," during the shelf screening test. Although such a failure may offhand appear to indicate rapid and destructive deterioration at 125 °C shelf stress (as was discussed for the 7 units of manufacture B which failed under the power screening stress), such a conclusion is surely questionable in light of the fact that one out of four of the same manufacturer's units also failed while subjected to 25 °C shelf storage, which was part of an experiment control.

Comparison of the screening summaries indicates superior results for the shelf-stress screen of figure 7. Such comparisons are usually difficult because of the several factors which should be considered. A better intuitive understanding may be reached for judging the effectiveness of the different screening tests by examining the summary in table 2. This table compares the relative number of "unsatisfactory" transistors present before screening with the number present after screening. An indication of the cost of the improvement through screening is given in terms of the relative number of "unsatisfactory" units rejected correctly compared to the total number rejected. The latter ratio indicates the (fractional) number of units rejected correctly.

TABLE 2. *Summary of effectiveness of screening tests*

Screening test (125 °C)		Relative number of "unsatisfactory" units present		Rejected correctly / Total rejected
Stress	Limit	Before screening	After screening	
Shelf	1.6	4/59 or 6.8%	1/55 or 1.8%	3/4 or 75%
	2.2		1/56 or 1.8%	3/3 or 100%
Power	1.6	2/53 or 3.8%	1/37 or 2.7%	1/16 or 6%
	2.2		1/52 or 1.9%	1/1 or 100%

This summary shows that for shelf stress screening, the two screening limits (1.6 and 2.2) were almost equally effective. For the power stress screening, however, the results were very sensitive to the choice of limit. The 2.2 value was preferred by far because the 1.6 limit caused 15 "satisfactory" units to be rejected in error. This is a relatively poor showing compared to the other three outcomes.

The results of the shelf screening test, even though the screening stress (125 °C) is somewhat more severe than that used in the first experiment (100 °C), support the general findings of the earlier experiment. The fractional change in leakage current appears to provide a useful measure of expected performance.

9. Conclusion

A study of the aging behavior of low-power germanium alloy switching transistors has revealed a relationship between small changes in junction leakage current, associated with a brief aging stress, and later deterioration in performance. Other parameters studied were ICES, ICER, ICEO, and 1 + hFB, which were measured, and the voltage sensitive component of the leakage current, the intrinsic leakage current, and hFE*, which were computed. With the possible exception of hFE*, none of these parameters appeared promising for stress-screening purposes.

These findings apply to transistors which had been accepted for stringent military requirements and were considered "high reliability" units. They had conformed to military acceptance specifications which had included a series of measurements on each device. It was not surprising, therefore, that the NBS 0-hr measurements proved to be of little value as a screening criterion. Even the variable or noisy character of some of the 0-hr measurements offered little hope as an indicator of expected performance. Shifts or jumps in parameter values while lightly tapping the transistor case, however, proved to be quite useful. Six type 2N396 transistors having fractured wafers or other mechanical faults were clearly identified while making preliminary measurements using this procedure, and were not included in the aging study.

The observed junction leakage current relationship to aging appears characteristic of several types and manufactures of germanium-alloy transistors. This relationship may provide the basis for a promising nondestructive screening procedure which would serve for the identification of germanium-alloy transistors likely to deteriorate through excessive growth in junction leakage current. Since leakage current deterioration has continued to be one of the more common forms of degradation in transistor performance, a screening procedure which is effective in guarding against such a fault would be of substantial value.

The proposed screening procedure involves the determination of relatively small changes in junction leakage current, increases of the order of 15 percent or more, associated with 1,000 hr of aging at a shelf (bake) stress of 100 °C. Because the leakage current changes of interest are small, high demands are placed upon measurement repeatability. A number of factors are important in maintaining the necessary long-term repeatability. There is need for operating procedures which provide a record of proof of stable performance through a history of frequent calibration and through a history of measurements on a group of "control" transistors. Also, the measurement procedure should treat each transistor alike. A stabilization or "soaking" period of a fixed duration (24 hr $\pm$ 2 hr) under measurement ambient conditions prior to measurement should be incorporated in the test procedure so as to minimize the transient recovery effects associated with the removal of the transistor from a high-temperature aging stress environment.

Relatively close ambient temperature control during measurement is essential. The very close control of ±0.01 °C of the NBS measurement facility, although proven to be a key feature in the aging studies, is unnecessarily stringent. Commercial equipment having control with ±0.1 or 0.2 °C is adequate for the leakage-current bake-stress screening described in this paper.

The initial choice of value of fractional change in junction leakage current as the screening limit is necessarily somewhat arbitrary. There is evidence that even transistors bearing identical type numbers but of different manufacture might require different screening limits. Once an initial choice is made, however, an *a posteriori* aging test of all rejected units and sample groups of accepted units is recommended as an evaluation procedure for monitoring the screening effectiveness and for improving the choice of screening limits. These procedures are now being followed at NBS in a further study of the proposed screening procedure as applied to much larger groups of transistors and to germanium transistors of different construction.

10. Appendix

A total of 516 germanium low-power alloy-junction switching-type transistors (type 2N396), obtained from a single manufacturer, were aged under 13 different combinations of ambient temperature, collector voltage, and collector current. The thirteen aging conditions are summarized in table 3, from which it may be seen that these conditions form an incomplete factorial experiment. Each condition is identified by a number in the lower left corner of each box. Each condition contained 40 transistors mounted on four plugs.

Immediately prior to being subjected to its aging environment, each transistor was measured twice, a morning group of 10 parameter measurements being replicated in the afternoon of the same day. During the course of the experiment, the transistors were periodically removed from their aging environments and the 10 parameters were measured four times before the aging treatments were again applied. The measurement period began with removal of the transistors from the aging environment, after which

Table 3 Aging Conditions

	Tj=25 °C	Tj=55 °C	Tj=100 °C	Tj=145 °C	Tj=200 °C	
VCB=0v	PC=0mw, Ta=25°C, ΔTj=0°C STA PLUG: 1 1000; 2 1002; 3 1004; 4 1006 1 (0,0,25)25	7	PC=0mw, Ta=100°C, ΔTj=0°C STA PLUG: 5 1040; 6 1042; 7 1044; 8 1046 13 (0,0,100)100	19	PC=0mw, Ta=200°C, ΔTj=0°C STA PLUG: 1 1096; 2 1098; 3 1904; 4 1906 25 (0,0,200)200	I_c=0ma
VCB=3v	2	PC=120mw, Ta=25°C, ΔTj≈30°C STA PLUG: 1 1016; 2 1018; 3 1020; 4 1022 8 (3,120,25)55	PC=120mw, Ta=70°C, ΔTj≈30°C STA PLUG: 1 1048; 2 1050; 3 1052; 4 1054 14 (3,120,70)100	PC=120mw, Ta=115°C, ΔTj≈30°C STA PLUG: 5 1072; 6 1074; 7 1076; 8 1078 20 (3,120,115)145	26	I_c=40ma
	3	PC=3mw, Ta=55°C, ΔTj≈1°C STA PLUG: 5 1024; 6 1026; 7 1028; 8 1030 9 (3,3,55)55	PC=3mw, Ta=100°C, ΔTj≈1°C STA PLUG: 5 1056; 6 1058; 7 1060; 8 1062 15 (3,3,100)100	PC=3mw, Ta=145°C, ΔTj≈1°C STA PLUG: 1 1080; 2 1082; 3 1084; 4 1086 *21 (3,3,145)145	27	I_c=1ma
VCB=12v	4	10	16	22	28	
	5	PC=480mw, Ta=-65°C, ΔTj≈120°C STA PLUG: 1 1032; 2 1034; 3 1036; 4 1038 11 (12,480,-65)55	17	PC=480mw, Ta=25°C, ΔTj≈120°C STA PLUG: 5 1088; 6 1090; 7 1092; 8 1094 23 (12,480,25)145	29	I_c=40ma
VCB=24v	PC≈0mw, Ta=25°C, ΔTj=0°C STA PLUG: 5 1008; 6 1010; 7 1012; 8 1014 6 (24,0,25)25	12	PC≈0mw, Ta=100°C, ΔTj=0°C STA PLUG: 1 1064; 2 1066; 3 1068; 4 1070 18 (24,0,100)100	24	30	I_c=0ma

OVEN AND COLDBOX AMBIENT TEMPERATURE

-65°C (4 PLUGS) +100°C (12 PLUGS)
+25°C (16 PLUGS) +115°C (4 PLUGS)
+55°C (4 PLUGS) +145°C (4 PLUGS)
+70°C (4 PLUGS) +200°C (4 PLUGS)

POWER CONDITIONS

SHELF AGING (12 PLUGS)
0mw, 0ma, 24v (8 PLUGS)
3mw, 1ma, 3v (12 PLUGS)
120mw, 40ma, 3v (12 PLUGS)
480mw, 40ma, 12v (8 PLUGS)

NOTES

1—PLUG 1910 IS CONTROL PLUG
2—CONDITION 25 CONTAINS 4 PLUGS WITH MIXED WEEK OF MANUFACTURE.
3—(VCB, PC, Ta)Tj IS CODING USED FOR BOTTOM LINE IN EACH CONDITION.
*4—LEVEL OF CURRENT IN CONDITION 21 INCREASED TO 4ma, PC=12mw AND ΔTj≈3°C.

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they were permitted to stabilize for 24 hr at 25 °C. During the morning of the second day of the measurement period, the 10 parameters were measured and a replicate set of measurements made during the afternoon. The transistors were then permitted to stabilize for an additional seven days, the a.m. and p.m. sets of measurements being repeated during the eighth day of the measurement period. A computer was used to compare the a.m. and p.m. replicate measurements and print out all which changed by more than 2 percent. This allowed all such measurements to be reviewed and, if necessary, repeated before returning the transistors to the aging environment.

The first three measurement periods, 340, 1,000, and 2,000 hr, were selected to correspond to those commonly used in aging schedules and specifications. The remaining periods were selected to provide approximately equal log-time intervals between the measurement periods. The intervals so determined are a fixed fraction of the elapsed time, and for this experiment, were roughly 40 percent of the elapsed time. This procedure gave the following total elapsed times at which the measurement periods fell: 3.4, 4.7, 6.0, 8.7, 11, 14, and 20 khr.

The d-c parameters measured, using automatic equipment, were as follows: IEBO and ICBO at 2 and 10 V; ICES, ICER (R = 10 kΩ), and ICEO at 10 V; normal and inverse 1 + hFB at 10 mA and 5 V. The tenth parameter, 1 + hfb, was measured using a 270-Hz small signal. From these measurements a number of additional parameters were computed. The computed parameters provided estimates of: the voltage-sensitive components of the leakage currents, the intrinsic leakage currents, and (1 + hFB)* (the asterisk indicating that the leakage current was subtracted from the measurement of 1 + hFB) and, finally, hFE*.

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